

N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

V _{DSS}	R _{DS(ON)}	Q _g	Q _{gd}	I _D
12V	18mΩ	3.2nC	0.3nC	4.8A

Typ. @ V_{GS} = 4.5V, T_A = +25°C

Description

This 2nd generation Lateral MOSFET (LD-MOS) is engineered to minimize on-state losses and switch ultra-fast, making it ideal for high efficiency power transfer. It uses Chip-Scale Package (CSP) to increase power density by combining low thermal impedance with minimal R_{DS(ON)} per footprint area.

Applications

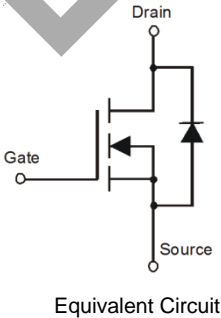
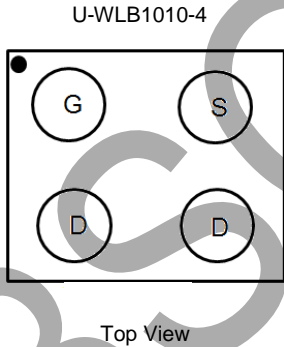
- DC-DC converters
- Battery management
- Load switches

Features

- LD-MOS Technology with the Lowest Figure of Merit: R_{DS(ON)} = 18mΩ to Minimize On-State Losses
Q_g = 3.2nC for Ultra-Fast Switching
- V_{GS(th)} = 0.8V Typ. for a Low Turn-On Potential
- CSP with Footprint 1.0mm x 1.0mm
- Height = 0.62mm for Low Profile
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e.: parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please refer to the related automotive grade (Q-suffix) part. A listing can be found at <https://www.diodes.com/products/automotive/automotive-products/>.**
- **This part is qualified to JEDEC standards (as references in AEC-Q) for High Reliability. <https://www.diodes.com/quality/product-definitions/>**

Mechanical Data

- Package: U-WLB1010-4
- Terminal Connections: See Diagram Below



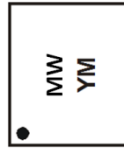
Ordering Information (Note 4)

Part Number	Package	Packing	
		Qty.	Carrier
DMN1032UCB4-7	U-WLB1010-4	3,000	Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information

U-WLB1010-4



MW = Product Type Marking Code
 YM = Date Code Marking
 Y or \bar{Y} = Year (ex: J = 2022)
 M or \bar{M} = Month (ex: 9 = September)

Date Code Key

Year	2013	...	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031
Code	A	...	J	K	L	M	N	O	P	R	S	T

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	12	V
Gate-Source Voltage	V _{GS}	±8	V
Continuous Drain Current (Note 5) V _{GS} = 4.5V	Steady State	T _A = +25°C	4.8
		T _A = +70°C	3.8
Continuous Drain Current (Note 5) V _{GS} = 2.5V	Steady State	T _A = +25°C	4.5
		T _A = +70°C	3.6
Pulsed Drain Current (Note 6)	I _{DM}	15	A

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 7)	P _D	0.9	W
Thermal Resistance, Junction to Ambient @T _A = +25°C (Note 7)	R _{θJA}	138.81	°C/W
Thermal Resistance, Junction to Case @T _C = +25°C (Note 7)	R _{θJC}	31.77	°C/W
Power Dissipation (Note 5)	P _D	1.16	W
Thermal Resistance, Junction to Ambient @T _A = +25°C (Note 5)	R _{θJA}	107.59	°C/W
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C

- Notes:
- Device mounted on FR4 material with 1inch² (6.45cm²), 2oz. (0.071mm thick) Cu.
 - Repetitive rating, pulse width limited by junction temperature.
 - Device mounted on FR-4 PCB with minimum recommended pad layout, single sided.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV _{DSS}	12	—	—	V	V _{GS} = 0V, I _D = 250μA
Zero Gate Voltage Drain Current T _J = +25°C	I _{DSS}	—	—	1.0	μA	V _{DS} = 9.6V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±8V, V _{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	V _{GS(th)}	0.4	0.8	1.2	V	V _{DS} = V _{GS} , I _D = 250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	18	26	mΩ	V _{GS} = 4.5V, I _D = 1A
		—	21	29		V _{GS} = 2.5V, I _D = 1A
		—	27	38		V _{GS} = 1.8V, I _D = 1A
Forward Transfer Admittance	Y _{fs}	—	8.1	—	S	V _{DS} = 6V, I _D = 1A
Diode Forward Voltage	V _{SD}	—	0.7	1.0	V	V _{GS} = 0V, I _S = 1A
Reverse Recovery Charge	Q _{rr}	—	1.2	—	nC	V _{dd} = 5V, I _F = 1A, di/dt = 100A/μs
Reverse Recovery Time	t _{rr}	—	10.5	—	ns	
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C _{iss}	—	325	450	pF	V _{DS} = 6V, V _{GS} = 0V, f = 1MHz
Output Capacitance	C _{oss}	—	183	250		
Reverse Transfer Capacitance	C _{rss}	—	31	47		
Series Gate Resistance	R _G	—	3.1	—	Ω	f = 1MHz, V _{GS} = 0V, V _{DS} = 0V
Total Gate Charge	Q _g	—	3.2	4.5	nC	V _{GS} = 4.5V, V _{DS} = 6V, I _D = 1A
Gate-Source Charge	Q _{gs}	—	0.4	—		
Gate-Drain Charge	Q _{gd}	—	0.3	—		
Gate Charge at V _{th}	Q _{g(th)}	—	0.2	—		
Turn-On Delay Time	t _{D(on)}	—	3.3	10	ns	V _{DS} = 6V, V _{GS} = 4.5V, R _G = 20Ω, I _D = 1A
Turn-On Rise Time	t _r	—	5.6	—		
Turn-Off Delay Time	t _{D(off)}	—	24	36		
Turn-Off Fall Time	t _f	—	9	—		

Notes: 8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to production testing.

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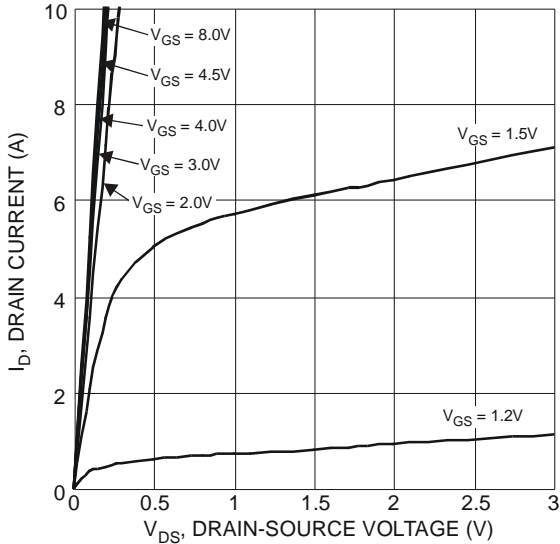


Figure 1 Typical Output Characteristics

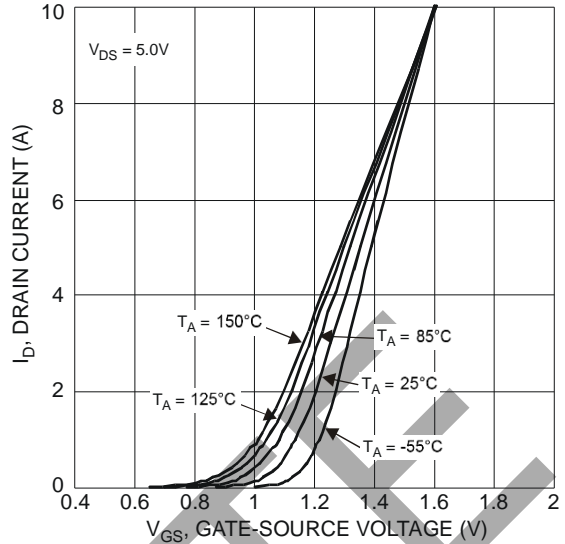


Figure 2 Typical Transfer Characteristics

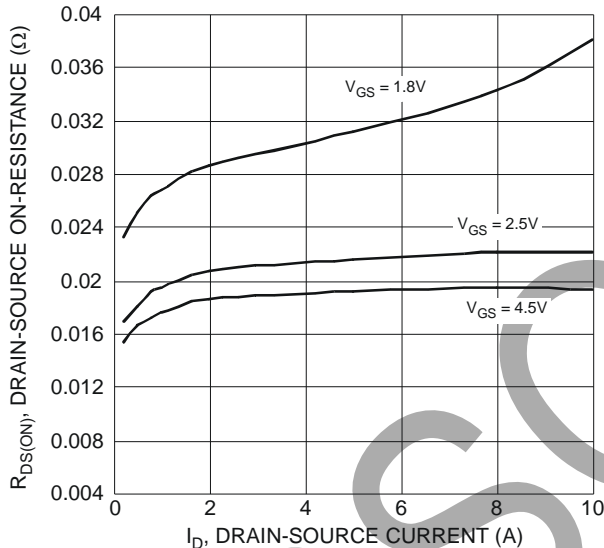


Figure 3 Typical On-Resistance vs. Drain Current and Gate Voltage

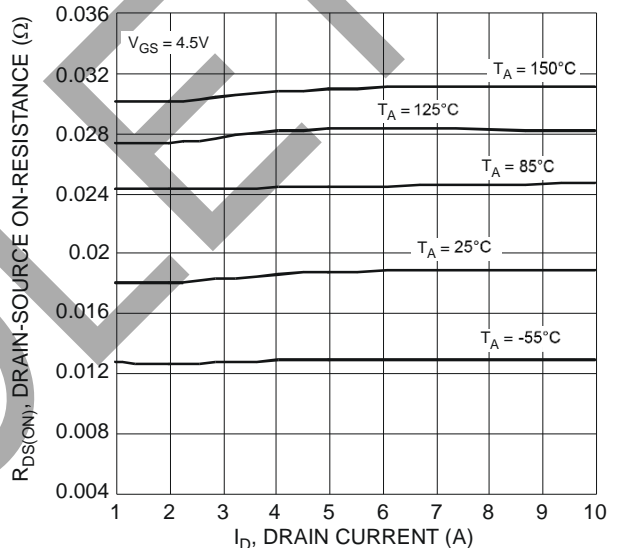


Figure 4 Typical On-Resistance vs. Drain Current and Temperature

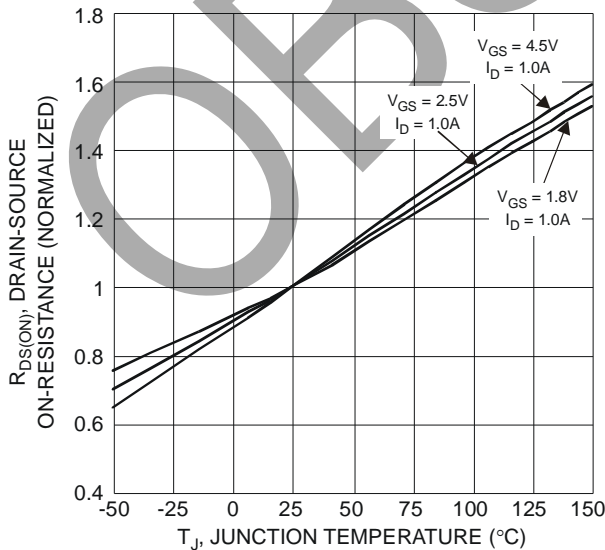


Figure 5 On-Resistance Variation with Temperature

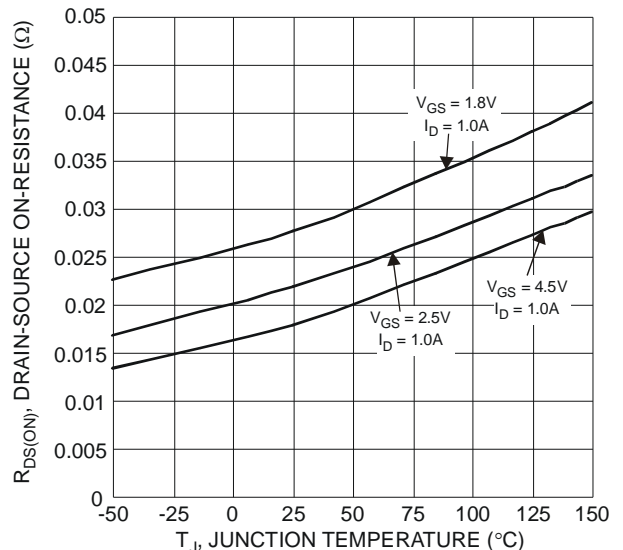


Figure 6 On-Resistance Variation with Temperature

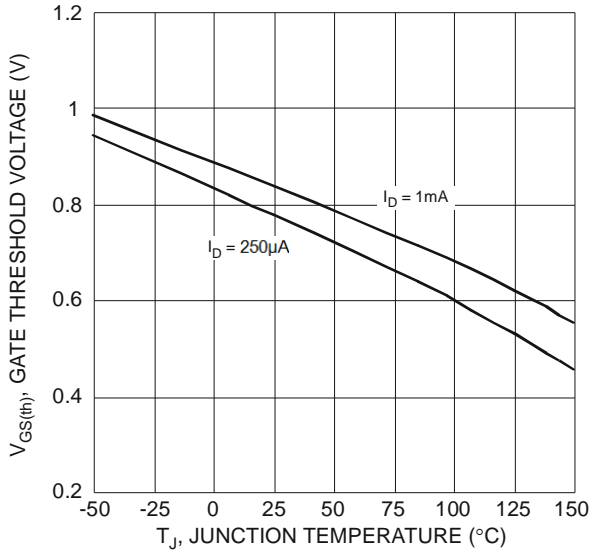


Figure 7 Gate Threshold Variation vs. Junction Temperature

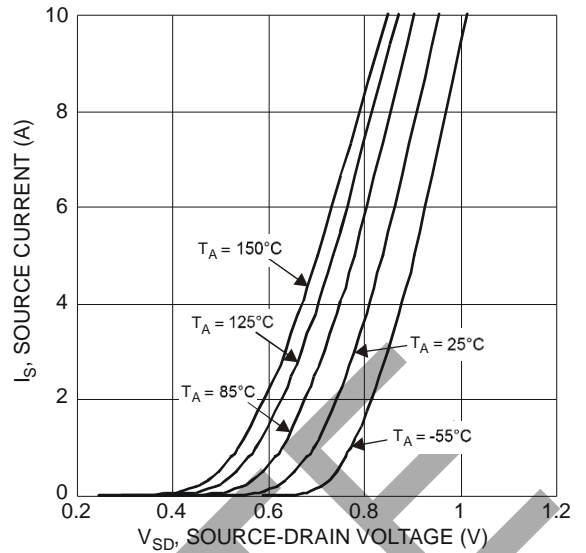


Figure 8 Diode Forward Voltage vs. Current

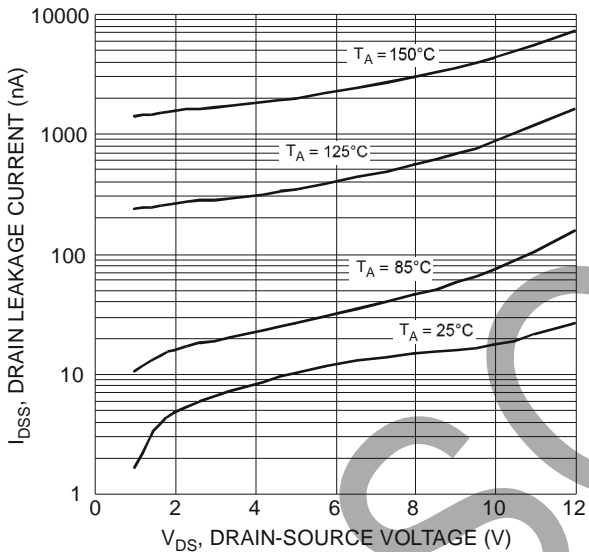


Figure 9 Typical Drain-Source Leakage Current vs. Voltage

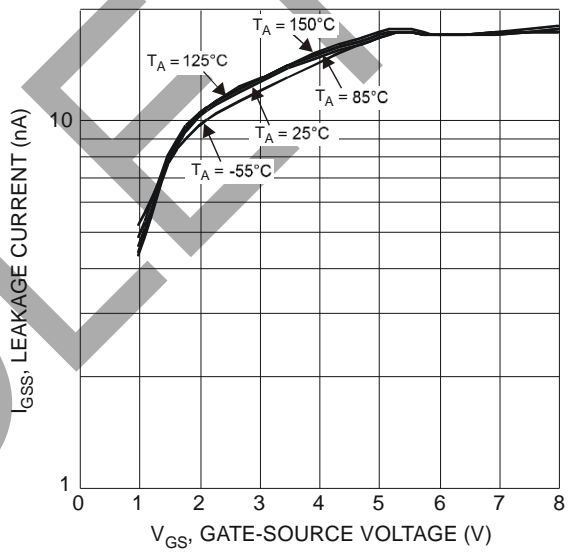


Figure 10 Gate-Source Leakage Current vs. Voltage

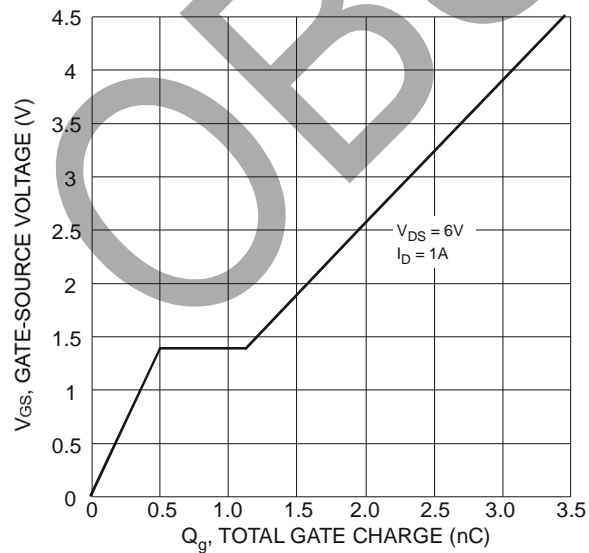


Figure 11 Gate Charge

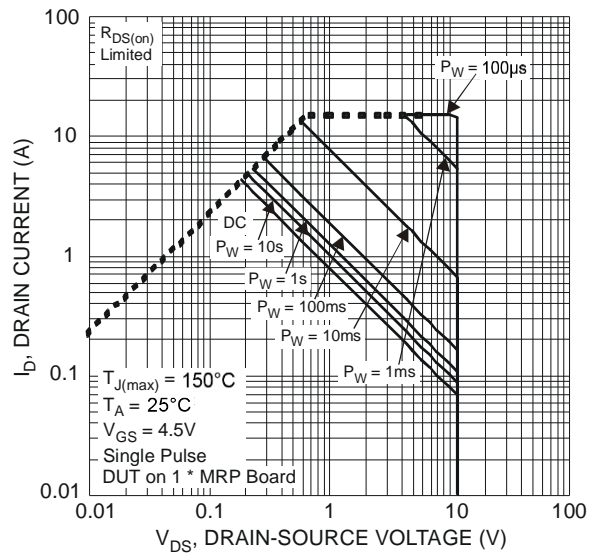
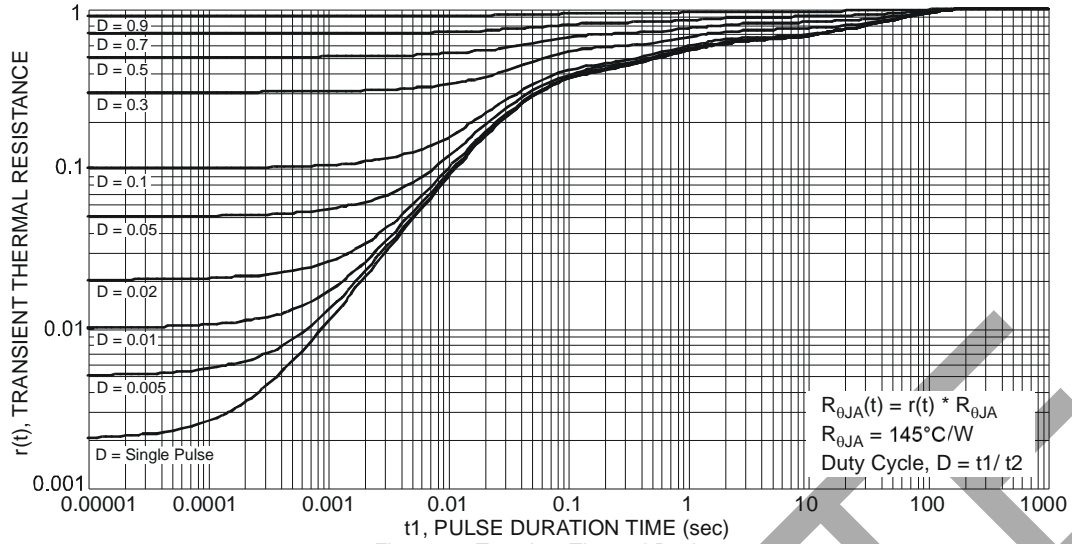


Figure 12 SOA, Safe Operation Area

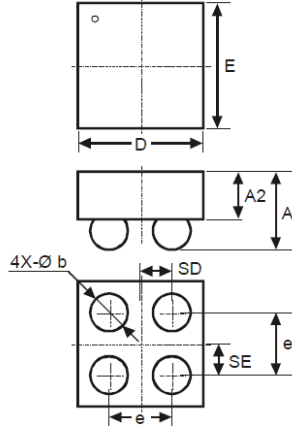


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Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

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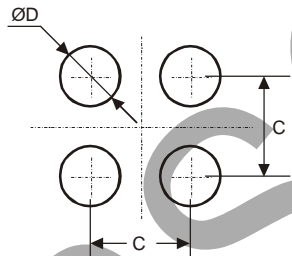


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Dim	Min	Max	Typ
D	0.95	1.05	1.00
E	0.95	1.05	1.00
A	-	0.62	-
A2	-	-	0.38
b	0.25	0.35	0.30
e	-	-	0.50
SD	-	-	0.25
SE	-	-	0.25
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

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Dimensions	Value (in mm)
C	0.50
D	0.25

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