DUAL N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BV_{DSS}	$R_{DS(ON)}$ Max	I_D T_A = +25°C
20V	0.55Ω @ V_{GS} = 4.5V	540mA

Description

This MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

Applications

- Load switches

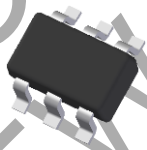
Features

- Dual N-Channel MOSFET
- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Ultra-Small Surface Mount Package
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The DIODES™ DMN2004DWKQ is suitable for automotive applications requiring specific change control; this part is AEC-Q101 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**
  https://www.diodes.com/quality/product-definitions/

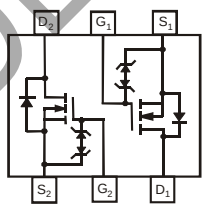
Mechanical Data

- Package: SOT363
- Package Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish—Matte Tin Annealed over Alloy 42 Lead-Frame. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.006 grams (Approximate)

SOT363



Top View



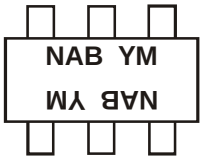
Top View
Internal Schematic

Ordering Information (Note 4)

Part Number	Package	Packing	
		Qty.	Carrier
DMN2004DWKQ-7	SOT363	3,000	Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



NAB = Product Type Marking Code
YM = Date Code Marking
$\overline{Y}$ or Y = Year (ex: J = 2022)
M = Month (ex: 9 = September)

Date Code Key

Year	2016	…	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031
Code	D	…	J	K	L	M	N	O	P	R	S	T

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@ T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	20	V
Gate-Source Voltage			V_{GSS}	±8	V
Drain Current (Note 5)	Steady State	T_A = +25°C T_A = +85°C	I_D	540 390	mA
Pulsed Drain Current (Note 6)			I_{DM}	1.5	A

Thermal Characteristics (@ T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P_D	200	mW
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	625	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@ T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	20	—	—	V	V_{GS} = 0V, I_D = 10µA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	µA	V_{DS} = 16V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±1	µA	V_{GS} = ±4.5V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	0.5	—	1.0	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	0.4 0.5 0.7	0.55 0.70 0.9	Ω	V_{GS} = 4.5V, I_D = 540mA V_{GS} = 2.5V, I_D = 500mA V_{GS} = 1.8V, I_D = 350mA
Forward Transfer Admittance	$\|Y_{fs}\|$	200	—	—	mS	V_{DS} =10V, I_D = 0.2A
Diode Forward Voltage (Note 7)	V_{SD}	0.5	—	1.4	V	V_{GS} = 0V, I_S = 115mA
DYNAMIC CHARACTERISTICS (Note 7)						
Input Capacitance	C_{iss}	—	36	150	pF	V_{DS} = 16V, V_{GS} = 0V f = 1.0MHz
Output Capacitance	C_{oss}	—	5.7	25	pF	
Reverse Transfer Capacitance	C_{rss}	—	4.2	20	pF	
Total Gate Charge (V_{GS} = 4.5V)	Q_g	—	0.53	—	nC	V_{DS} = 10V, I_D = 250mA
Total Gate Charge (V_{GS} = 8.0V)	Q_g	—	0.95	—		
Gate-Source Charge	Q_{gs}	—	0.08	—		
Gate-Drain Charge	Q_{gd}	—	0.07	—		
Turn-On Delay Time	$t_{D(ON)}$	—	4.1	—	ns	V_{DD} = 10V, R_L = 47Ω, V_{GEN} = 4.5V, R_{GEN} = 10Ω
Turn-On Rise Time	t_R	—	7.3	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	13.8	—	ns	
Turn-Off Fall Time	t_F	—	10.5	—	ns	

Notes: 5. Device mounted on FR-4 PCB.
6. Pulse width ≤10µS, Duty Cycle ≤1%.
7. Short duration pulse test used to minimize self-heating effect.

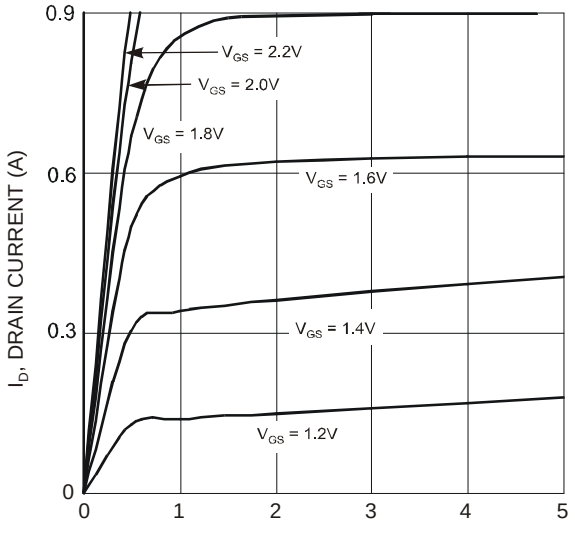


Fig. 1 Typical Output Characteristics

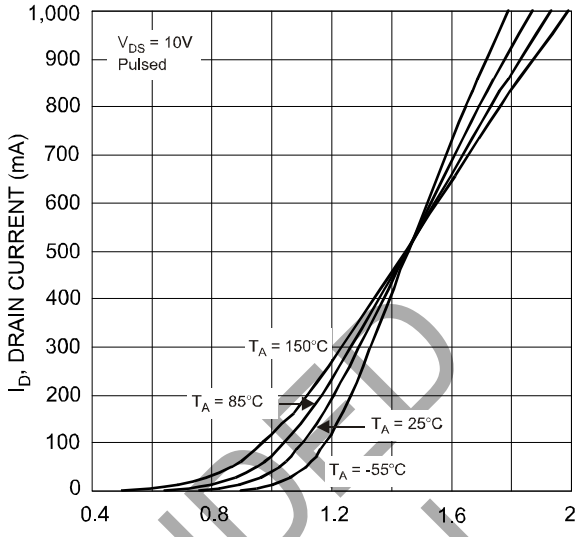


Fig. 2 Reverse Drain Current vs. Source-Drain Voltage

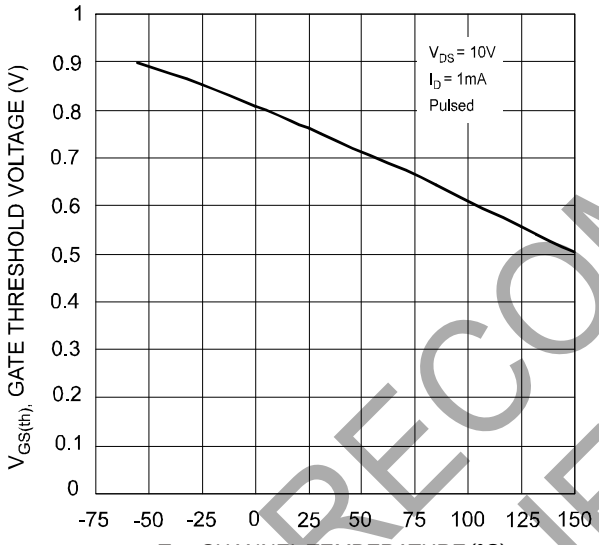


Fig. 3 Gate Threshold Voltage vs. Channel Temperature

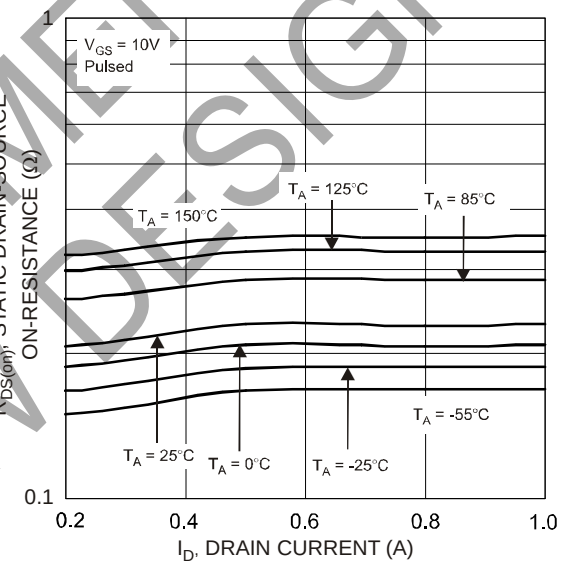


Fig. 4 Static Drain-Source On-Resistance Vs. Drain Current

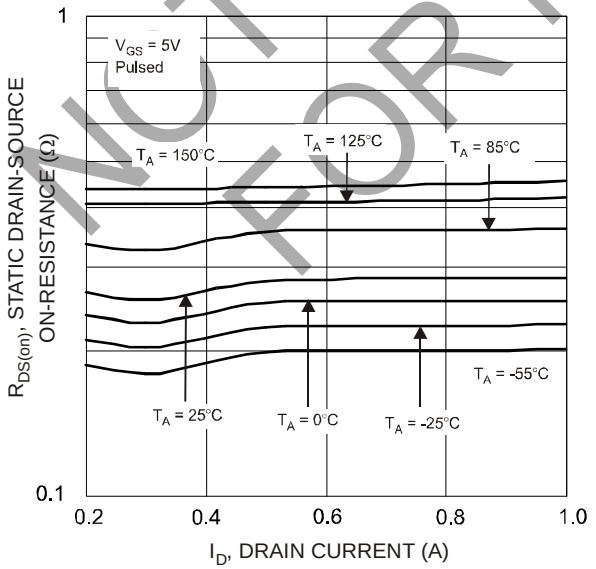


Fig. 5 Static Drain-Source On-Resistance vs. Drain Current

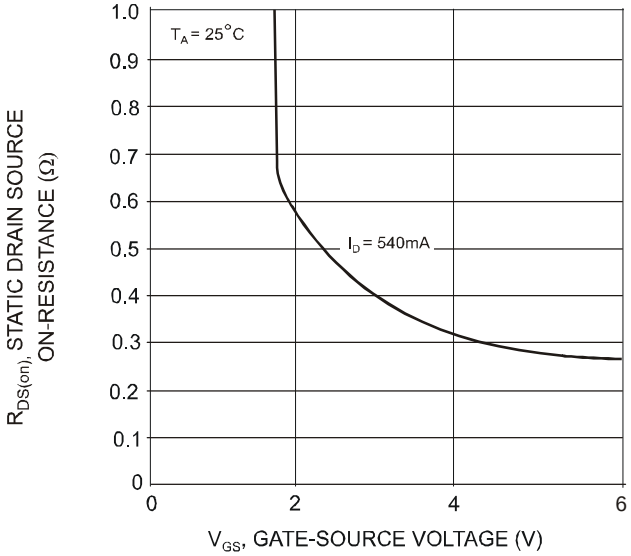


Fig. 6 Static Drain-Source, On-Resistance vs. Gate-Source Voltage

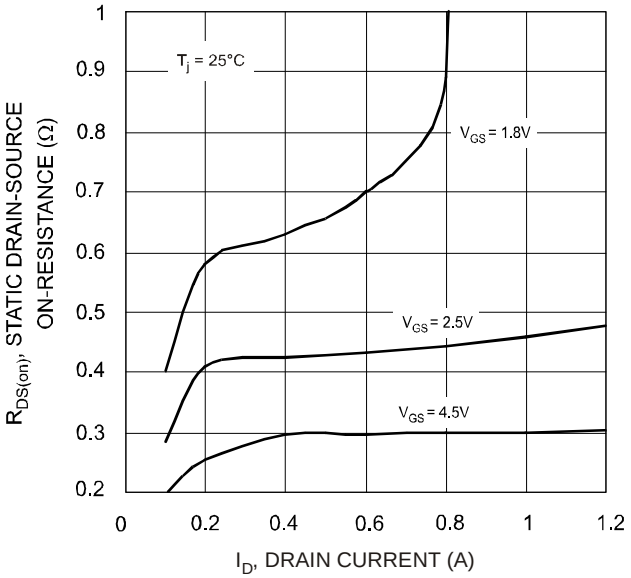


Fig. 7 On-Resistance vs. Drain Current and Gate Voltage

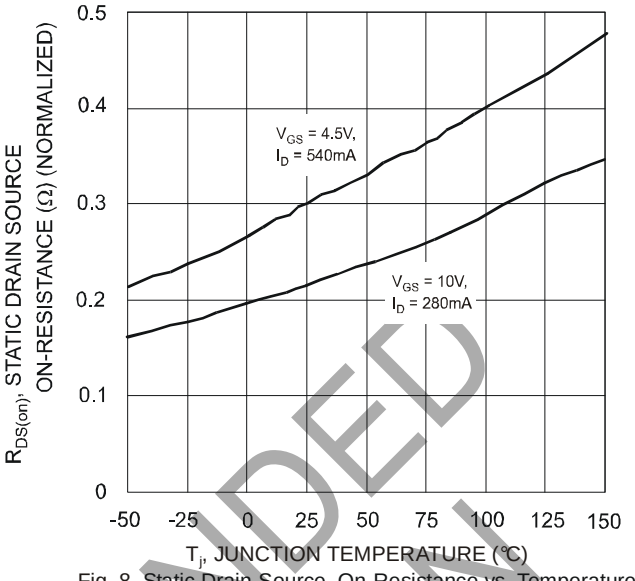


Fig. 8 Static Drain-Source, On-Resistance vs. Temperature

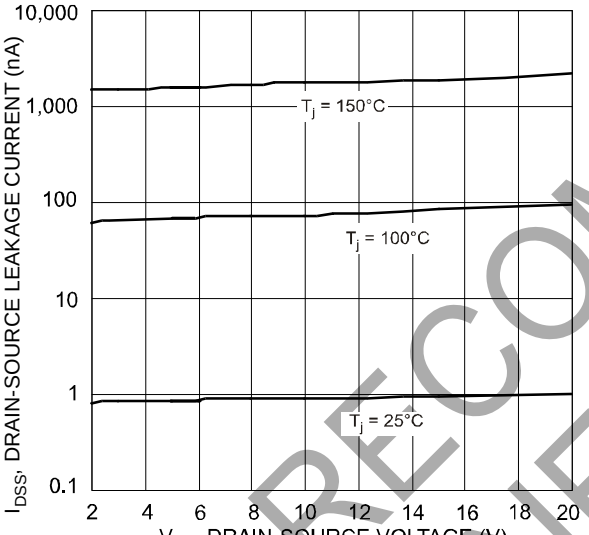


Fig. 9 Drain Source Leakage Current vs. Voltage

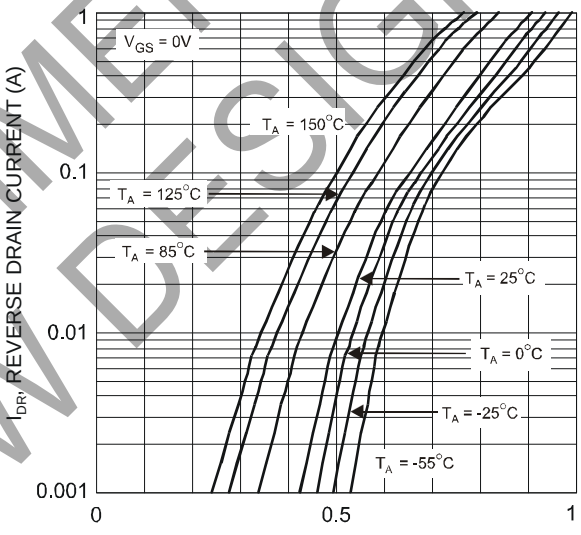


Fig. 10 Reverse Drain Current vs. Source-Drain Voltage

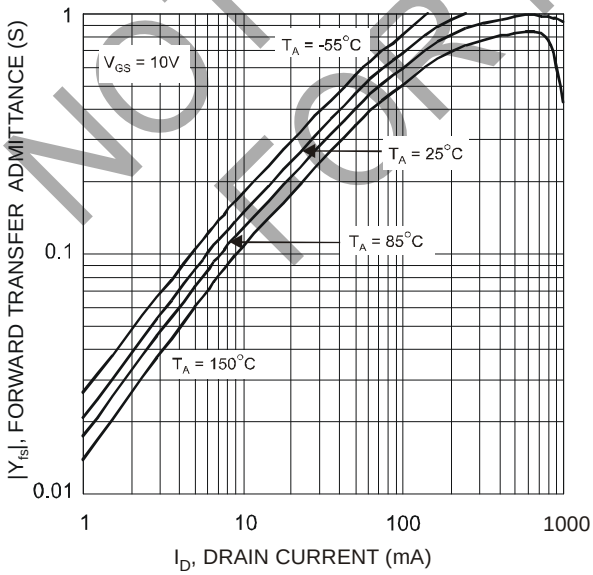


Fig. 11 Forward Transfer Admittance vs. Drain Current

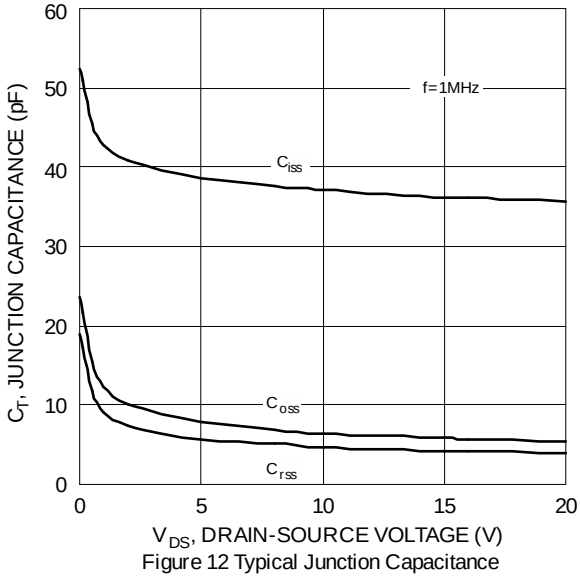


Figure 12 Typical Junction Capacitance

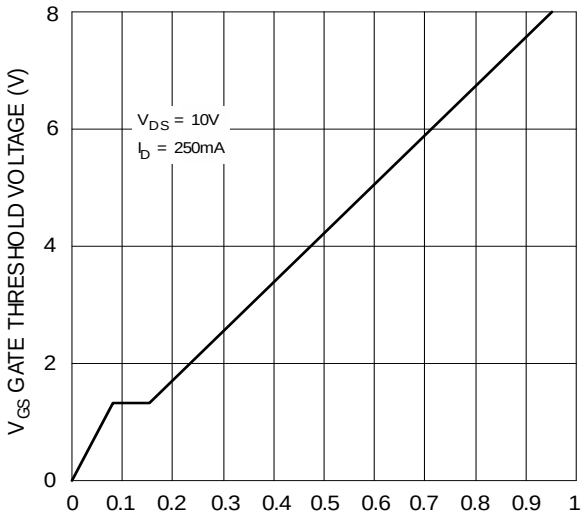


Figure 13 Gate Charge

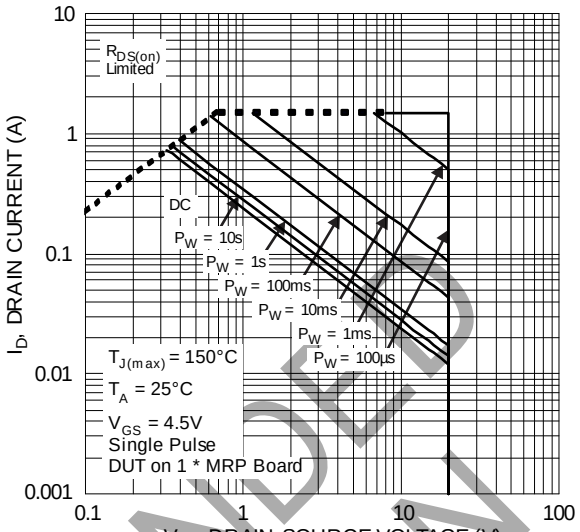


Figure 14 SOA, Safe Operation Area

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

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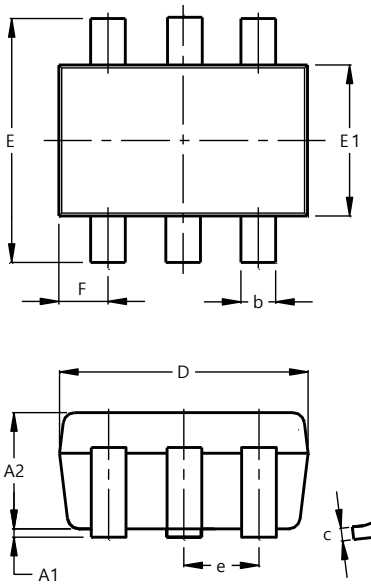

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Dim	**Min**	**Max**	**Typ**
A1	0.00	0.10	0.05
A2	0.90	1.00	0.95
b	0.10	0.30	0.25
c	0.10	0.22	0.11
D	1.80	2.20	2.15
E	2.00	2.20	2.10
E1	1.15	1.35	1.30
e	0.650 BSC		
F	0.40	0.45	0.425
L	0.25	0.40	0.30
a	0°	8°	--
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

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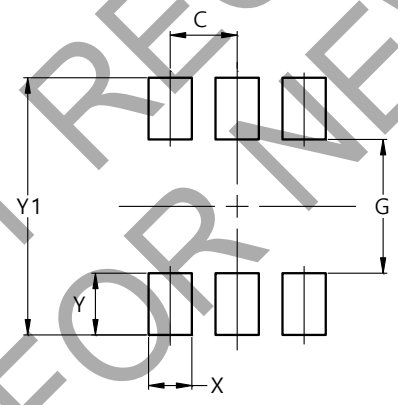

Dimensions	Value (in mm)
C	0.650
G	1.300
X	0.420
Y	0.600
Y1	2.500

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