N-CHANNEL ENHANCEMENT MODE FIELD MOSFET

Product Summary

BV_{SSS}	$R_{SS(ON)}$ Typ	I_S T_A = +25°C
30V	6.7mΩ @ V_{GS} = 10V	16.0A

Description

This new generation MOSFET has been designed to minimize the on-state resistance ($R_{SS(ON)}$) with a 3.37mm x 1.47mm x 0.2mm size yet maintain superior switching performance, making it ideal for high-efficiency power-management applications.

Applications

- Battery management
- Load switches
- Battery protections

Features

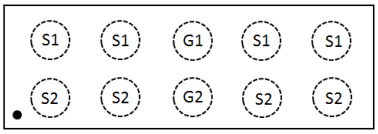
- Built-in G-S Protection Diode Against ESD 1kV HBM
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Mechanical Data

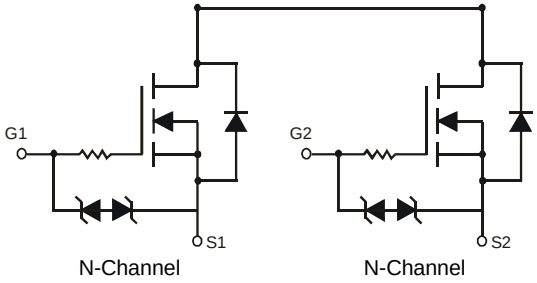
- Package: X4-DSN3415-10
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish – NiAu. Solderable per MIL-STD-202, Method 208 e4
- Weight: 0.0023 grams (Approximate)

ESD PROTECTED

X4-DSN3415-10



Top View



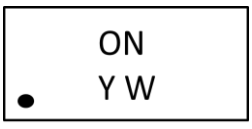
Equivalent Circuit

Ordering Information (Note 4)

Part Number	Package	Packing	
		Qty.	Carrier
DMN38M1SCA10-7	X4-DSN3415-10	3000	Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



ON = Product Type Marking Code
YW = Date Code Marking
Y or $\overline{Y}$ = Year (ex: 3 = 2023)
W or $\overline{W}$ = Week (ex: a = Week 27; z Represents Week 52 and 53)

Date Code Key

Year	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034
Code	3	4	5	6	7	8	9	0	1	2	3	4

Week	1-26	27-52	53
Code	A-Z	a-z	z

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Source-Source Voltage			V_{SSS}	30	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Source Current @T_A = +25°C, V_{GS} = 10V (Note 5)	Steady State	T_A = +25°C T_A = +70°C	I_S	16.0 12.8	A
Continuous Source Current @T_A = +25°C, V_{GS} = 4.5V (Note 5)	Steady State	T_A = +25°C T_A = +70°C	I_S	13.5 10.8	A
Pulsed Source Current @T_A = +25°C (Notes 5 & 6)			I_{SM}	90	A

Thermal Characteristics

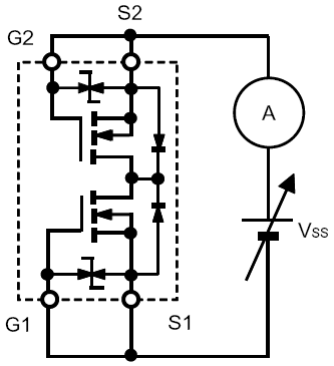
Characteristic	Symbol	Value	Unit
Power Dissipation @T_A = +25°C (Note 5)	P_D	3.0	W
Thermal Resistance, Junction to Ambient @T_A = +25°C (Note 5)	$R_{\theta JA}$	41.6	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

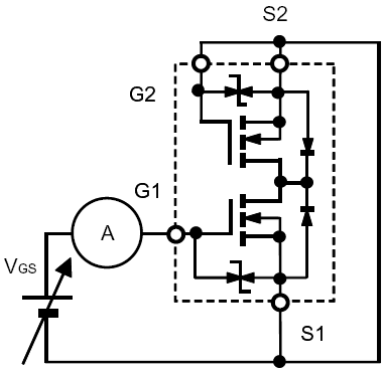
Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Source to Source Breakdown Voltage, T_J = +25°C	BV_{SSS}	30	—	—	V	I_S = 250µA, V_{GS} = 0V, TEST CIRCUIT 1
Zero Gate Voltage Source Current, T_J = +25°C	I_{SSS}	—	—	1.0	µA	V_{SS} = 24V, V_{GS} = 0V, TEST CIRCUIT 1
Gate-Body Leakage	I_{GSS}	—	—	10	µA	V_{GS} = ±20V, V_{DS} = 0V, TEST CIRCUIT 2
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	1.3	—	2.3	V	V_{SS} = 10V, I_S = 250µA, TEST CIRCUIT 3
Static Source-Source On-Resistance	$R_{SS(ON)}$	— —	6.7 8.1	7.8 11	mΩ	V_{GS} = 10V, I_S = 7.0A, TEST CIRCUIT 5 V_{GS} = 4.5V, I_S = 7.0A, TEST CIRCUIT 5
Body Diode Forward Voltage	$V_{F(S-S)}$	—	0.8	1.2	V	I_F = 7.0A, V_{GS} = 0V, TEST CIRCUIT 6
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	1914	—	pF	V_{SS} = 15V, V_{GS} = 0V, f = 1.0MHz TEST CIRCUIT 7
Output Capacitance	C_{oss}	—	185	—		
Reverse Transfer Capacitance	C_{rss}	—	66	—		
Gate Resistance	R_g	—	433	—	Ω	V_{SS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (10V)	Q_g	—	36.7	—	nC	V_{SS} = 15V, I_S = 7A TEST CIRCUIT 9
Total Gate Charge (4.5V)	Q_g	—	16.9	—	nC	
Gate-Source Charge	Q_{gs}	—	5.6	—	nC	
Gate-Drain Charge	Q_{gd}	—	4.1	—	nC	
Gate Charge at V_{TH}	$Q_{g(TH)}$	—	4.1	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	319	—	ns	V_{SS} = 15V R_L = 2.1Ω, I_S = 7A TEST CIRCUIT 8
Turn-On Rise Time	t_R	—	952	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	985	—	ns	
Turn-Off Fall Time	t_F	—	766	—	ns	

Notes: 5. Device mounted on FR-4 material with 1inch^2 (6.45cm^2), 2oz (0.071mm thick) Cu.
6. Repetitive rating, pulse width limited by junction temperature.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to production testing.

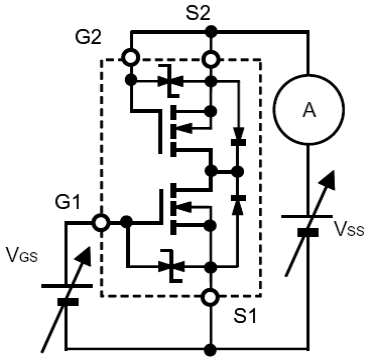
Test Circuits



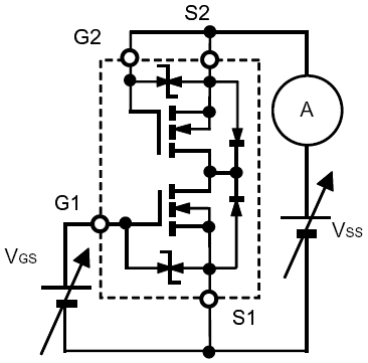
TEST CIRCUIT 1 I_{SSS}



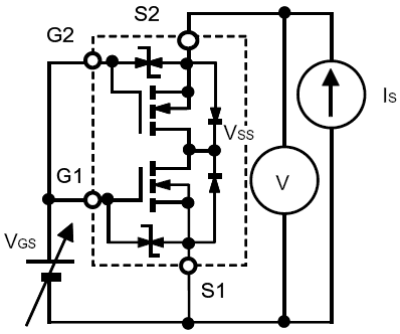
TEST CIRCUIT 2 I_{GSS}
When FET1 is measured, between GATE and SOURCE of FET2 are shorted.



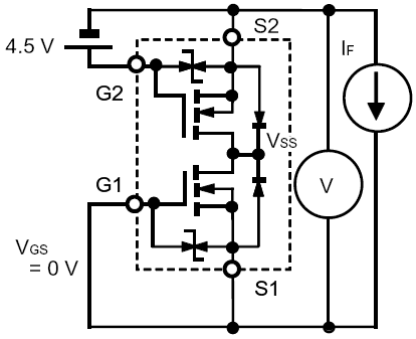
TEST CIRCUIT 3 $V_{GS(OFF)}$
When FET1 is measured, between GATE and SOURCE of FET2 are shorted.



TEST CIRCUIT 4 $|y_{fs}|$
$\Delta I_S/\Delta V_{GS}$

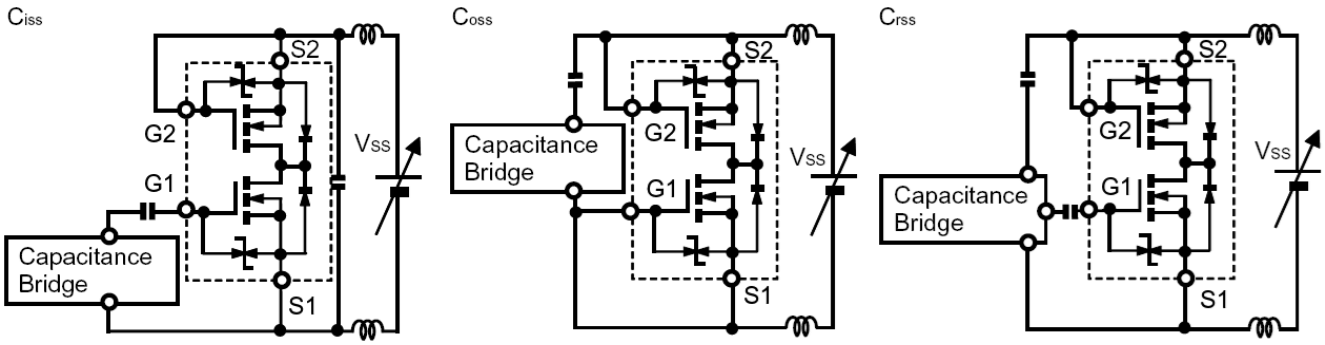


TEST CIRCUIT 5 $R_{SS(ON)}$
V_{SS}/I_S

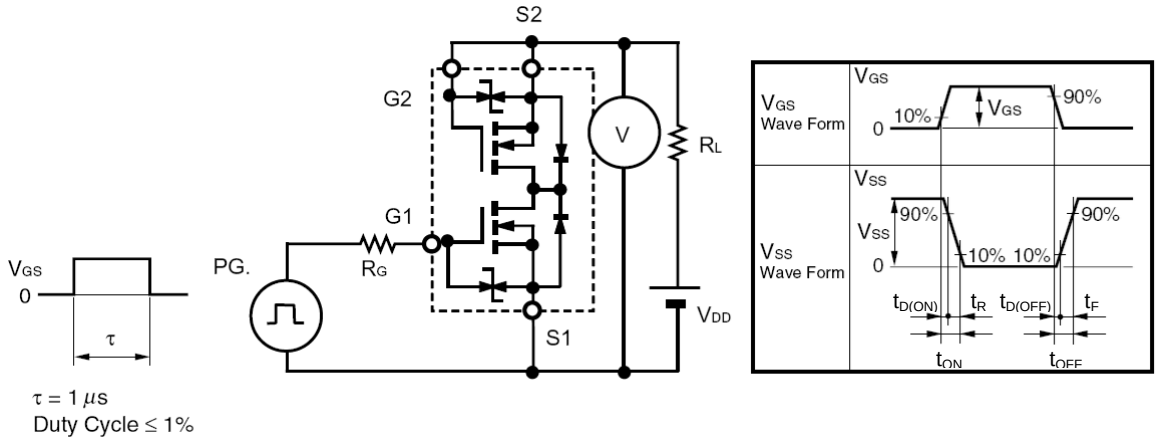


TEST CIRCUIT 6 $V_{F(S-S)}$
When FET1 is measured, FET2 is added V_{GS} +4.5V.

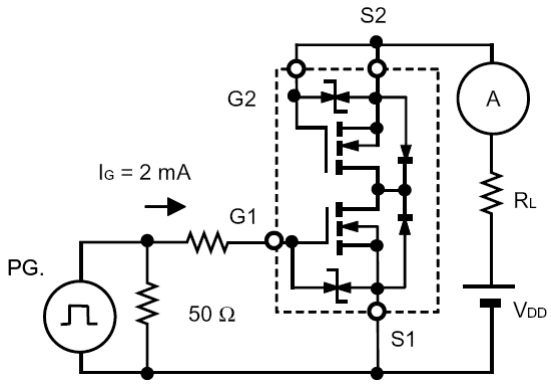
Test Circuits (continued)



TEST CIRCUIT 7



TEST CIRCUIT 8 $t_{D(ON)}$, t_R, $t_{D(OFF)}$, t_F



TEST CIRCUIT 9 Q_g

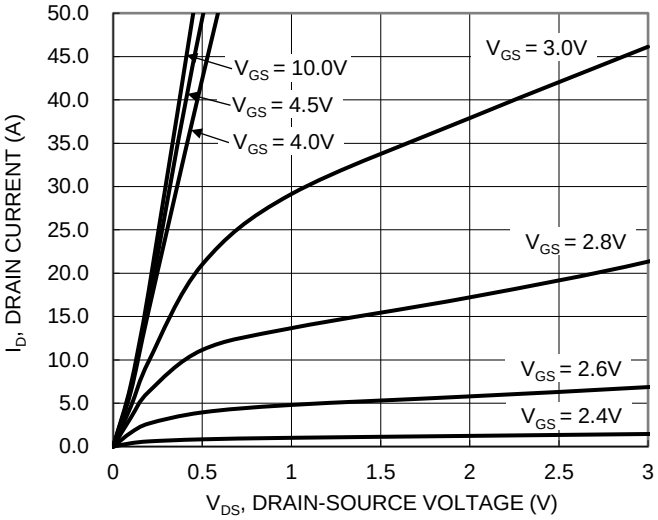


Figure 1. Typical Output Characteristic

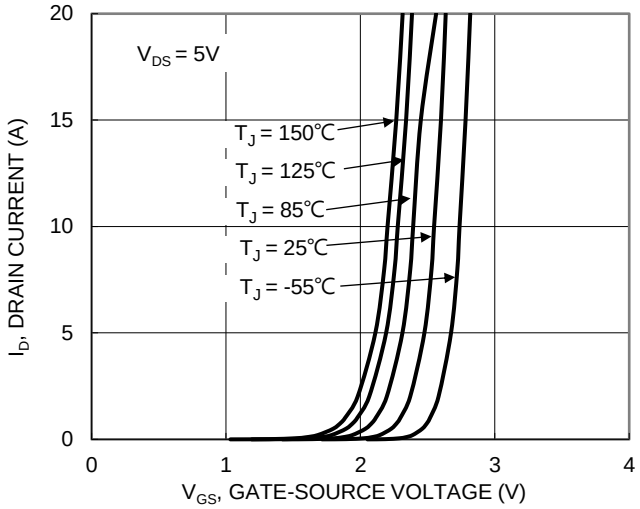


Figure 2. Typical Transfer Characteristic

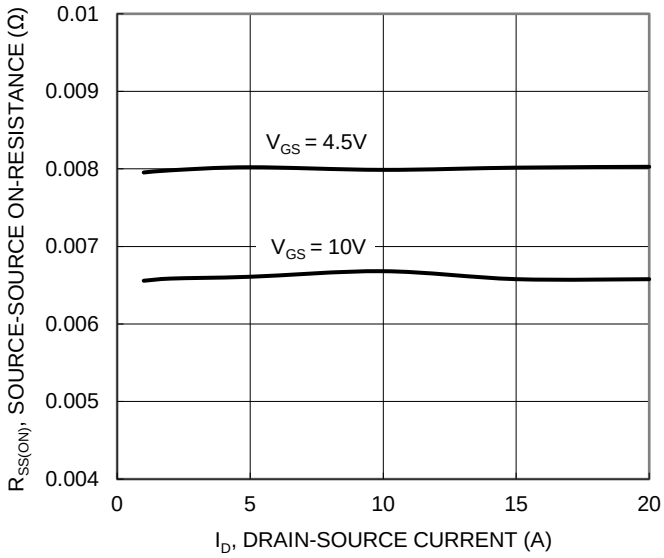


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

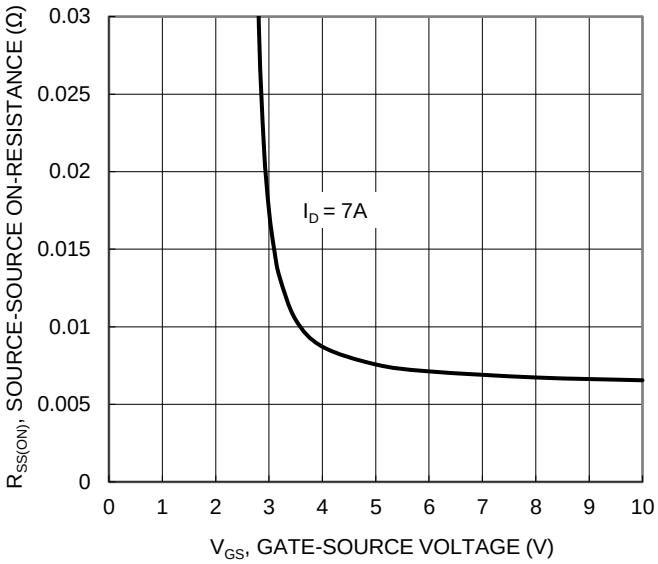


Figure 4. Typical Transfer Characteristic

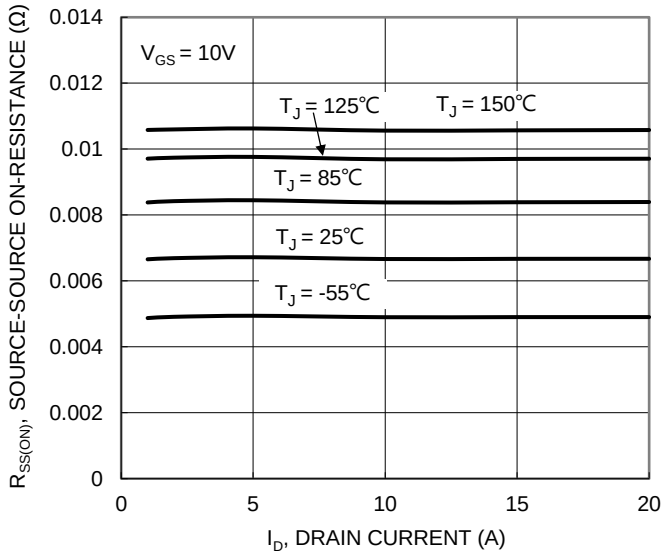


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

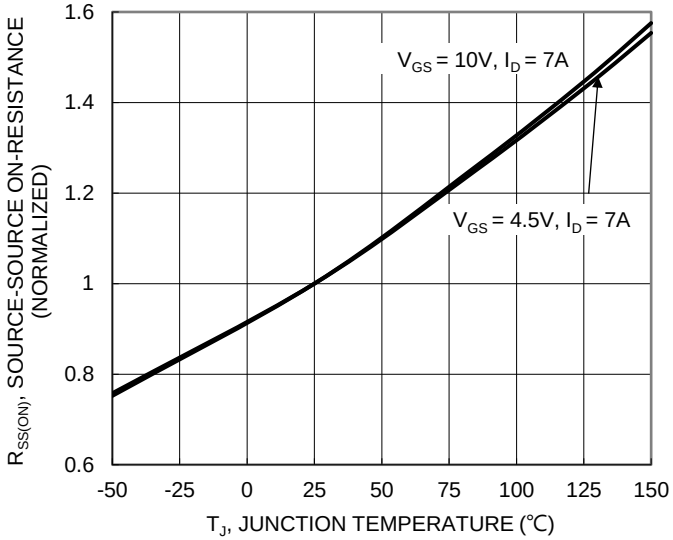


Figure 6. On-Resistance Variation with Junction Temperature

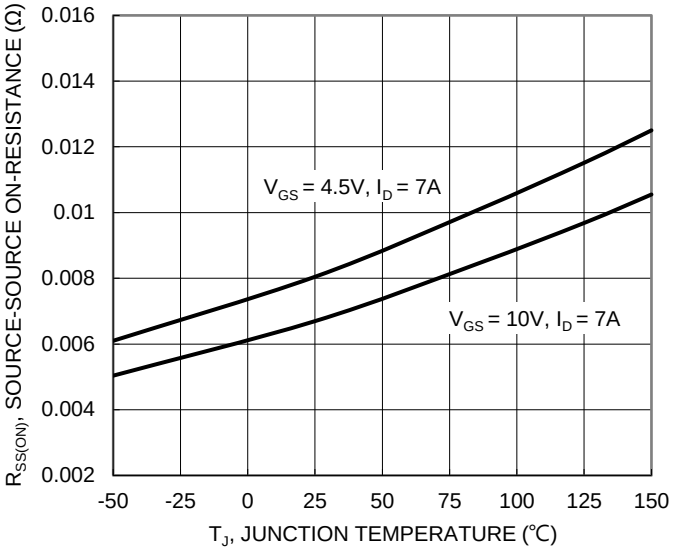


Figure 7. On-Resistance Variation with Junction Temperature

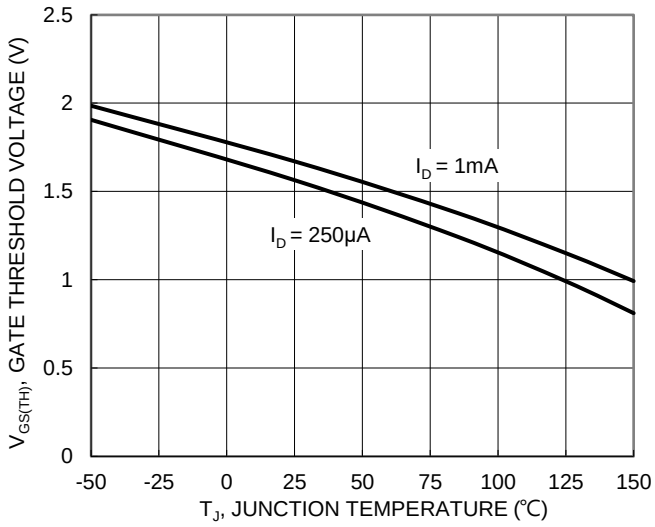


Figure 8. Gate Threshold Variation vs. Junction Temperature

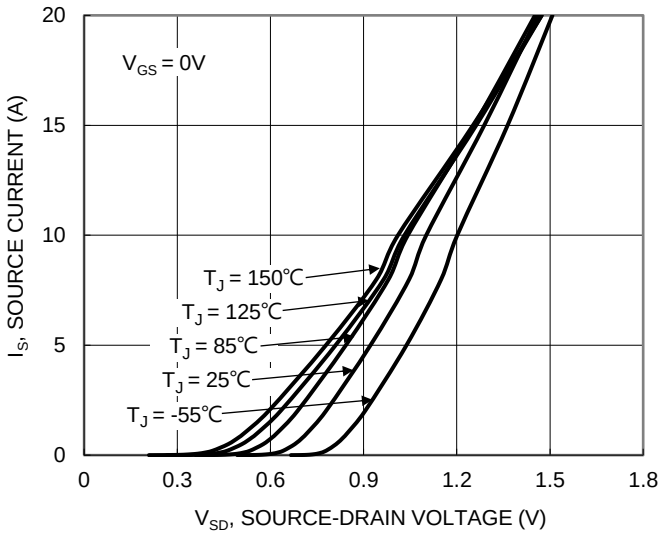


Figure 9. Diode Forward Voltage vs. Current

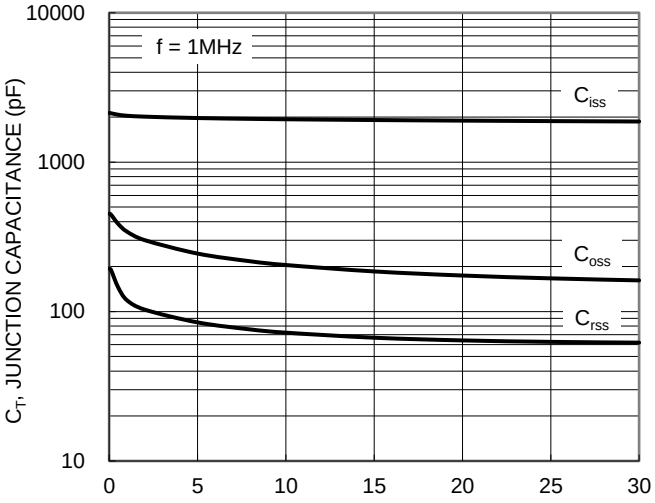


Figure 10. Typical Junction Capacitance

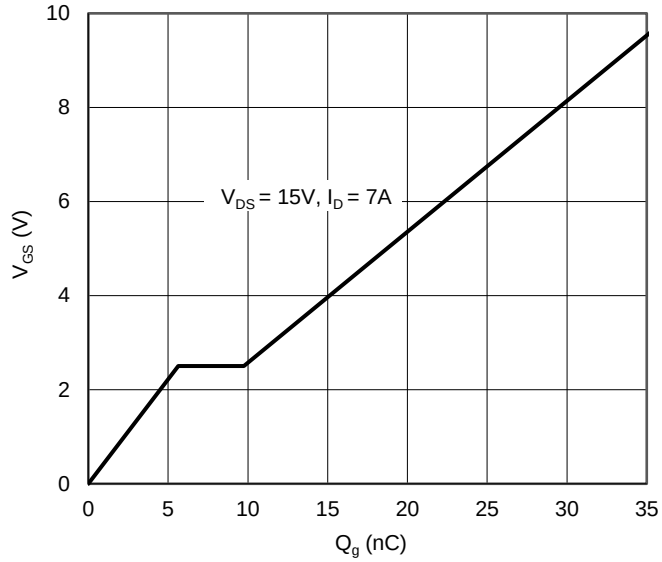


Figure 11. Gate Charge

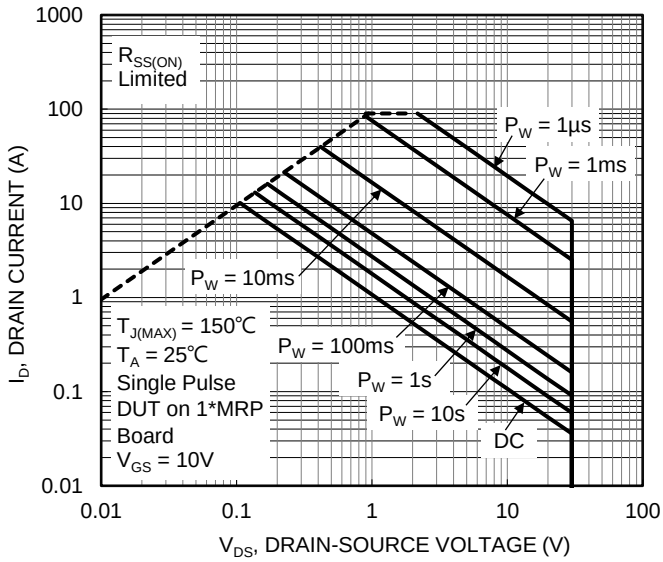


Figure 12. SOA, Safe Operation Area

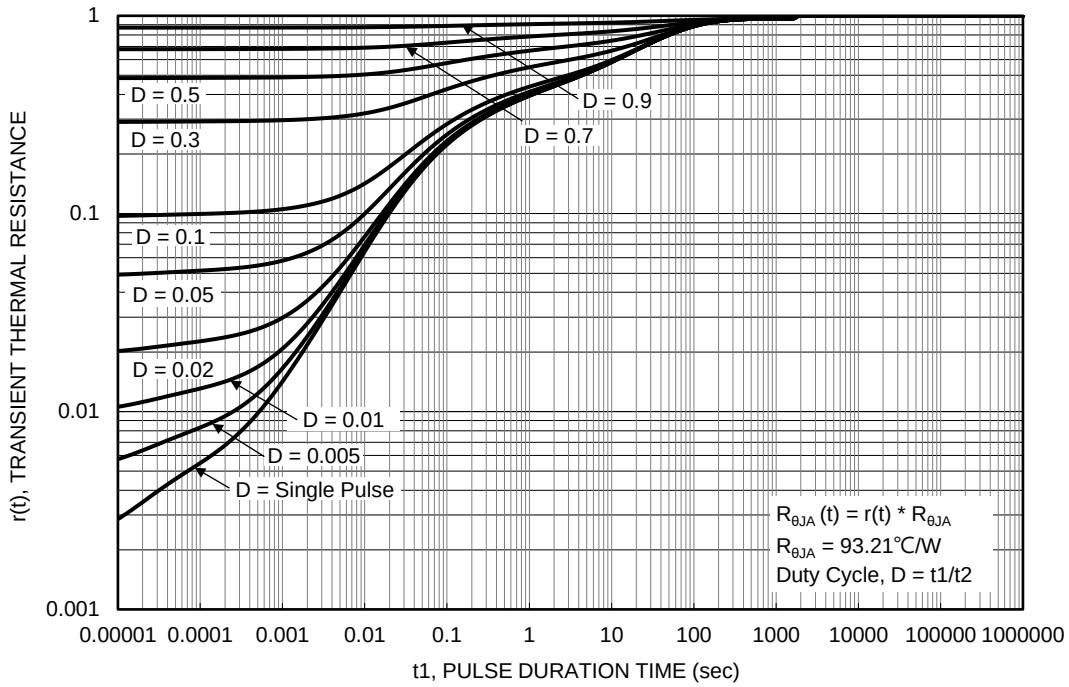
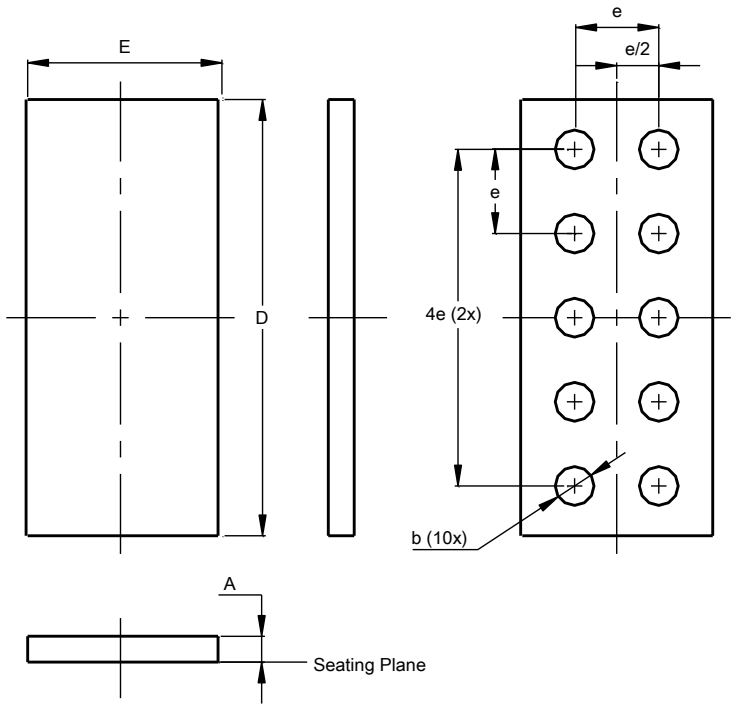


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

X4-DSN3415-10

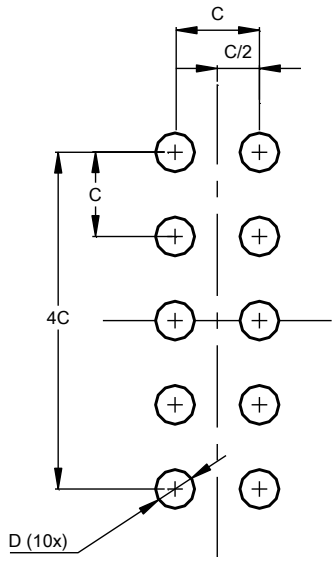


X4-DSN3415-10			
Dim	**Min**	**Max**	**Typ**
A	0.18	0.22	0.20
b	0.27	0.33	0.30
D	3.32	3.42	3.37
E	1.42	1.52	1.47
e	--	--	0.65
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

X4-DSN3415-10



Dimensions	Value (in mm)
C	0.65
D	0.30

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