

## Product Summary

V <sub>DSS</sub>	R <sub>DS(ON)</sub> Max	I <sub>D</sub> Max T <sub>A</sub> = +25°C
-8V	9.9mΩ @ V <sub>GS</sub> = -4.5V	-10A

## Description

This new generation Lateral MOSFET (LD-MOS) is designed to minimize on-state losses and switch ultra-fast, making it ideal for high-efficiency power transfer. It uses Chip-Scale Package (CSP) to increase power density by combining low thermal impedance with minimal R<sub>DS(ON)</sub> per footprint area.

## Applications

- Battery protections
- Battery managements
- Load switches

## Features

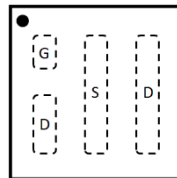
- LD-MOS Technology with the Lowest Figure of Merit:
  - R<sub>DS(ON)</sub> = 9.9mΩ to Minimize On-State Losses
  - Q<sub>g</sub> = 7.0nC for Ultra-Fast Switching
- V<sub>GS(TH)</sub> = -0.80V typ. for a Low Turn-On Potential
- CSP with Footprint 1.2mm × 1.2mm
- Height = 0.35mm for Low Profile
- ESD Protected Gate
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- Halogen and Antimony Free. "Green" Device (Note 3) For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](mailto:contact_us) or your local Diodes representative. <https://www.diodes.com/quality/product-definitions/>**

## Mechanical Data

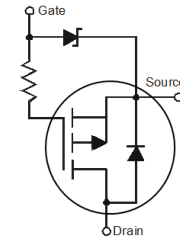
- Package: X2-DSN1212-4
- Terminal Connections: See Diagram Below
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Material: Finish – NiAu. Solderable per MIL-STD-202, Method 208@4
- Weight: 0.00092 grams (Approximate)



X2-DSN1212-4  
(Note 4)



Top-View  
Pin Configuration



Equivalent Circuit

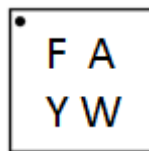
## Ordering Information (Note 5)

Part Number	Package	Packing	
		Qty.	Carrier
DMP1010UCA4-7	X2-DSN1212-4	3,000	Tape & Reel

- Notes:
- No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
  - See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  - Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  - Device with exposed silicon sidewall is non-isolated area.
  - For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

## Marking Information

X2-DSN1212-4



FA = Product Type Marking Code  
 YW = Date Code Marking  
 Y or  $\bar{Y}$  = Year (ex: 3 = 2023)  
 W or  $\bar{W}$  = Week (ex: a = Week 27; z Represents Week 52 and 53)

### Date Code Key

Year	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034
Code	3	4	5	6	7	8	9	0	1	2	3	4

Week	1-26	27-52	53
Code	A-Z	a-z	z

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V <sub>DSS</sub>	-8	V
Gate-Source Voltage	V <sub>GSS</sub>	-6	V
Continuous Drain Current (Note 6) V <sub>GS</sub> = -4.5V	I <sub>D</sub>	Steady State T <sub>A</sub> = +25°C	-6
		T <sub>A</sub> = +70°C	-4.8
Continuous Drain Current (Note 7) V <sub>GS</sub> = -4.5V	I <sub>D</sub>	Steady State T <sub>A</sub> = +25°C	-10
		T <sub>A</sub> = +70°C	-8
Pulsed Drain Current (Pulse Duration 10μs, Duty Cycle ≤1%)	I <sub>DM</sub>	-60	A

**Thermal Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 6)	P <sub>D</sub>	0.63	W
Total Power Dissipation (Note 7)	P <sub>D</sub>	1.75	W
Thermal Resistance, Junction to Ambient (Note 6)	R <sub>θJA</sub>	200.0	°C/W
Thermal Resistance, Junction to Ambient (Note 7)	R <sub>θJA</sub>	71.7	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 8)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-8	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA
Zero Gate Voltage Drain Current @T <sub>C</sub> = +25°C	I <sub>DSS</sub>	—	—	-1	μA	V <sub>DS</sub> = -6.4V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	-100	nA	V <sub>GS</sub> = -6.0V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 8)</b>						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	-0.4	-0.80	-1.05	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA
Static Drain-Source On-Resistance	R <sub>D(S(ON))</sub>	—	8.4	9.9	mΩ	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -1A
			11.6	15		V <sub>GS</sub> = -2.5V, I <sub>D</sub> = -1A
			17.2	40		V <sub>GS</sub> = -1.8V, I <sub>D</sub> = -1A
			30	—		V <sub>GS</sub> = -1.5V, I <sub>D</sub> = -0.2A
Diode Forward Voltage (Note 7)	V <sub>SD</sub>	—	-0.66	-1	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = -1A
<b>DYNAMIC CHARACTERISTICS (Note 9)</b>						
Input Capacitance	C <sub>iss</sub>	—	699	—	pF	V <sub>DS</sub> = -4V, V <sub>GS</sub> = 0V, f = 1.0MHz
Output Capacitance	C <sub>oss</sub>	—	463	—	pF	
Reverse Transfer Capacitance	C <sub>rss</sub>	—	109	—	pF	
Series Gate Resistance	R <sub>G</sub>	—	21.5	—	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1.0MHz
Total Gate Charge (-4.5V)	Q <sub>g</sub>	—	7.0	—	nC	V <sub>DS</sub> = -4.0V, I <sub>D</sub> = -1A
Gate-Source Charge	Q <sub>gs</sub>	—	1.0	—	nC	
Gate-Drain Charge	Q <sub>gd</sub>	—	1.0	—	nC	
Gate Charge at V <sub>TH</sub>	Q <sub>g(th)</sub>	—	0.7	—	nC	
Output Charge	Q <sub>g(OSS)</sub>	—	2.2	—	nC	V <sub>DS</sub> = -4.0V, V <sub>GS</sub> = 0V
Turn-On Delay Time	t <sub>D(ON)</sub>	—	17.5	—	ns	V <sub>DS</sub> = -4V, V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -1A, R <sub>G</sub> = 0Ω
Turn-On Rise Time	t <sub>R</sub>	—	4.6	—	ns	
Turn-Off Delay Time	t <sub>D(OFF)</sub>	—	46.0	—	ns	
Turn-Off Fall Time	t <sub>F</sub>	—	17.5	—	ns	
Reverse Recovery Charge	Q <sub>RR</sub>	—	5.7	—	nC	V <sub>DS</sub> = -4V, I <sub>F</sub> = -1A, di/dt = 200A/μs
Reverse Recovery Time	t <sub>RR</sub>	—	17.6	—	ns	

- Notes:
6. Device mounted on FR-4 PCB with minimum recommended pad layout.
  7. Device mounted on FR-4 material with 1-inch<sup>2</sup> (6.45cm<sup>2</sup>), 2oz (0.071mm thick) Cu.
  8. Short duration pulse test used to minimize self-heating effect.
  9. Guaranteed by design. Not subject to production testing.

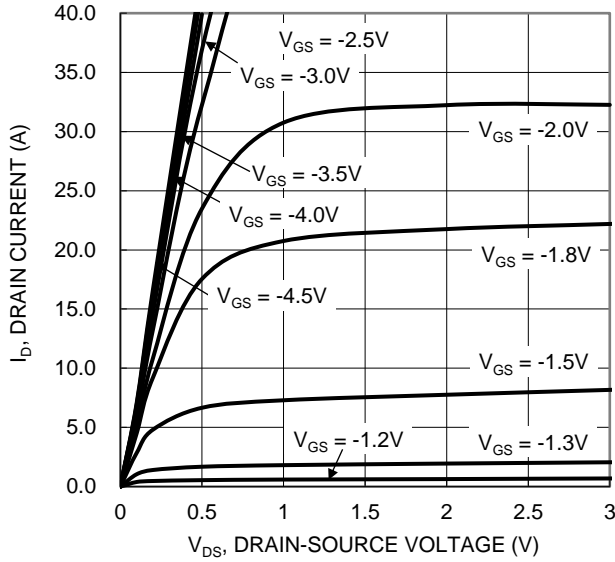


Figure 1. Typical Output Characteristic

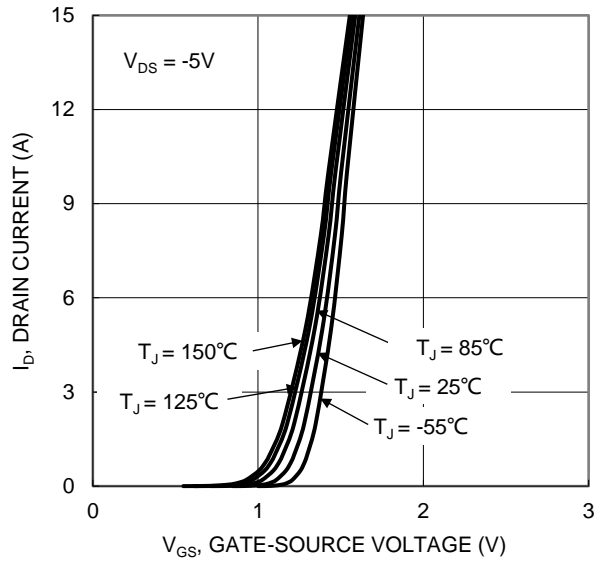


Figure 2. Typical Transfer Characteristic

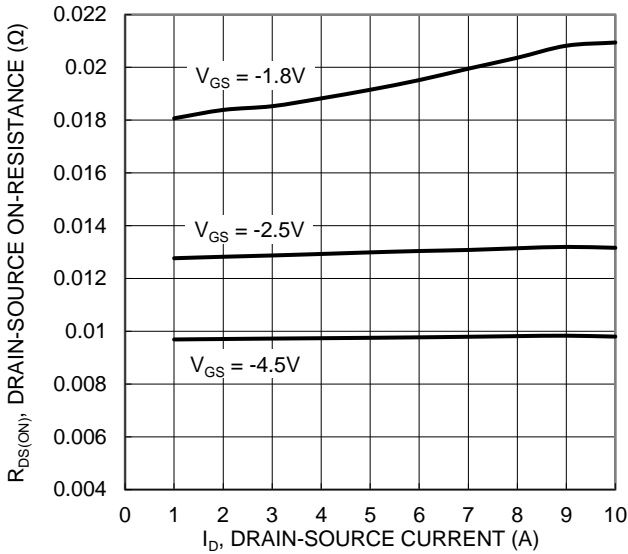


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

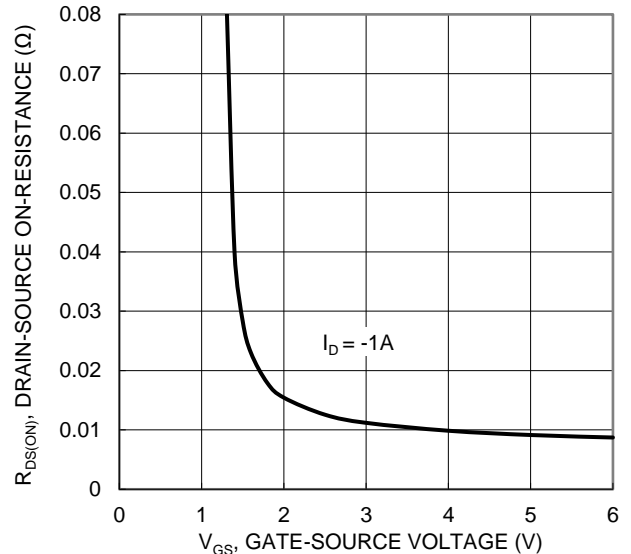


Figure 4. Typical Transfer Characteristic

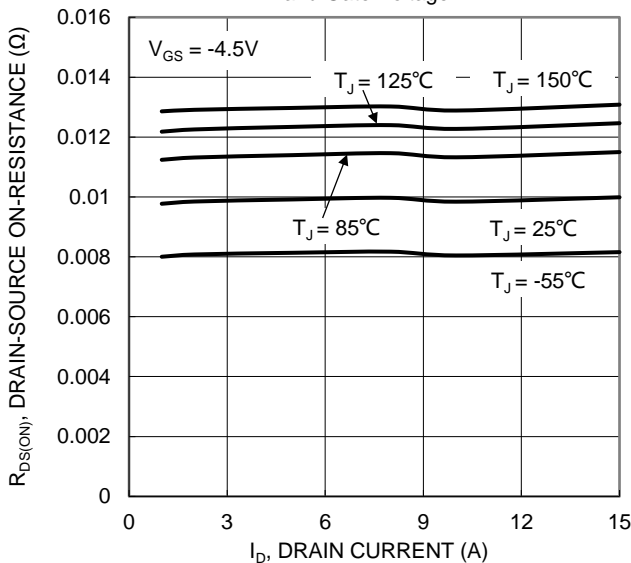


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

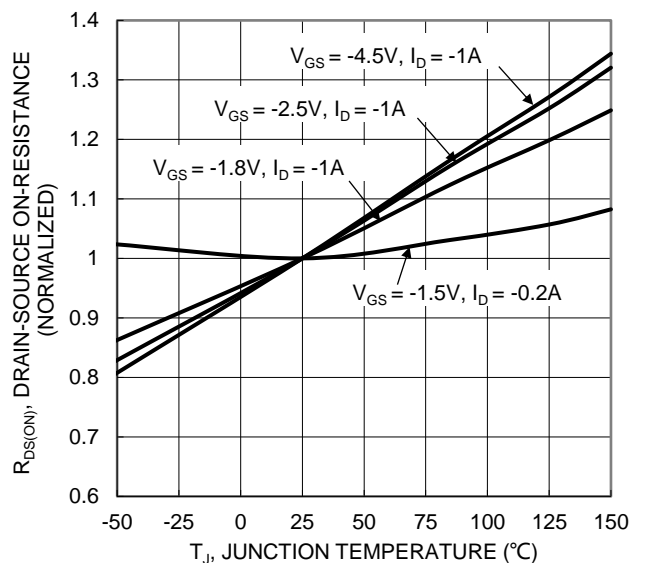


Figure 6. On-Resistance Variation with Junction Temperature

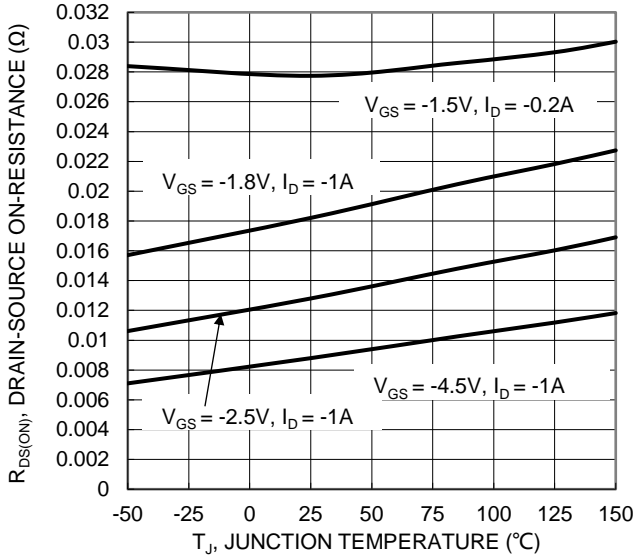


Figure 7. On-Resistance Variation with Junction Temperature

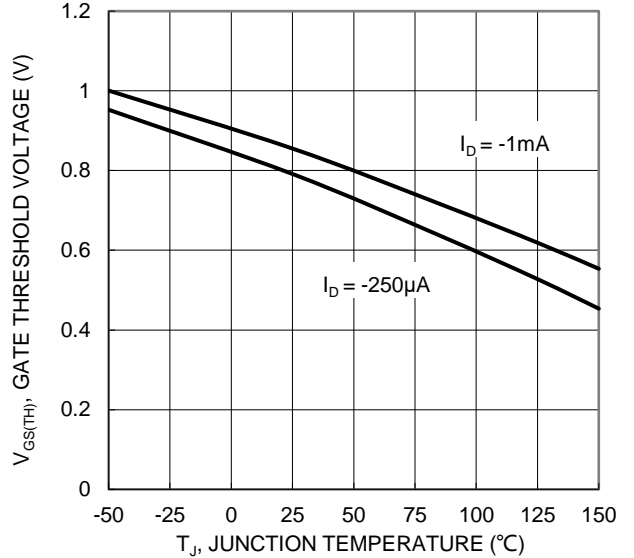


Figure 8. Gate Threshold Variation vs. Junction Temperature

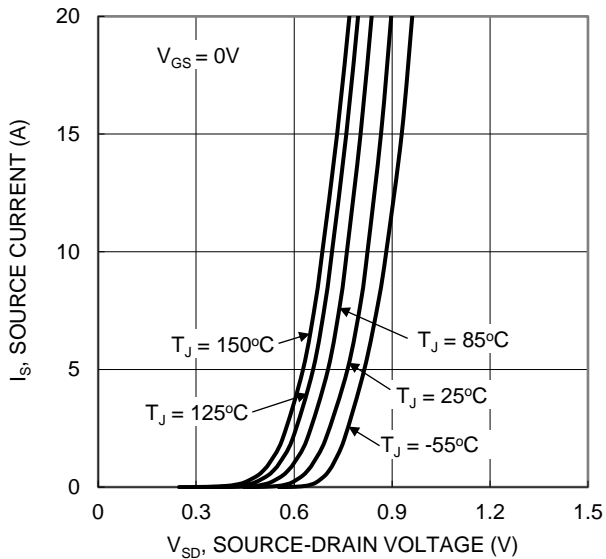


Figure 9. Diode Forward Voltage vs. Current

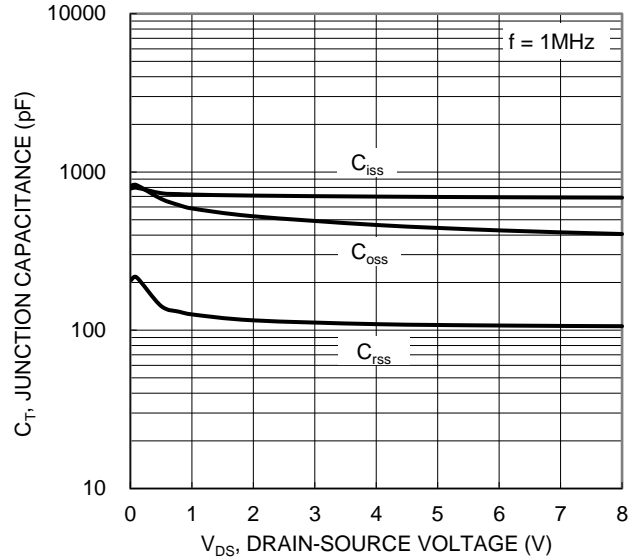


Figure 10. Typical Junction Capacitance

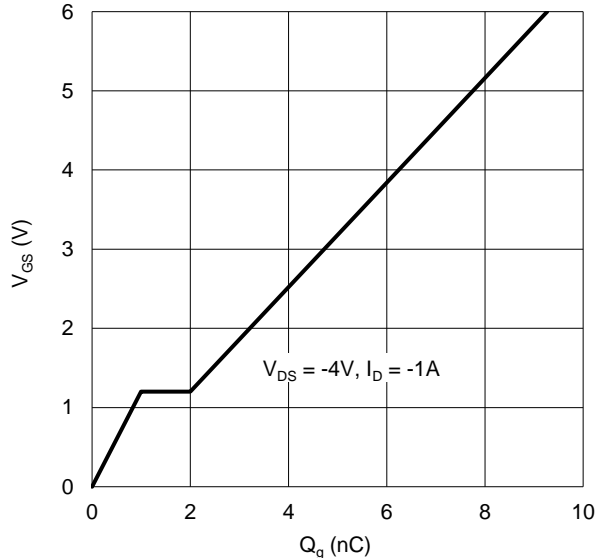


Figure 11. Gate Charge

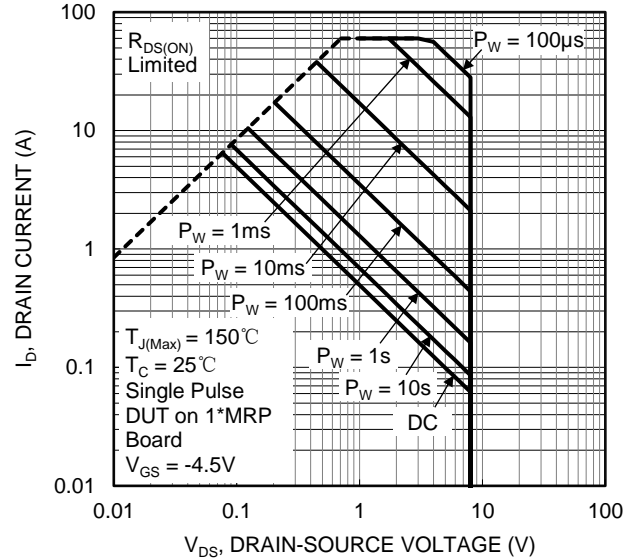


Figure 12. SOA, Safe Operation Area

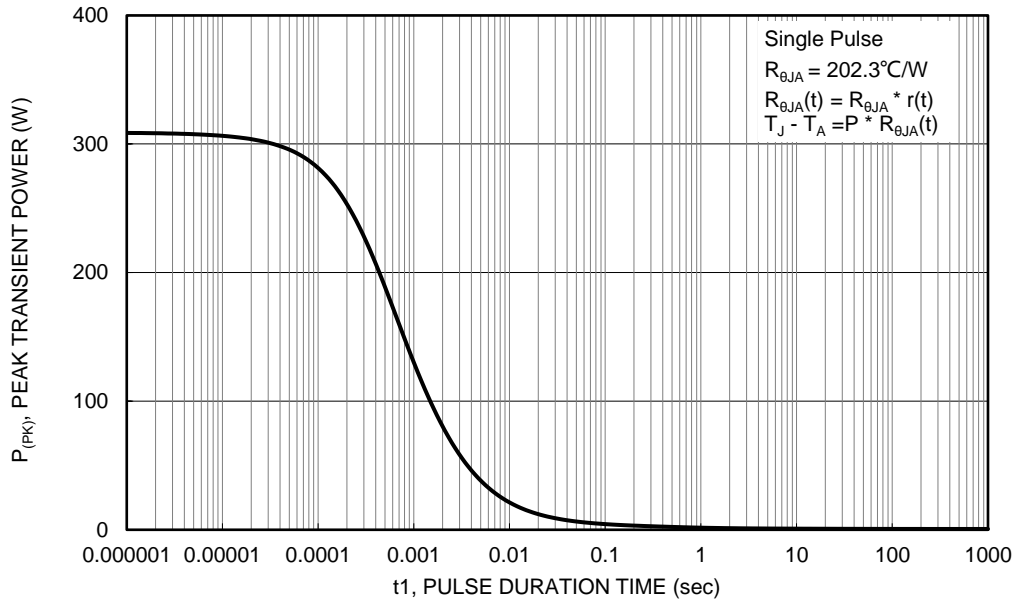


Figure 13. Single Pulse Maximum Power Dissipation

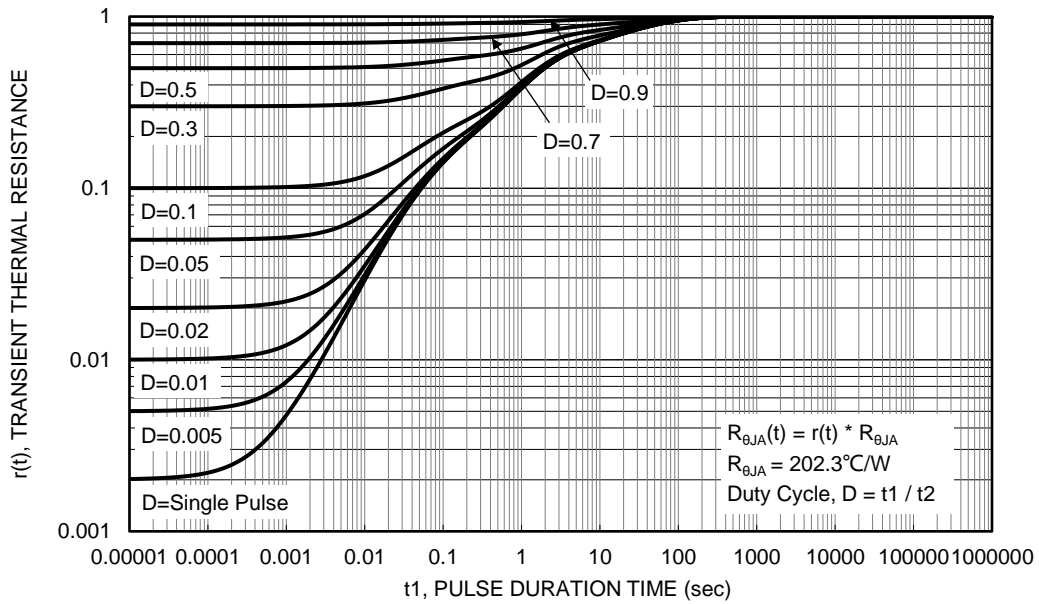
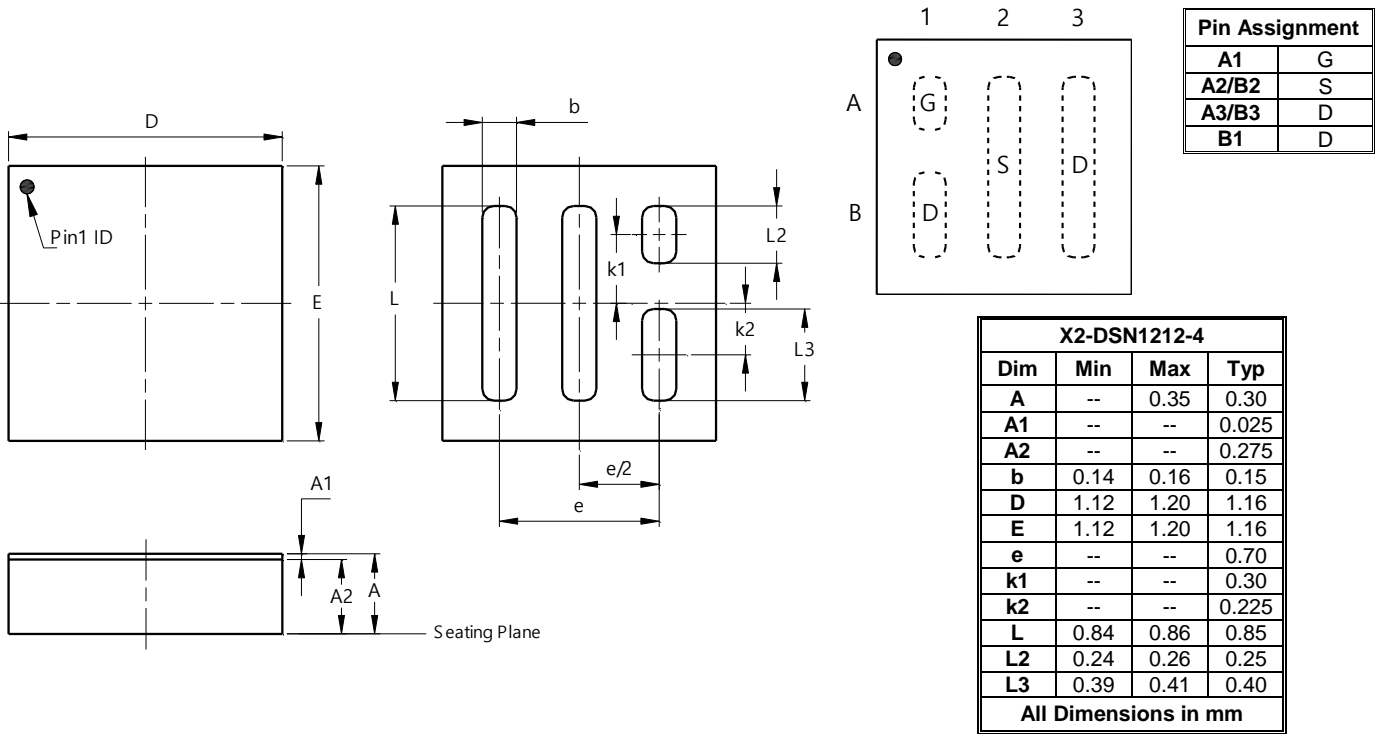


Figure 14. Transient Thermal Resistance

**Package Outline Dimensions**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

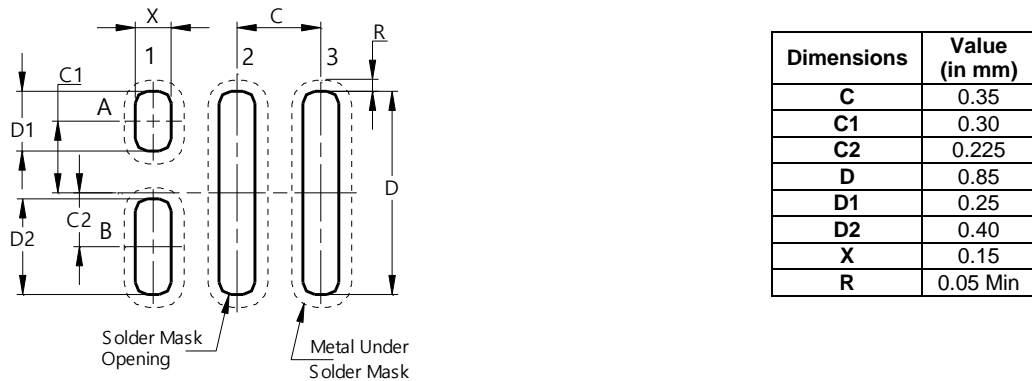
**X2-DSN1212-4**



**Suggested Pad Layout**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**X2-DSN1212-4**



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