Product Summary

BV_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX T_A = +25°C
-20V	45mΩ @ V_{GS} = -4.5V	-4.2A
	62mΩ @ V_{GS} = -2.5V	-3.4A

Description and Applications

This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) making it ideal for high efficiency power management applications.

- Battery Management
- Load Switch
- Battery Protection

Features and Benefits

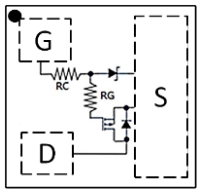
- Low Q_g & Q_{gd}
- Small Footprint
- Low Profile 0.35mm Height
- ESD Protected
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Mechanical Data

- Case: X2-DSN1010-3
- Terminal Connections: See Diagram Below
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish — NiPdAu or NiAu. Solderable per MIL-STD-202, Method 208 e4

ESD PROTECTED

X2-DSN1010-3



Top View
Equivalent Circuit

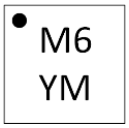
Ordering Information (Note 4)

Part Number	Case	Packaging
DMP2043UCA3-7	X2-DSN1010-3	5000/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen and Antimony free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information (Note 5)

Marking 1



M6 = Product Type Marking Code
YM = Date Code Marking
Y or $\overline{Y}$ = Year (ex: I = 2021)
M or $\overline{M}$ = Month (ex: 9 = September)

Date Code Key

Year	2017	…	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
Code	E	…	I	J	K	L	M	N	O	P	R	S

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Marking 2

M6 = Product Type Marking Code
YW = Date Code Marking
Y or $\overline{Y}$ = Year (ex: 1 = 2021)
W or $\overline{W}$ = Week (ex: a = Week 27; z Represents Week 52 and 53)

Date Code Key

Year	2017	…	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
Code	7	…	1	2	3	4	5	6	7	8	9	0

Week	1-26	27-52	53
Code	A-Z	a-z	z

Note: 5. The marking code changed to Marking 2 from week 6, 2021.

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	-20	V
Gate-Source Voltage		V_{GSS}	-20	V
Continuous Drain Current (Note 6) V_{GS} = -4.5V	T_A = +25°C T_A = +70°C	I_D	-4.2 -3.4	A
Continuous Drain Current (Note 6) V_{GS} = -2.5V	T_A = +25°C T_A = +70°C	I_D	-3.4 -2.7	A
Pulsed Drain Current (Note 7)		I_{DM}	-25	A
Continuous Gate Clamp Current		I_G	-5	mA

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 8)	P_D	0.65	W
Thermal Resistance, Junction to Ambient @T_A = +25°C (Note 8)	$R_{\theta JA}$	193.5	°C/W
Power Dissipation (Note 6)	P_D	1.3	W
Thermal Resistance, Junction to Ambient @T_A = +25°C (Note 6)	$R_{\theta JA}$	98.5	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 9)						
Drain-Source Breakdown Voltage	BV_{DSS}	-20	—	—	V	V_{GS} = 0V, I_D = -250µA
Zero Gate Voltage Drain Current T_J = +25°C	I_{DSS}	—	—	-1	µA	V_{DS} = -10V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	-100	nA	V_{GS} = -6V, V_{DS} = 0V
ON CHARACTERISTICS (Note9)						
Gate Threshold Voltage	$V_{GS(TH)}$	-0.4	-0.8	-1.2	V	V_{DS} = V_{GS}, I_D = -250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	36	45	mΩ	V_{GS} = -4.5V, I_D = -1A
		—	47	62		V_{GS} = -2.5V, I_D = -1A
Diode Forward Voltage	V_{SD}	—	-0.7	-1	V	V_{GS} = 0V, I_S = -1A
Reverse Recovery Charge	Q_{RR}	—	3.3	—	nC	V_{DS} = -10V, I_F = -1A, di/dt = 200A/µs
Reverse Recovery Time	t_{RR}	—	10.2	—	ns	
DYNAMIC CHARACTERISTICS (Note 10)						
Input Capacitance	C_{iss}	—	327	425	pF	V_{DS} = -10V, V_{GS} = 0V, f = 10kHz
Output Capacitance	C_{oss}	—	174	226		
Reverse Transfer Capacitance	C_{rss}	—	13	17		
Series Gate Resistance	R_g	—	20	30	Ω	—
Series Clamp Resistance	R_C	—	14000	—		
Total Gate Charge	Q_g	—	1.46	1.90	nC	V_{DS} = -10V, V_{GS} = -4.5V, I_D = -1A
Gate-Source Charge	Q_{gs}	—	0.35	—		
Gate-Drain Charge	Q_{gd}	—	0.37	—		
Gate Charge at V_{TH}	$Q_{g(TH)}$	—	0.20	—		
Turn-On Delay Time	$t_{D(ON)}$	—	986	1479	ns	V_{DS} = -10V, V_{GS} = -2.5V, R_g = 10Ω, I_D = -1A
Turn-On Rise Time	t_R	—	1877	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	2120	3180		
Turn-Off Fall Time	t_F	—	2230	—		

Notes:
6. Device mounted on FR-4 material with 1inch^2 (6.45cm^2), 2oz. (0.071mm thick) Cu.
7. Repetitive rating, pulse width limited by junction temperature.
8. Device mounted on FR-4 PCB with minimum recommended pad layout, single sided.
9. Short duration pulse test used to minimize self-heating effect.
10. Guaranteed by design. Not subject to production testing.

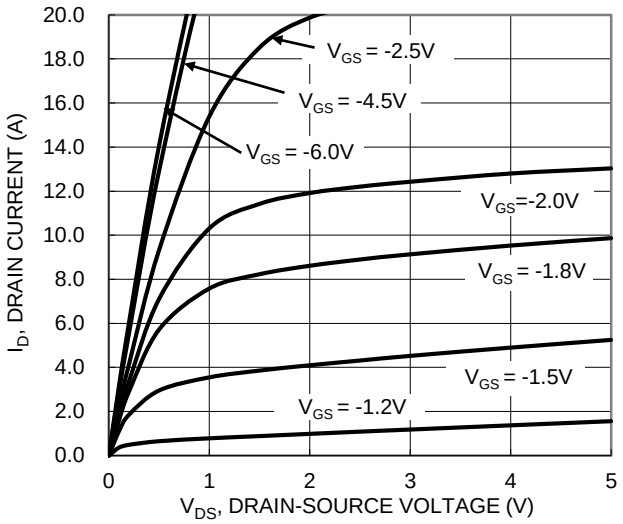


Figure 1. Typical Output Characteristic

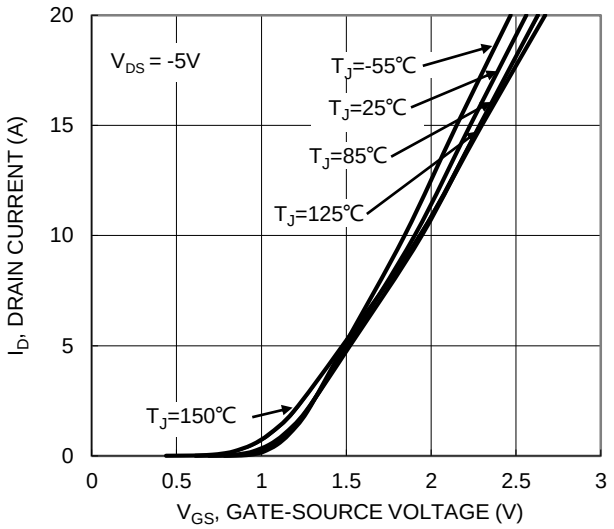


Figure 2. Typical Transfer Characteristic

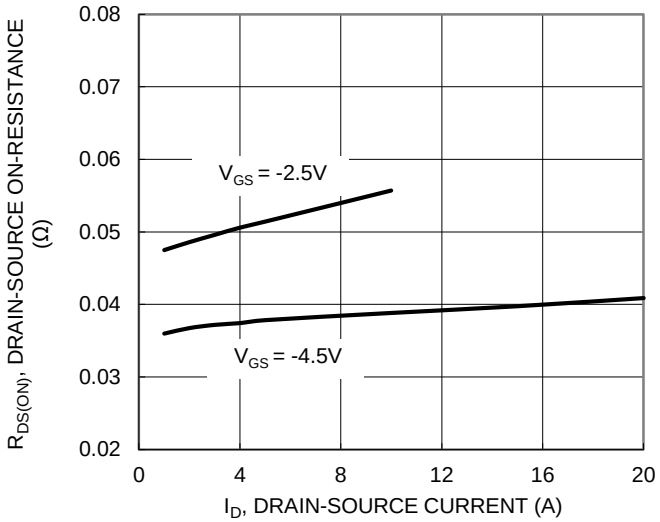


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

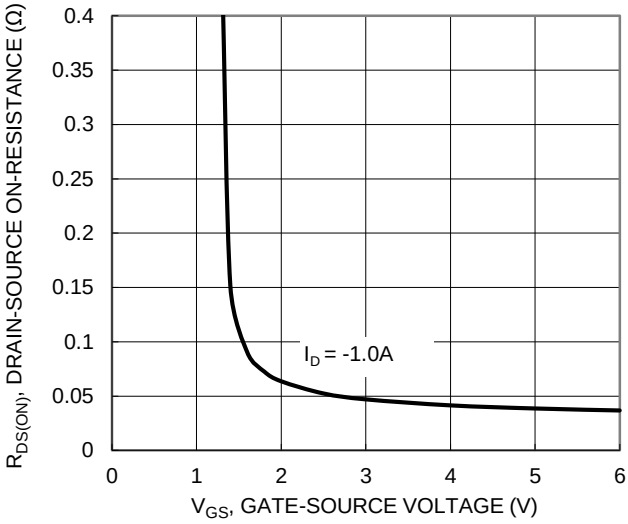


Figure 4. Typical Transfer Characteristic

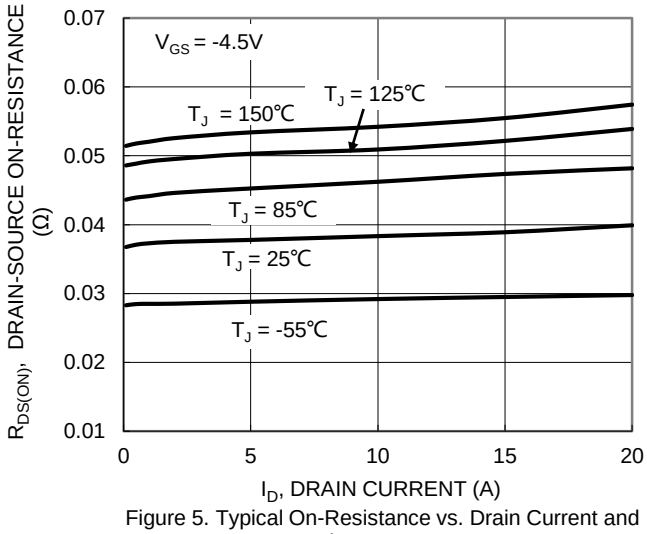


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

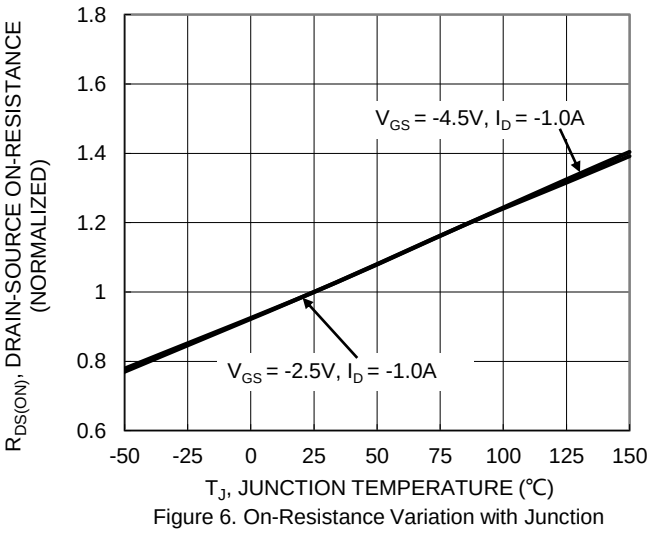


Figure 6. On-Resistance Variation with Junction Temperature

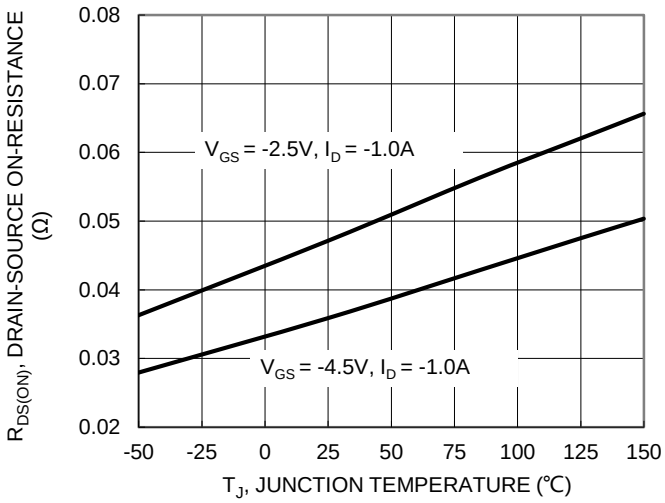


Figure 7. On-Resistance Variation with Junction Temperature

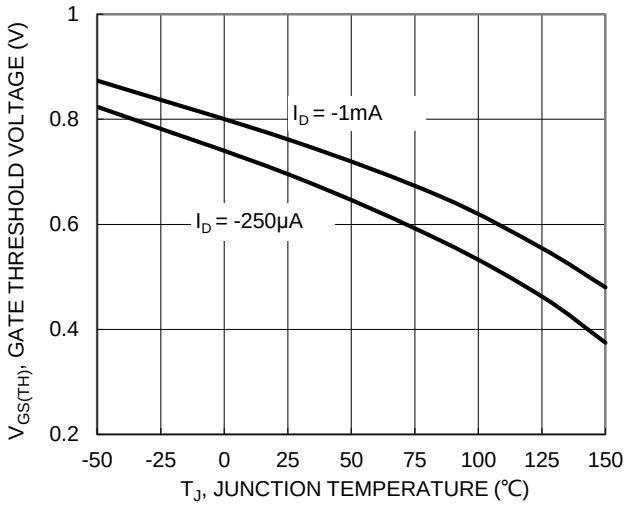


Figure 8. Gate Threshold Variation vs. Junction Temperature

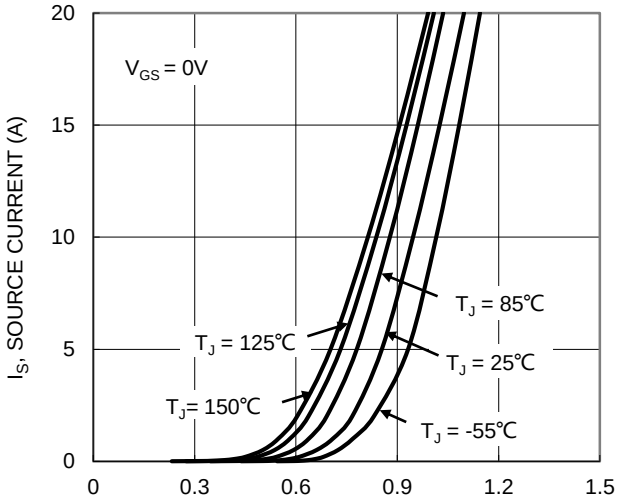


Figure 9. Diode Forward Voltage vs. Current

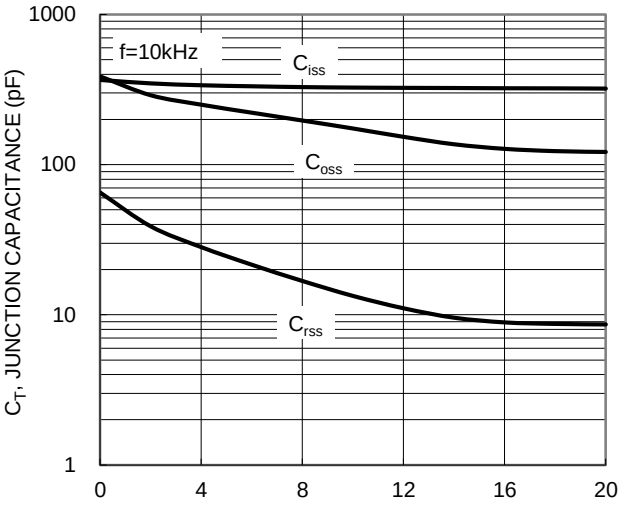


Figure 10. Typical Junction Capacitance

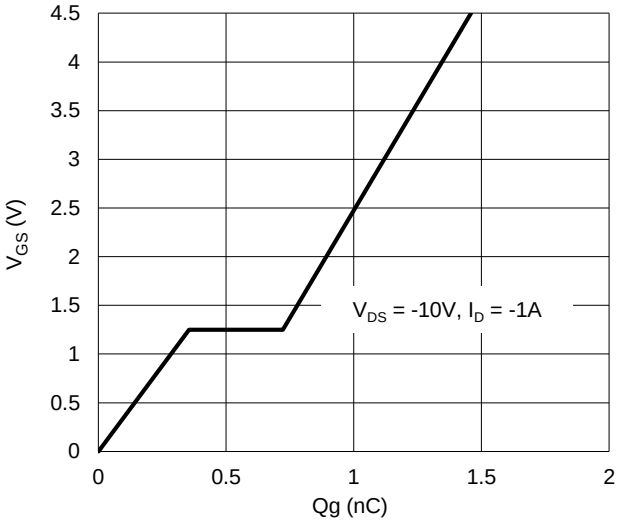


Figure 11. Gate Charge

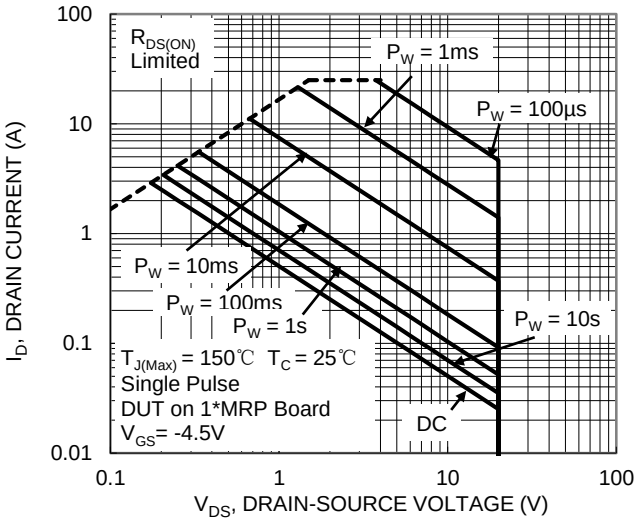


Figure 12. SOA, Safe Operation Area

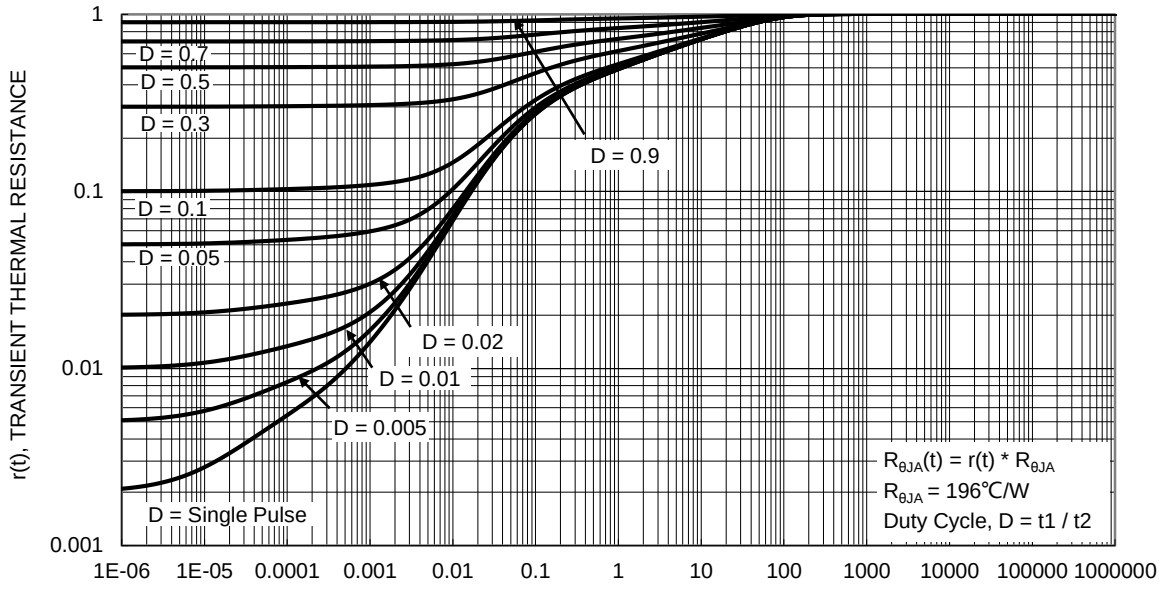
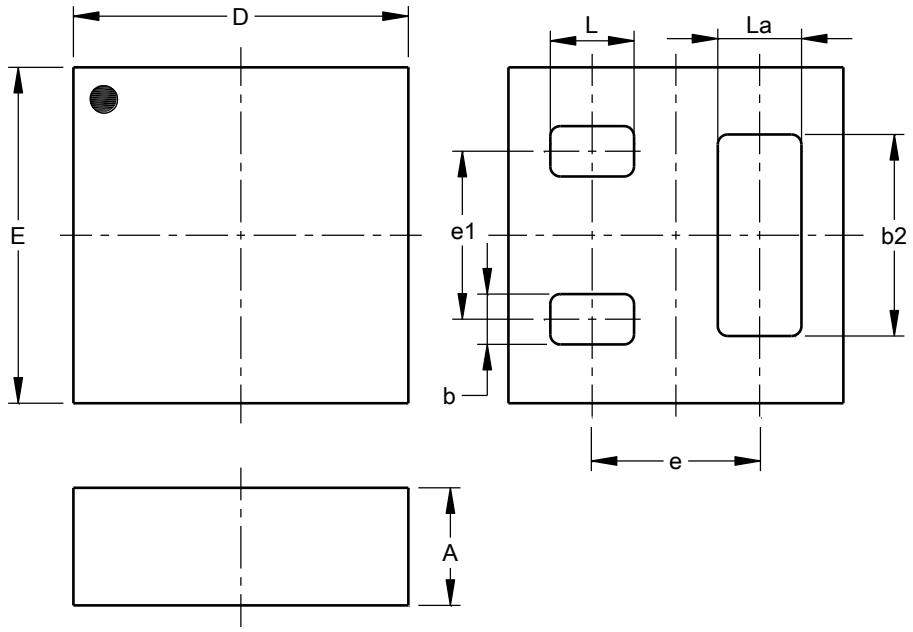


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

X2-DSN1010-3

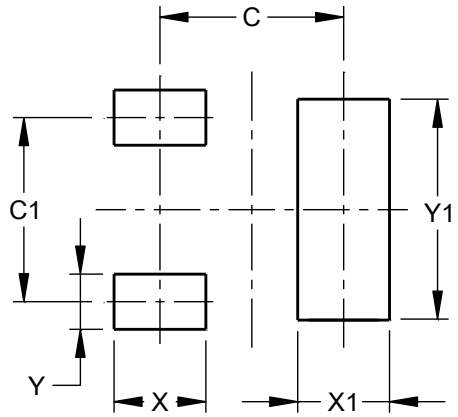


X2-DSN1010-3			
Dim	**Min**	**Max**	**Typ**
A	--	0.35	0.30
b	0.14	0.16	0.15
b2	0.64	0.66	0.65
D	0.92	1.00	0.96
E	0.92	1.00	0.96
e	-	-	0.50
e1	-	-	0.50
L	0.24	0.26	0.25
La	0.24	0.26	0.25
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

X2-DSN1010-3



Dimensions	Value (in mm)
C	0.50
C1	0.50
X	0.25
X1	0.25
Y	0.15
Y1	0.65

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