DUAL P-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BV_{D1D2}	$R_{D1D2(ON)}$ Typ.	I_{D1D2} T_A = +25°C
-20V	63mΩ @V_{GS} = -4.5V	-3.2A

Description

This new generation MOSFET is designed to minimize the on-state resistance ($R_{D1D2(ON)}$) yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

Applications

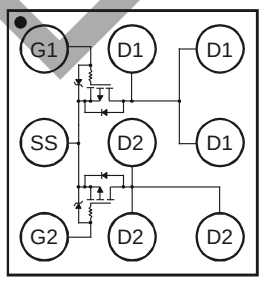
- Battery management
- Load switches
- Battery protections

Features and Benefits

- LD-MOS Technology with the Lowest Figure of Merit:
  - $R_{D1D2(ON)}$ = 63mΩ to Minimize On-State Losses
  - Q_g = 3.2nC for Ultra-Fast Switching
- $V_{GS(TH)}$ = -0.74V Typ. for a Low Turn-On Potential
- CSP with Footprint 1.5mm × 1.5mm
- Height = 0.62mm for Low Profile
- Gate ESD Protection <HBM Class 3A>
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Mechanical Data

- Package: U-WLB1515-9
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal: Finish - SnAgCu. Solderable per MIL-STD-202 Method 208 e1
- Terminal Connections: See Diagram Below
- Weight: 0.0018 grams (Approximate)



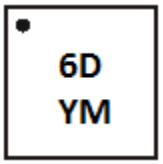
Top View

Ordering Information (Note 4)

Part Number	Package	Packing	
		Qty.	Carrier
DMP2101UCB9-7	U-WLB1515-9 (Type E)	3,000	Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



6D = Product Type Marking Code
YM = Date Code Marking
Y = Year (ex: J = 2022)
M = Month (ex: 9 = September)

Date Code Key

Year	2018	…	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031
Code	F	…	J	K	L	M	N	O	P	R	S	T

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-to-Drain Voltage			V_{D1D2}	-20	V
Gate-to-Source Voltage			V_{GS}	-6	V
Continuous Drain Current (Note 5) V_{GS} = -4.5V	Steady State	T_A = +25°C T_A = +70°C	I_{D1D2}	-2.2 -1.7	A
Continuous Drain Current (Note 6) V_{GS} = -4.5V	Steady State	T_A = +25°C T_A = +70°C	I_{D1D2}	-3.2 -2.5	A
Continuous Source Pin Current (Note 6)			I_S	-1.6	A
Pulsed Source Pin Current (Pulse Duration 10µs, Duty Cycle ≤ 1%)			I_{SM}	-25	A
Pulsed Drain Current (Pulse Duration 10µs, Duty Cycle ≤ 1%)			I_{DM}	-25	A

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P_D	0.74	W
Total Power Dissipation (Note 6)	P_D	1.56	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	170	°C/W
Thermal Resistance, Junction to Ambient (Note 6)	$R_{\theta JA}$	81	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Notes: 5. Device mounted on FR-4 PCB with minimum recommended pad layout.
6. Device mounted on FR-4 material with 1inch^2 (6.45cm^2), 2oz. (0.071mm thick) Cu.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-to-Drain Breakdown Voltage	BV_{D1D2}	-20	—	—	V	V_{GS} = 0V, I_{D1D2} = -250μA
Zero Gate Voltage Drain Current @T_C = +25°C	I_{DDS}	—	—	-1	μA	V_{D1D2} = -16V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	-100	nA	V_{GS} = -6V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	-0.4	-0.74	-0.9	V	V_{D1D2} = V_{GS}, I_{DS} = -250μA
Static Drain-to-Drain On-Resistance	$R_{D1D2(ON)}$	—	63	100	mΩ	V_{GS} = -4.5V, I_{D1D2} = -1A
		—	72	130		V_{GS} = -2.5V, I_{D1D2} = -1A
		—	87	175		V_{GS} = -1.8V, I_{D1D2} = -1A
DIODE CHARACTERISTICS						
Diode Forward Voltage (Note 6)	V_{SD}	—	-0.7	-1	V	V_{GS} = 0V, I_{D1D2} = -1A
Reverse Recovery Charge	Q_{RR}	—	4.1	—	nC	V_{D1D2} = -9.5V, I_F = -1A, di/dt = 200A/μs
Reverse Recovery Time	t_{RR}	—	10.5	—	ns	
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	392	588	pF	V_{D1D2} = -10V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	183	274	pF	
Reverse Transfer Capacitance	C_{rss}	—	8.4	12.6	pF	
Series Gate Resistance	R_g	—	5.2	10	Ω	V_{GS} = 0V, V_{D1D2} = 0V, f = 1.0MHz
Total Gate Charge (-4.5V)	Q_g	—	3.2	4.8	nC	V_{GS} = -4.5V, V_{D1D2} = -10V, I_{D1D2} = -1A
Gate-Source Charge	Q_{gs}	—	0.3	—	nC	
Gate-Drain Charge	Q_{gd}	—	0.6	—	nC	
Gate Charge at V_{th}	$Q_{g(th)}$	—	0.18	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	3.6	7	ns	V_{D1D2} = -10V, V_{GS} = -4.5V, I_{D1D2} = -1A, R_G = 30Ω
Turn-On Rise Time	t_R	—	5.3	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	40	80	ns	
Turn-Off Fall Time	t_F	—	20	—	ns	

Notes: 6. Device mounted on FR-4 material with 1inch^2 (6.45cm^2), 2oz. (0.071mm thick) Cu.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to production testing.

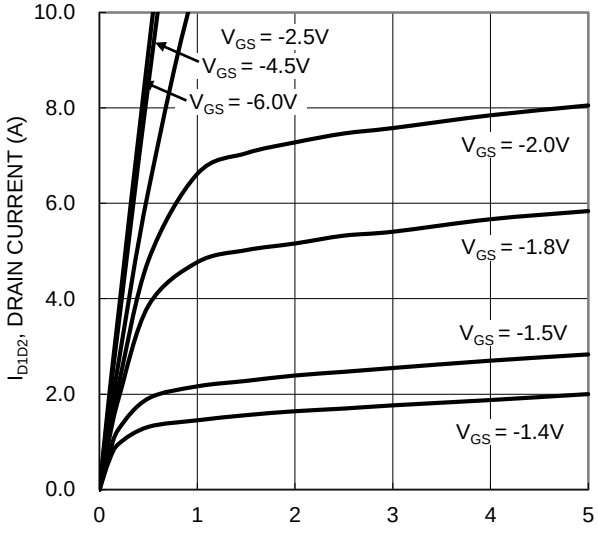


Figure 1. Typical Output Characteristic

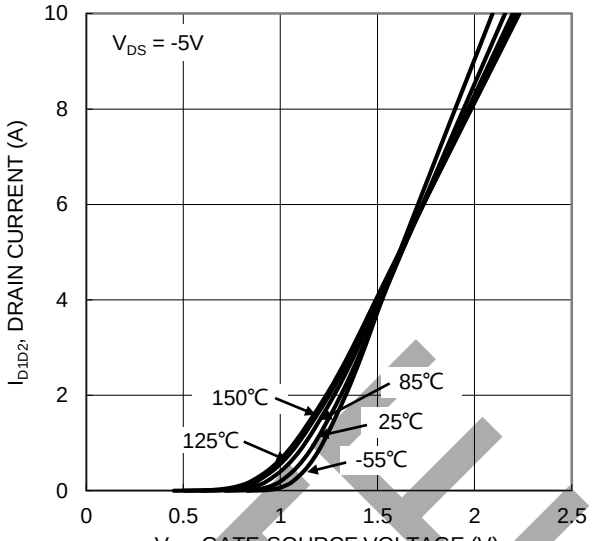


Figure 2. Typical Transfer Characteristic

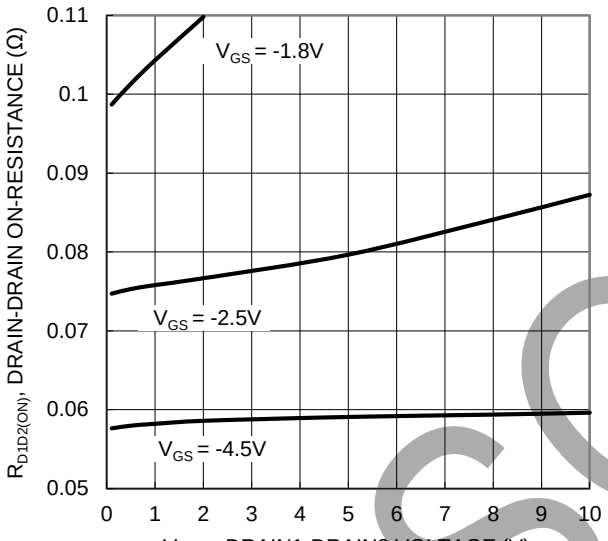


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

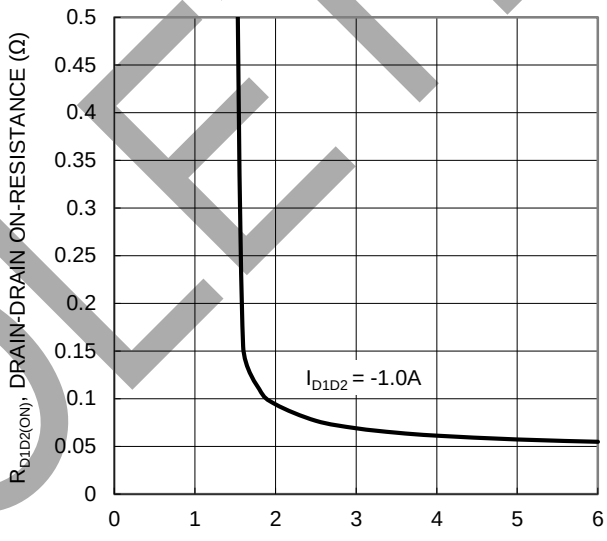


Figure 4. Typical Transfer Characteristic

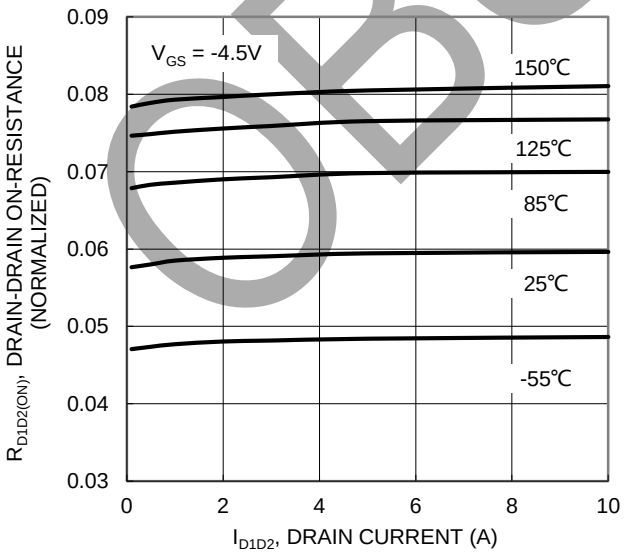


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

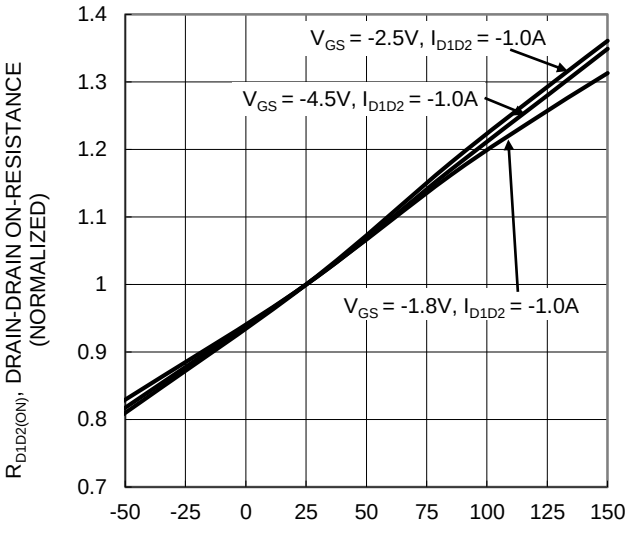


Figure 6. On-Resistance Variation with Junction Temperature

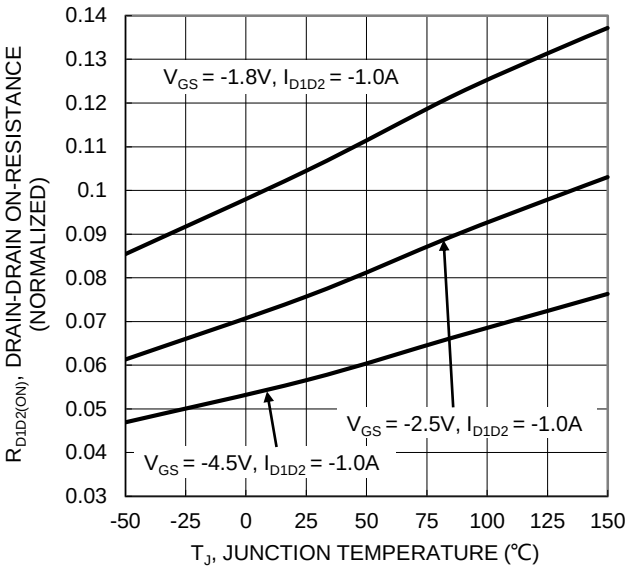


Figure 7. On-Resistance Variation with Junction Temperature

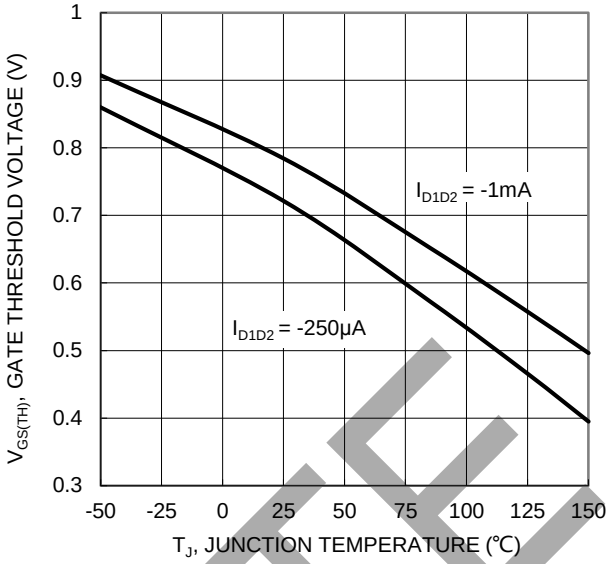


Figure 8. Gate Threshold Variation vs. Junction Temperature

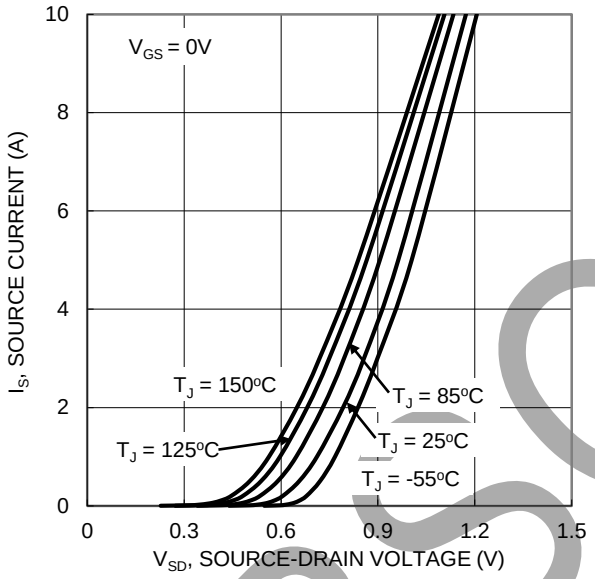


Figure 9. Diode Forward Voltage vs. Current

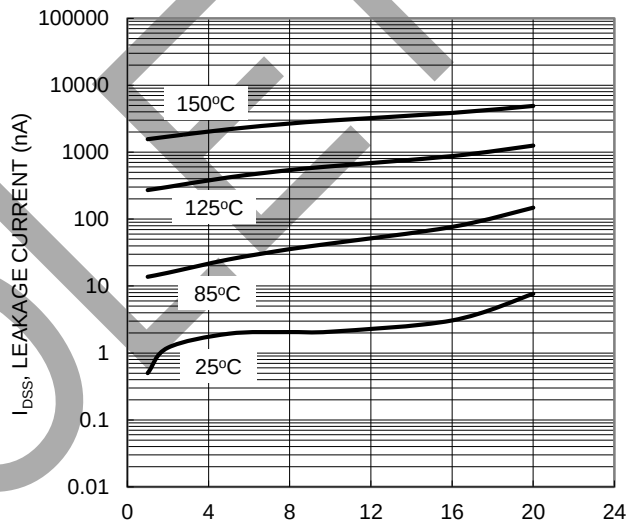


Figure 10. Typical Drain-Source Leakage Current vs. Voltage

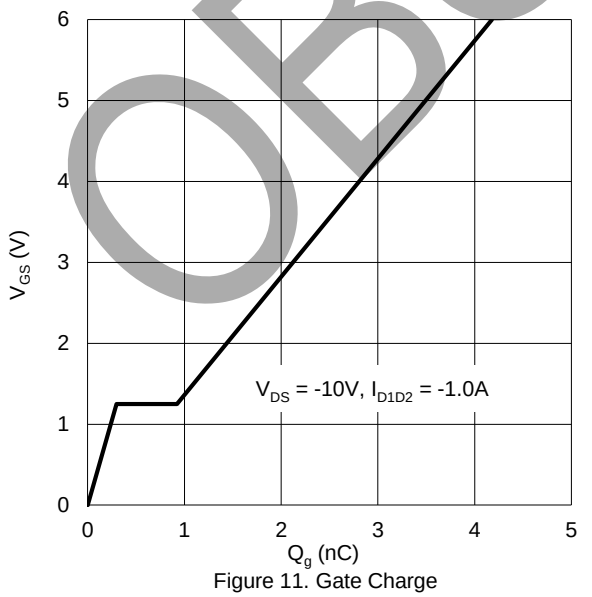


Figure 11. Gate Charge

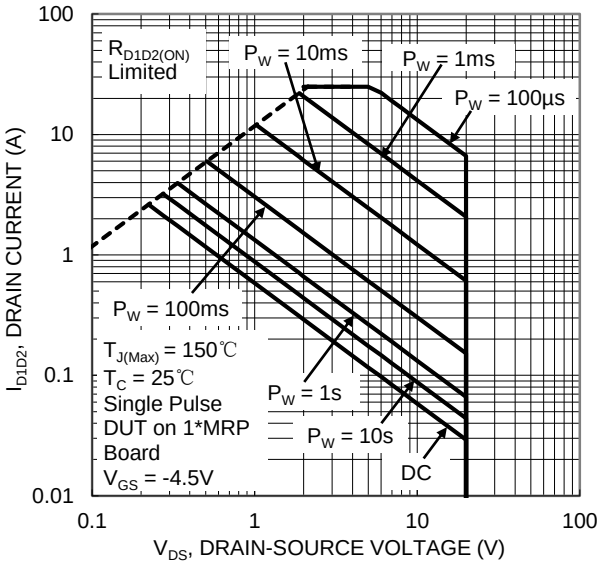


Figure 12. SOA, Safe Operation Area

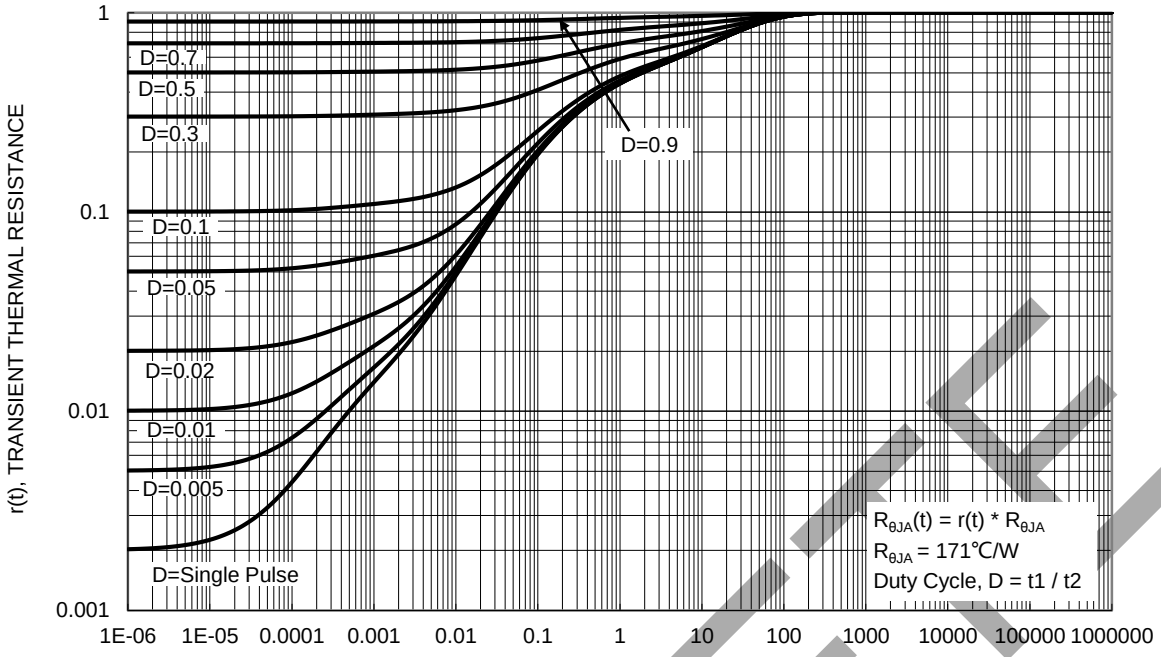
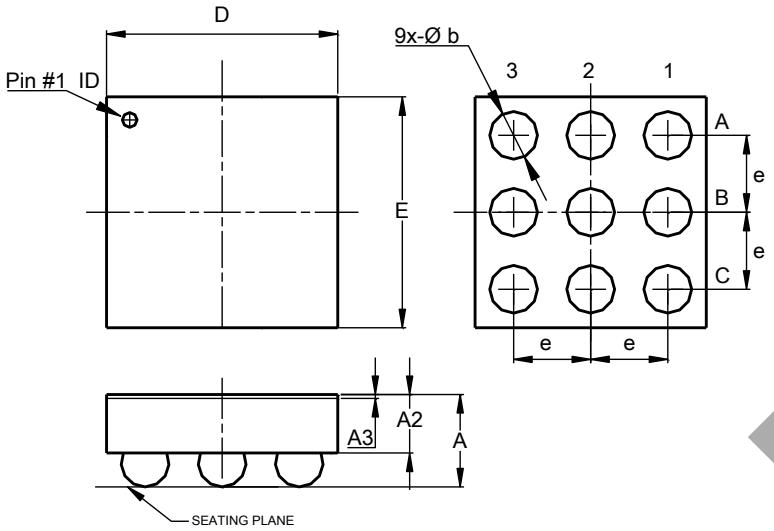


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-WLB1515-9 (Type E)

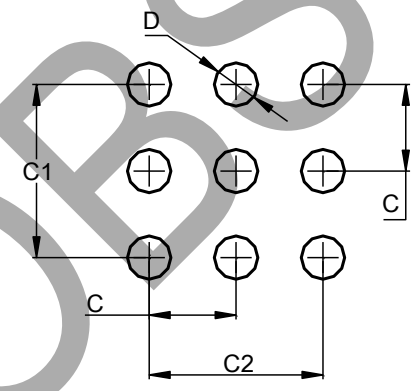


U-WLB1515-9 (Type E)			
Dim	**Min**	**Max**	**Typ**
A	--	0.62	--
A2	--	0.36	0.36
A3	0.020	0.030	0.025
b	0.27	0.37	0.32
D	1.47	1.51	1.49
E	1.47	1.51	1.49
e	--	--	0.50
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-WLB1515-9 (Type E)



Dimensions	Value (in mm)
C	0.50
C1	1.00
C2	1.00
D	0.25

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