NOT RECOMMENDED FOR NEW DESIGN USE DMP3007SPSQ



DMP3010LPSQ

P-CHANNEL ENHANCEMENT MODE MOSFET PowerDI5060-8

Product Summary

BV _{DSS}	R _{DS(ON)}	I _D T _A = +25°C
-30V	$7.5 \text{m}\Omega$ @ $V_{GS} = -10 \text{V}$	-36A
-307	10mΩ @ V _{GS} = -4.5V	-31A

Description

This new generation 30V P-Channel Enhancement Mode MOSFET is designed to minimize $R_{DS(ON)}$, yet maintain superior switching performance. This device is ideal for use in notebook battery power management and load switches.

Applications

- Notebook battery power management
- DC-DC converters
- Load switches

Features

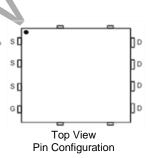
- Thermally Efficient Package Cooler Running Applications
- High Conversion Efficiency
- Low Rds(ON) Minimizes On-State Losses
- Low Input Capacitance
- Fast Switching Speed
- <1.1mm Package Profile Ideal for Thin Applications
- ESD HBM Protected up to 1kV
- Lead-Free Finish; RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- The DIODES™ DMP3010LPSQ is suitable for automotive applications requiring specific change control; this part is AEC-Q101 qualified, PPAP capable, and manufactured in IATF16949 certified facilities.

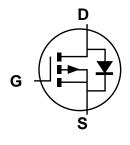
https://www.diodes.com/quality/product-definitions/

Mechanical Data

- Package: PowerDI[®]5060-8
- Package Material: Molded Plastic, "Green" Molding Compound.
 UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram Below
- Terminals: Finish 100% Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 (©3)
- Weight: 0.097 grams (Approximate)







Internal Schematic

Ordering Information (Note 4)

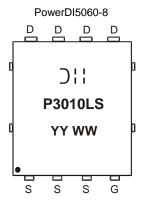
Part Number	Packago	Packing		
Part Number	Package	Qty.	Carrier	
DMP3010LPSQ-13	PowerDI5060-8	2,500	Tape & Reel	

Notes:

- 1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.



Marking Information



⊃H= Manufacturer's Marking P3010LS = Product Type Marking Code YYWW = Date Code Marking YY = Year (ex: 22 = 2022) WW = Week (01 to 53)

Maximum Ratings (@TA = +25°C, unless otherwise specified.)

Characteristic	C		Symbol	Value	Unit
Drain-Source Voltage			V _{DSS}	-30	V
Gate-Source Voltage			Vgss	±20	V
Continuous Drain Current (Note 5) V _{GS} = 10V	Steady State	$T_A = +25^{\circ}C$ $T_A = +70^{\circ}C$	<u>d</u>	-36 -29	Α
Continuous Drain Current (Note 5) V _{GS} = 4.5V	Steady State	T _A = +25°C T _A = +70°C	lD	-31 -25	А
Continuous Drain Current (Note 6) VGS = 10V	Steady State	$T_A = +25$ °C $T_A = +70$ °C	lo	-14.5 -11.5	А
Pulsed Drain Current (Notes 6 & 7)			Ірм	-100	Α
Avalanche Current (Notes 8 & 9)			las	-17.5	А
Avalanche Energy (Notes 8 & 9), L = 1mH			Eas	153	mJ

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 10)	P _D	1.26	W
Thermal Resistance, Junction to Ambient @T _A = +25°C (Note 10)	Reja	97	°C/W
Power Dissipation (Note 6)	PD	2.18	W
Thermal Resistance, Junction to Ambient @T _A = +25°C (Note 6)	Reja	55	°C/W
Power Dissipation (Note 5)	P _D	14.37	W
Thermal Resistance, Junction to Ambient @T _A = +25°C (Note 5)	Reja	8.7	°C/W
Power Dissipation (Notes 5 & 11)	PD	58.7	W
Thermal Resistance, Junction to Case @T _C = +25°C (Notes 5 & 11)	R ₀ JC	2.13	°C/W
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C

Notes:

- 5. Device mounted on FR-4 PCB with infinite heatsink.
 6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
 7. Repetitive rating, pulse width limited by junction temperature, 10 μ s pulse, duty cycle = 1%.
 8. μ s and μ s ratings are based on low frequency and duty cycles to keep μ s = +25°C.

- 9. Short duration pulse test used to minimize self-heating effect.
- 10. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
- 11. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



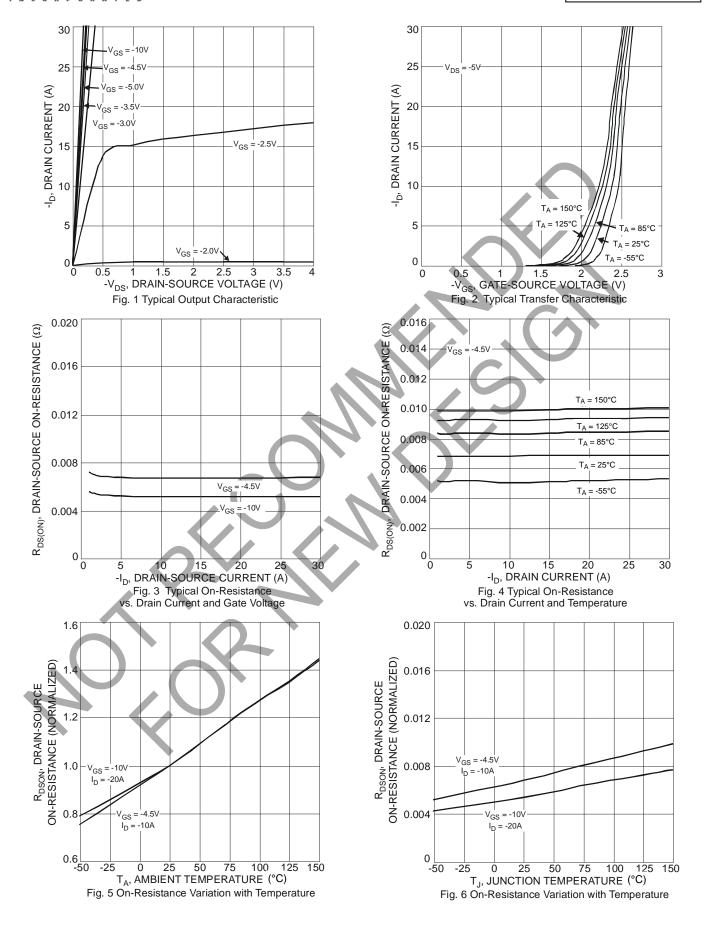
Electrical Characteristics ($@T_A = +25$ °C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 9)						
Drain-Source Breakdown Voltage	BV _{DSS}	-30	_	_	V	V _G S = 0V, I _D = -250µA
Zero Gate Voltage Drain Current	IDSS	_	_	-1	μA	V _{DS} = -30V, V _{GS} = 0V
Gate-Source Leakage	Igss	_	_	±100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 9)						
Gate Threshold Voltage	Vgs(th)	-1.1	-1.6	-2.1	٧	$V_{DS} = V_{GS}$, $I_D = -250\mu A$
Static Drain-Source On-Resistance	D-s/s/iii	_	5.7	7.5	mΩ	$V_{GS} = -10V, I_D = -10A$
Static Dialii-Source Off-Resistance	R _{DS(ON)}	_	7.2	10	11152	$V_{GS} = -4.5V$, $I_{D} = -10A$
Forward Transfer Admittance	Y _{fs}	_	30	1	S	$V_{DS} = -15V$, $I_{D} = -10A$
Diode Forward Voltage	VsD	_	-0.65	-1	V	Vgs = 0V, Is = -1A
DYNAMIC CHARACTERISTICS (Note 12)						
Input Capacitance	Ciss	_	6,234	1	pF	
Output Capacitance	Coss	_	1,500	+	рF	V _{DS} = 15V, V _{GS} = 0V f = 1MHz
Reverse Transfer Capacitance	Crss	_	774	_	pF	1 = 11/11/12
Gate Resistance	R_g	_	1.28		Ω	$V_{DS} = 0V$, $V_{GS} = 0V$, $f = 1MHz$
Total Gate Charge (VGS = -10V)	Qg	_	126.2		nC	$V_{DS} = -15V$, $I_{D} = -10A$
Total Gate Charge (Vgs = -4.5V)	Qg	_	59.2	1	nC	45// // 45//
Gate-Source Charge	Q_{gs}	_	16.1		nC	V _{DS} = -15V, V _{GS} = -4.5V In = -10A
Gate-Drain Charge	Q_{gd}	1	15.7	_	nC	16 = -10A
Turn-On Delay Time	t _{D(ON)}	4	11.4		ns	
Turn-On Rise Time	t _R	1/-	9.4	/-,	ns	V _{DS} = -15V, V _{GEN} = -10V
Turn-Off Delay Time	t _{D(OFF)}	-	260.7		ns	$R_G = 6\Omega$, $I_D = -1A$
Turn-Off Fall Time	tF	7	99.3	- /	ns	

Notes:

^{9.} Short duration pulse test used to minimize self-heating effect.12. Guaranteed by design. Not subject to product testing.







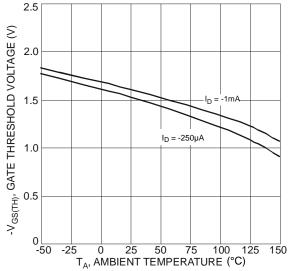
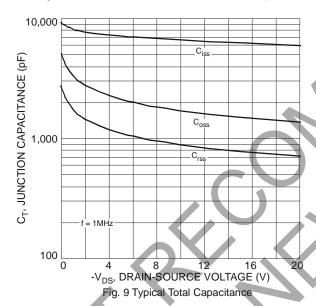


Fig. 7 Gate Threshold Variation vs. Ambient Temperature



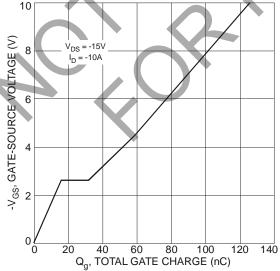
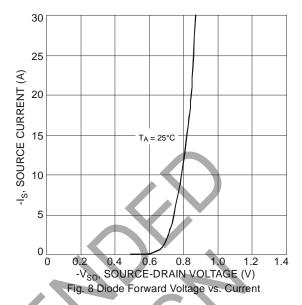


Fig. 11 Gate-Source Voltage vs. Total Gate Charge



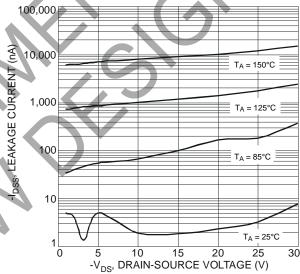
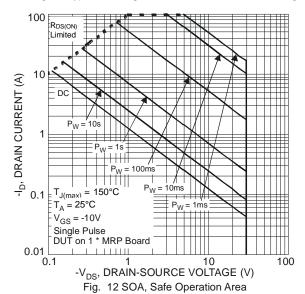
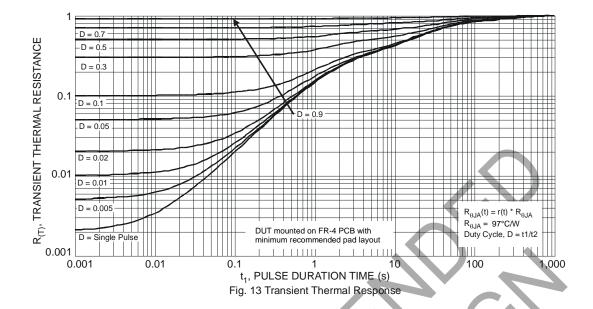


Fig. 10 Typical Leakage Current vs. Drain-Source Voltage





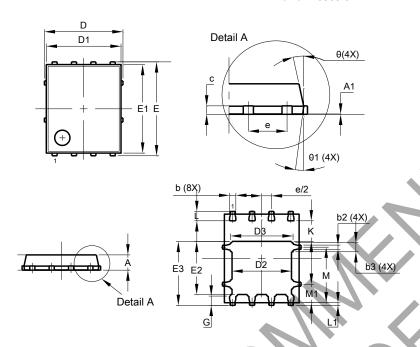




Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8

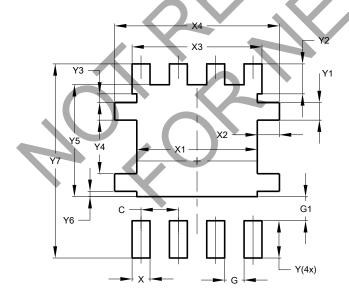


PowerDI5060-8				
Dim	Min	Max	Тур	
Α	0.90	1.10	1.00	
A1	0.00	0.05	-	
b	0.33	0.51	0.41	
b2	0.200	0.350	0.273	
b3	0.40	0.80	0.60	
C	0.230	0.330	0.277	
D		5.15 BSC	;	
D1	4.70	5.10	4.90	
D2	3.70	4.10	3.90	
D3	3.90	4.30	4.10	
E	•	5.15 BSC	;	
E1	5.60	6.00	5.80	
E2	3.28	3.68	3.48	
E3	3.99	4.39	4.19	
е		1.27 BSC		
G	0.51	0.71	0.61	
K	0.51	_	-	
L	0.51	0.71	0.61	
L1	0.100	0.200	0.175	
М	3.235	4.035	3.635	
M1	1.00	1.40	1.21	
Θ	10°	12°	11°	
Θ1	6°	8°	7°	
All Dimensions in mm				

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8



Dimensions	Value (in mm)			
С	1.270			
G	0.660			
G1	0.820			
Χ	0.610			
X1	4.100			
X2	0.755			
Х3	4.420			
X4	5.610			
Υ	1.270			
Y1	0.600			
Y2	1.020			
Y3	0.295			
Y4	1.825			
Y5	3.810			
Y6	0.180			
Y7	6.610			



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