Product Summary

BV_{DSS}	$R_{DS(ON)}$ Max	I_D T_A = +25°C
-30V	12mΩ @ V_{GS} = -10V	-10.7A
	25mΩ @ V_{GS} = -4.5V	-7.4A

Description

This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) yet maintain superior switching performance, making it ideal for high-efficiency power-management applications.

Applications

- Load switches
- Power-management functions
- DC-DC converters

Features and Benefits

- Low On-Resistance
- Low Input Capacitance
- Low Input/Output Leakage
- **ESD Protected Gate**
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

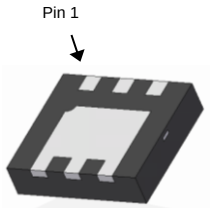
Mechanical Data

- Package: U-DFN2523-6
- Package Material: Molded Plastic, "Green" Molding Compound; UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish — NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e4
- Weight: 0.008 grams (Approximate)

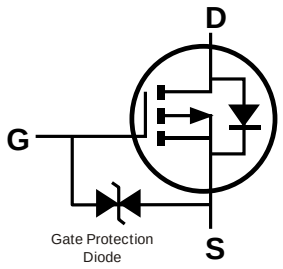
ESD PROTECTED

Pin 1, 2 = Source
Pin 3 = Gate
Pin 4, 5, 6 = Drain

U-DFN2523-6



Bottom View



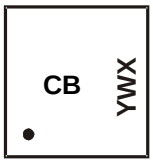
Equivalent Circuit

Ordering Information (Note 4)

Part Number	Package	Packing	
		Qty.	Carrier
DMP3011SFK-7	U-DFN2523-6	3,000	Tape & Reel
DMP3011SFK-13	U-DFN2523-6	10,000	Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



CB = Product Type Marking Code
YWX = Date Code Marking
Y = Year (ex: 3 = 2023)
W = Week (ex: a = Week 27; z Represents Week 52 and 53)
X = Internal Code (ex: B = Monday)

Date Code Key

Year	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034
Code	3	4	5	6	7	8	9	0	1	2	3	4

Week	1-26	27-52	53
Code	A-Z	a-z	z

Internal Code	Sun	Mon	Tue	Wed	Thu	Fri	Sat
Code	A	B	C	D	E	F	G

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	-30	V
Gate-Source Voltage			V_{GSS}	±25	V
Continuous Drain Current (Note 6) V_{GS} = -10V	Steady State	T_A = +25°C T_A = +70°C	I_D	-10.7 -8.6	A
Continuous Drain Current (Note 6) V_{GS} = -4.5V	Steady State	T_A = +25°C T_A = +70°C	I_D	-7.4 -5.9	A
Maximum Continuous Body Diode Forward Current (Note 6)			I_S	-3	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I_{DM}	-80	A
Avalanche Current (Note 7)			I_{AS}	-14	A
Avalanche Energy (Note 7)			E_{AS}	104	mJ

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)		P_D	1.04	W
Thermal Resistance, Junction to Ambient (Note 5)		$R_{\theta JA}$	121.03	°C/W
Total Power Dissipation (Note 6)		P_D	2.07	W
Thermal Resistance, Junction to Ambient (Note 6)		$R_{\theta JA}$	60.77	°C/W
Total Power Dissipation (Note 6)	T_C = +25°C	P_D	16.9	W
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	7.39	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	-30	—	—	V	V_{GS} = 0V, I_D = -250µA
Zero Gate Voltage Drain Current T_J = +25°C	I_{DSS}	—	—	-1	µA	V_{DS} = -24V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±10	µA	V_{GS} = ±25V, V_{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(th)}$	-1	—	-2.5	V	V_{DS} = V_{GS}, I_D = -250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	9.5	12	mΩ	V_{GS} = -10V, I_D = -9.5A
		—	15	25		V_{GS} = -4.5V, I_D = -6.9A
Diode Forward Voltage	V_{SD}	—	-0.7	-1.2	V	V_{GS} = 0V, I_S = -1A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	2380	—	pF	V_{DS} = -15V, V_{GS} = 0V, f = 1MHz
Output Capacitance	C_{oss}	—	341	—		
Reverse Transfer Capacitance	C_{rss}	—	296	—		
Gate Resistance	R_g	—	3	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = -5V)	Q_g	—	25	—	nC	V_{DS} = -15V, I_D = -11.5A
Total Gate Charge (V_{GS} = -10V)	Q_g	—	46	—		
Gate-Source Charge	Q_{gs}	—	6.8	—		
Gate-Drain Charge	Q_{gd}	—	13	—		
Turn-On Delay Time	$t_{D(on)}$	—	6	—	ns	V_{DD} = -15V, V_{GS} = -10V, R_G = 6Ω, I_D = -11.5A
Turn-On Rise Time	t_r	—	22	—		
Turn-Off Delay Time	$t_{D(off)}$	—	43	—		
Turn-Off Fall Time	t_f	—	33	—		
Reverse Recovery Time	t_{rr}	—	19	—	ns	I_S = -11.5A, dI/dt = 100A/µs
Reverse Recovery Charge	Q_{rr}	—	8.9	—	nC	

Notes:
5. Device mounted on FR-4 PCB, with minimum recommended pad layout.
6. Device mounted on minimum recommended pad layout test board, 10µs pulse duty cycle = 1%.
7. UIS in production with L = 1mH, T_J = +25°C.
8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to production testing.

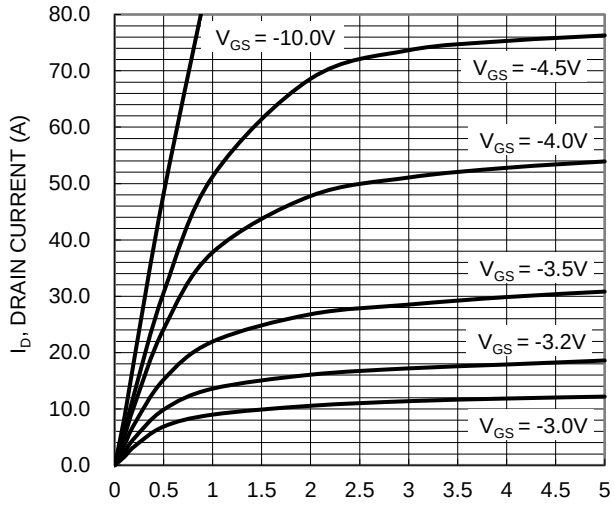


Figure 1. Typical Output Characteristic

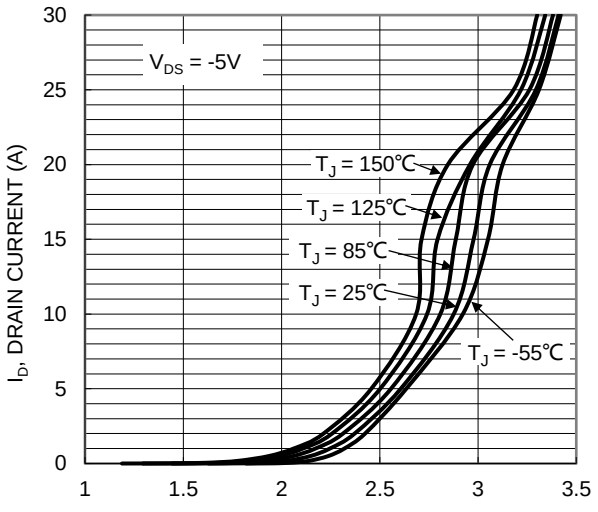


Figure 2. Typical Transfer Characteristic

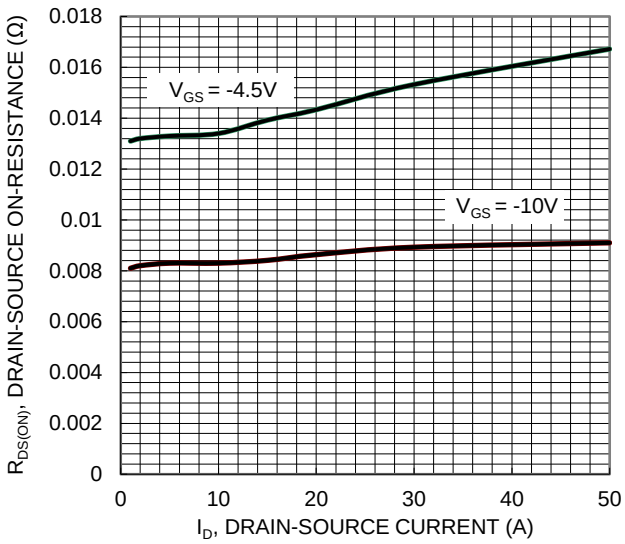


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

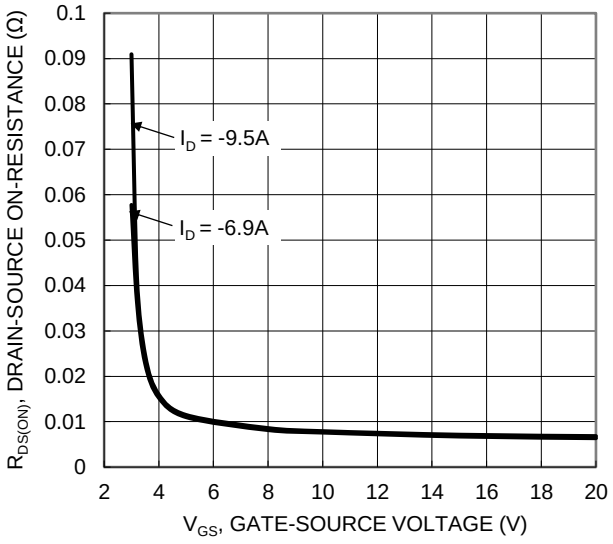


Figure 4. Typical Transfer Characteristic

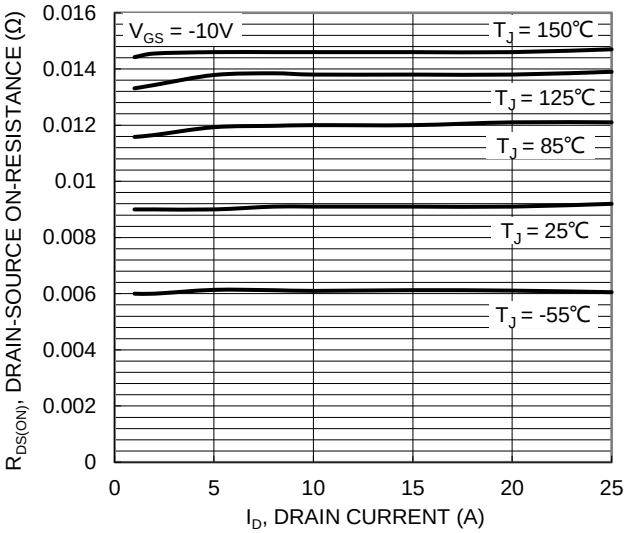


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

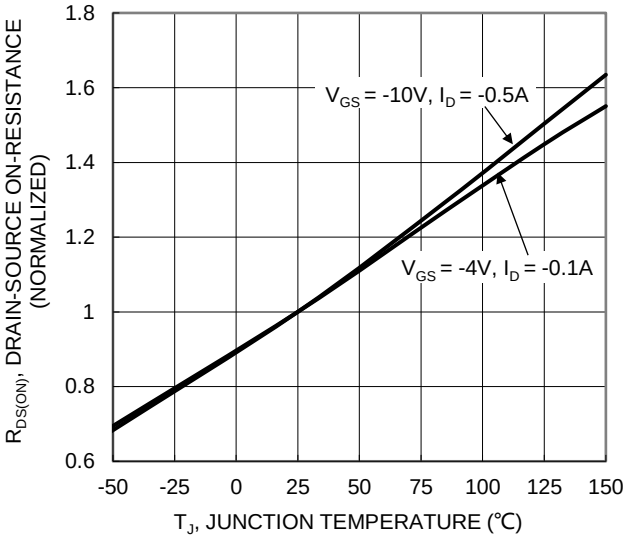


Figure 6. On-Resistance Variation with Temperature

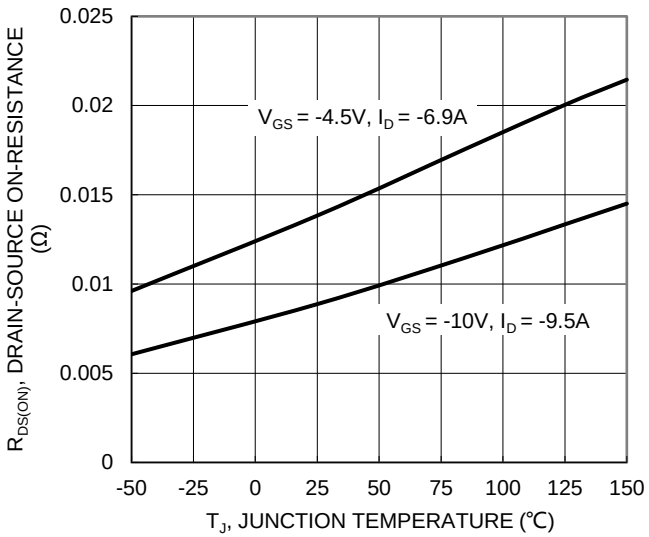


Figure 7. On-Resistance Variation with Temperature

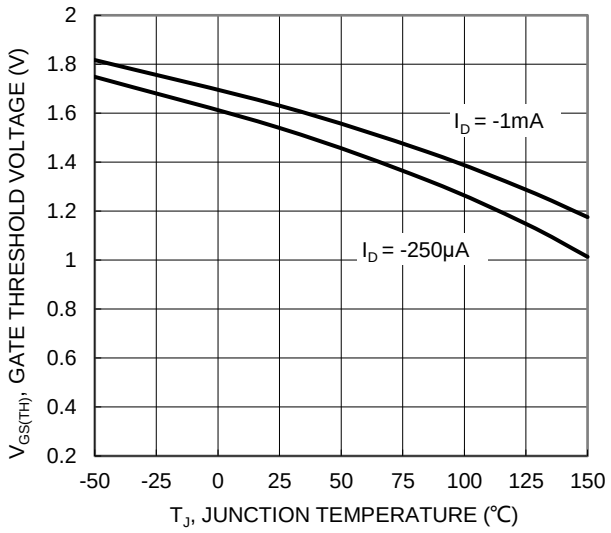


Figure 8. Gate Threshold Variation vs. Junction Temperature

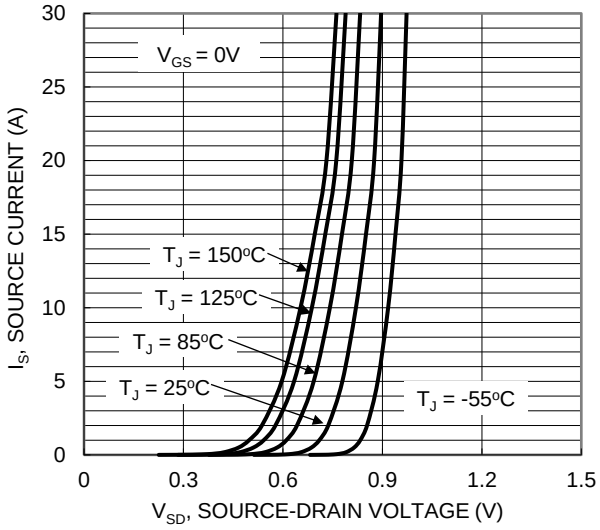


Figure 9. Diode Forward Voltage vs. Current

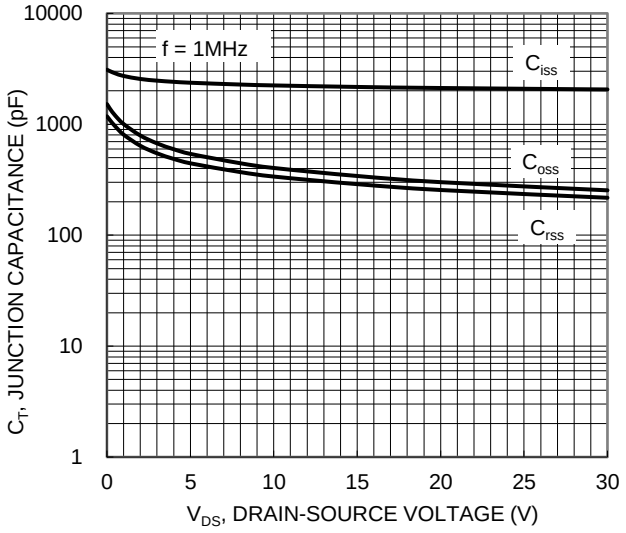


Figure 10. Typical Junction Capacitance

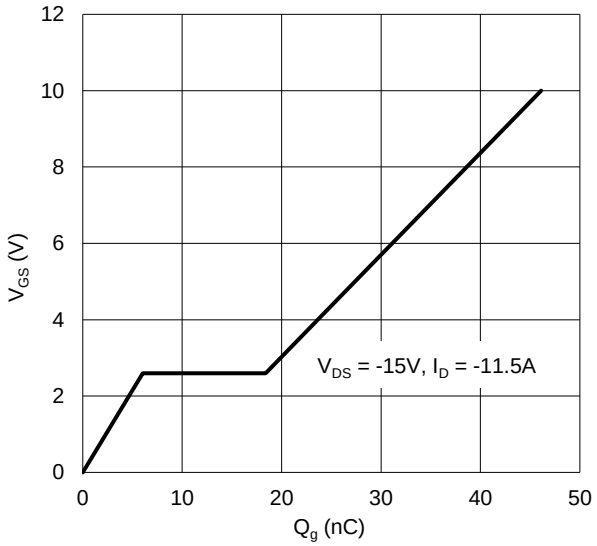


Figure 11. Gate Charge

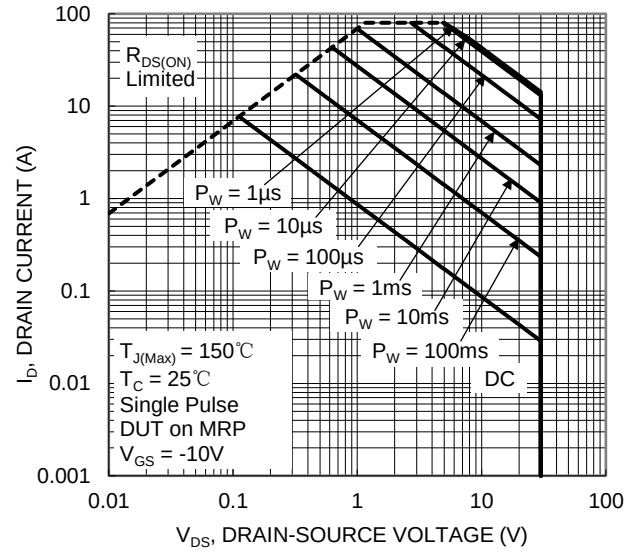


Figure 12. SOA, Safe Operation Area

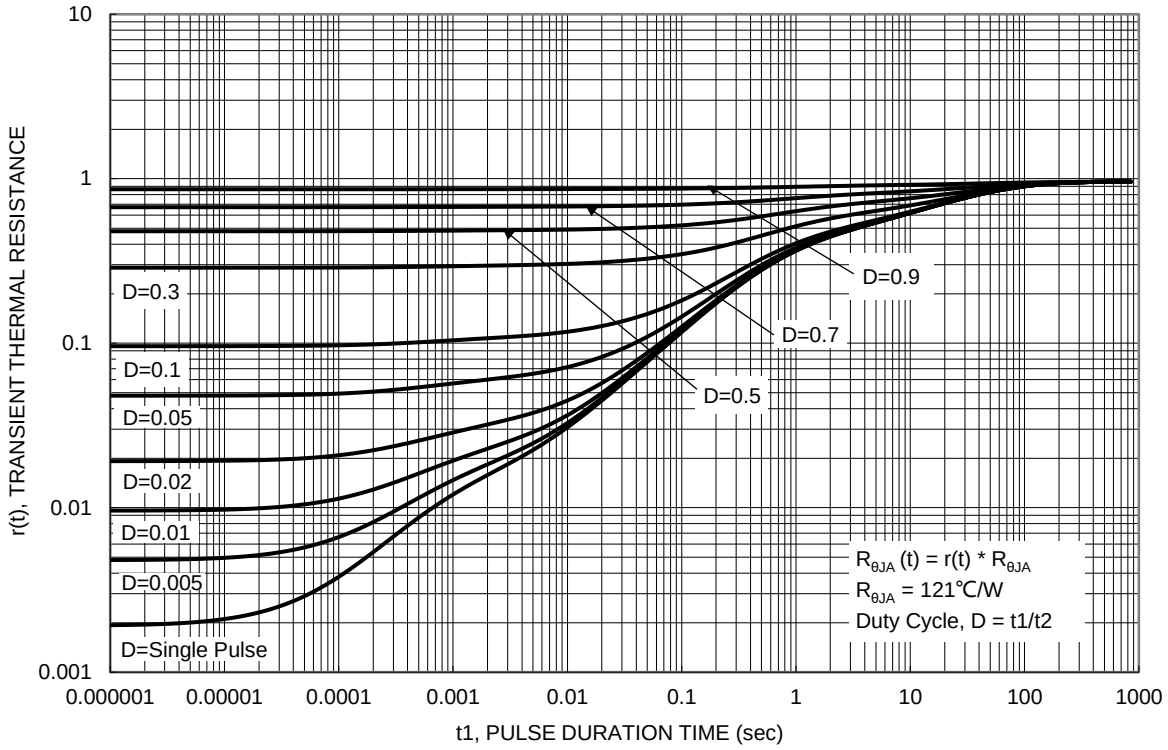
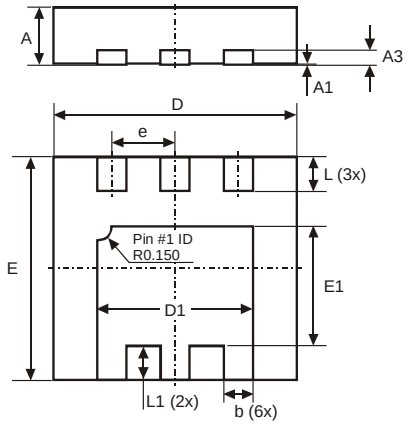


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN2523-6

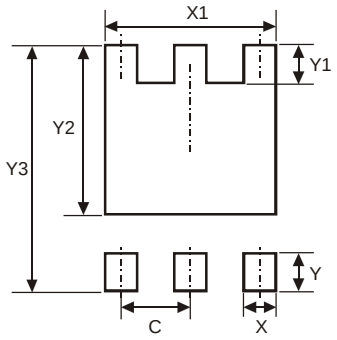


U-DFN2523-6			
Dim	**Min**	**Max**	**Typ**
A	0.57	0.63	0.60
A1	0	0.05	0.02
A3	-	-	0.152
b	0.25	0.35	0.30
D	2.45	2.55	2.50
D1	1.55	1.65	1.60
e	-	-	0.65
E	2.25	2.35	2.30
E1	1.18	1.28	1.23
L	0.30	0.40	0.35
L1	0.30	0.40	0.35
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN2523-6



Dimensions	Value (in mm)
C	0.650
X	0.400
X1	1.700
Y	0.650
Y1	0.450
Y2	1.830
Y3	2.700

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