40V P-CHANNEL ENHANCEMENT MODE MOSFET
PowerDI5060-8

Product Summary

BV_{DSS}	$R_{DS(ON)}$ MAX	I_D T_C = +25°C
-40V	10mΩ @ V_{GS} = -10V	-86A
	14mΩ @ V_{GS} = -4.5V	-75A

Features and Benefits

- 100% Unclamped Inductive Switch (UIS) Test in Production
- Low On-Resistance
- Fast Switching Speed
- Wettable Flank for Improved Optical Inspections
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Description and Applications

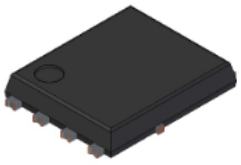
This new generation MOSFET has been designed to minimize the on-state resistance ($R_{DS(ON)}$) yet maintain superior switching performance, making it ideal for high-efficiency power-management applications.

- DC-DC converters
- Power-management functions
- Analog switches

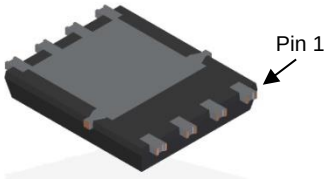
Mechanical Data

- Package: PowerDI®5060-8
- Package Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal: Finish – Matte Tin Annealed over Copper Leadframe; Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.097 grams (Approximate)

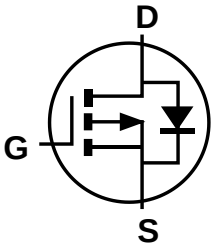
PowerDI5060-8/SWP (Type UX)



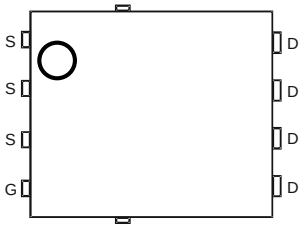
Top View



Bottom View



Internal Schematic



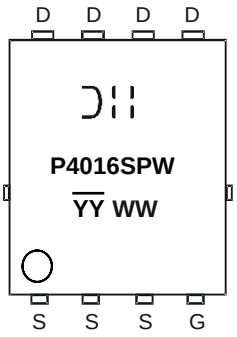
Top View
Pin Configuration

Ordering Information (Note 4)

Part Number	Package	Packing	
		Qty.	Carrier
DMP4016SPSW-13	PowerDI5060-8/SWP (Type UX)	2,500	Tape & Reel

Notes:
1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



= Manufacturer's Marking
P4016SPW = Product Type Marking Code
YYWW = Date Code Marking
YY = Year (ex: 23 = 2023)
WW = Week (01 to 53)

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	-40	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current (Note 5) V_{GS} = -10V	Steady State	T_C = +25°C T_C = +70°C	I_D	-86 -69	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I_{DM}	-345	A
Maximum Body Diode Continuous Current (Note 5)			I_S	-86	A
Pulsed Source Current (10µs Pulse, Duty Cycle = 1%)			I_{SM}	-345	A
Avalanche Current L = 1mH			I_{AS}	-28.9	A
Avalanche Energy L = 1mH			E_{AS}	418.6	mJ

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 6)	T_A = +25°C	P_D	3.9	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	32	°C/W
Total Power Dissipation (Note 5)	T_C = +25°C	P_D	119	W
Thermal Resistance, Junction to Case (Note 5)		$R_{\theta JC}$	1.05	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Notes: 5. Thermal resistance from junction to soldering point (on the exposed drain pad).
6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-40	—	—	V	V_{GS} = 0V, I_D = -250µA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	µA	V_{DS} = -40V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	-1.5	—	-2.5	V	V_{DS} = V_{GS}, I_D = -250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	5.4	10	mΩ	V_{GS} = -10V, I_D = -9.8A
		—	8.0	14		V_{GS} = -4.5V, I_D = -9.8A
Diode Forward Voltage	V_{SD}	—	-0.67	-1	V	V_{GS} = 0V, I_S = -1A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	5697	—	pF	V_{DS} = -20V, V_{GS} = 0V f = 1MHz
Output Capacitance	C_{oss}	—	534	—		
Reverse Transfer Capacitance	C_{rss}	—	408	—		
Gate Resistance	R_g	—	7	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = -4.5V)	Q_g	—	53	—	nC	V_{DS} = -20V, I_D = -9.8A
Total Gate Charge (V_{GS} = -10V)	Q_g	—	112	—		
Gate-Source Charge	Q_{gs}	—	20	—		
Gate-Drain Charge	Q_{gd}	—	18	—		
Turn-On Delay Time	$t_{D(ON)}$	—	11.5	—	ns	V_{GS} = -10V, V_{DD} = -20V R_g = 2Ω, I_D = -9.8A
Turn-On Rise Time	t_R	—	41	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	146	—		
Turn-Off Fall Time	t_F	—	165	—		
Reverse Recovery Time	t_{RR}	—	27	—	ns	I_F = -9.8A, dI/dt = -100A/µs
Reverse Recovery Charge	Q_{RR}	—	22	—	nC	I_F = -9.8A, dI/dt = -100A/µs

Notes: 7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

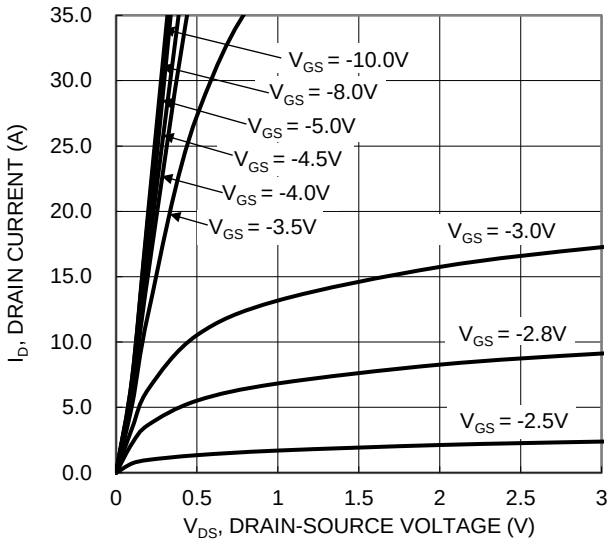


Figure 1. Typical Output Characteristic

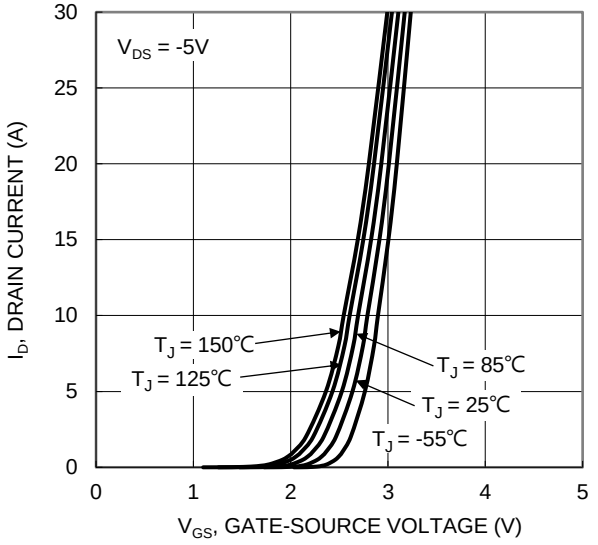


Figure 2. Typical Transfer Characteristic

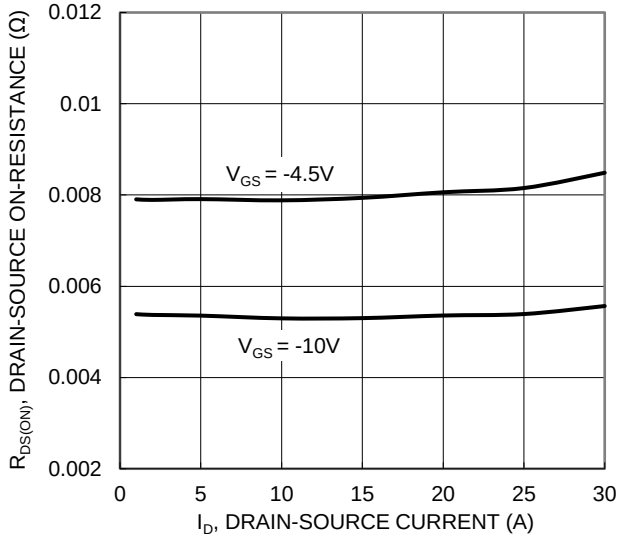


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

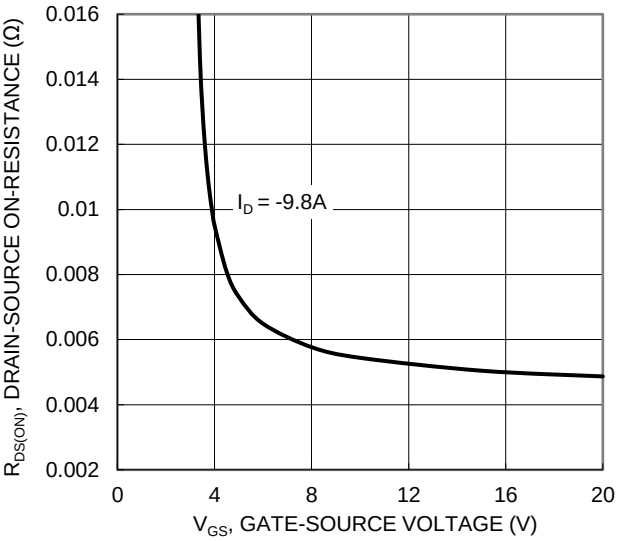


Figure 4. Typical Transfer Characteristic

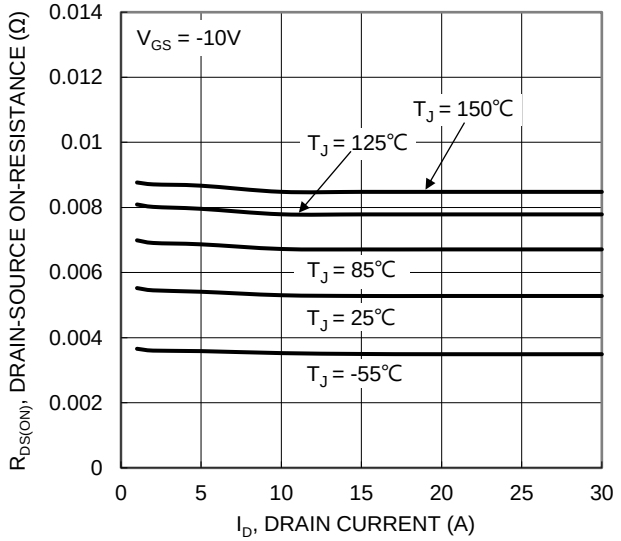


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

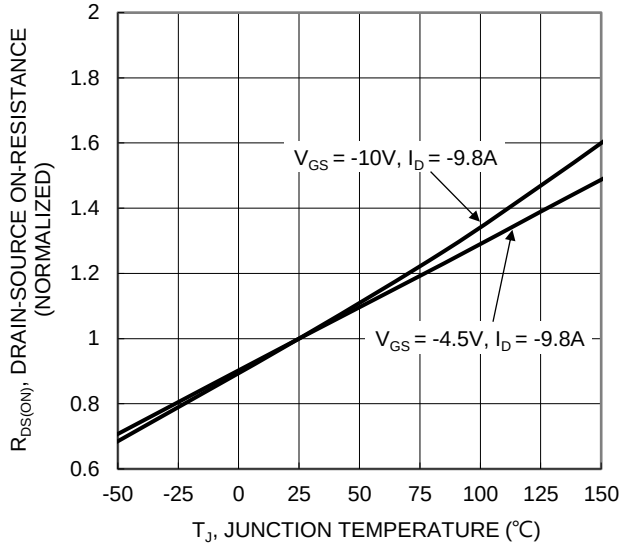


Figure 6. On-Resistance Variation with Junction Temperature

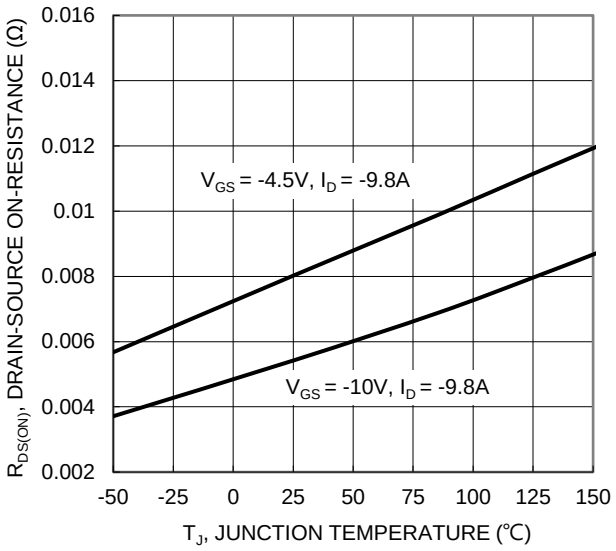


Figure 7. On-Resistance Variation with Junction Temperature

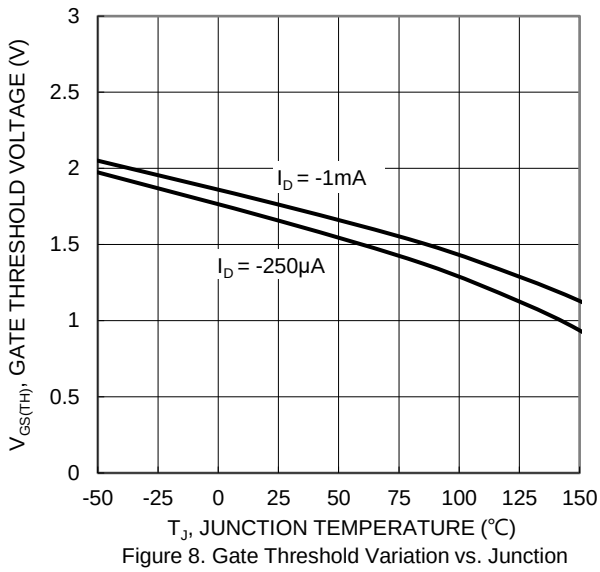


Figure 8. Gate Threshold Variation vs. Junction Temperature

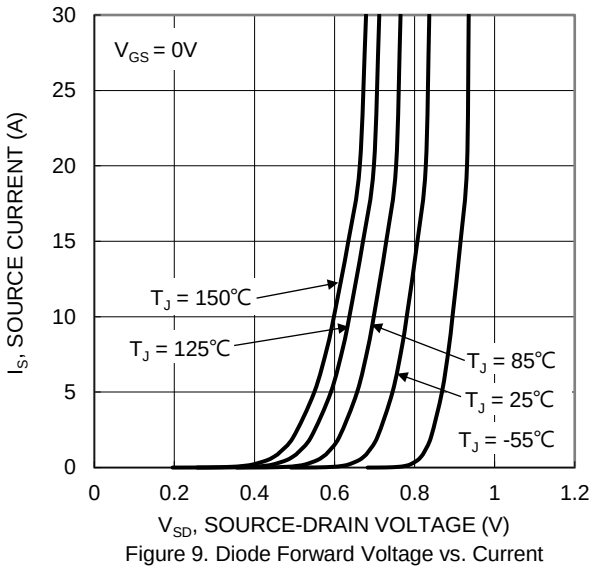


Figure 9. Diode Forward Voltage vs. Current

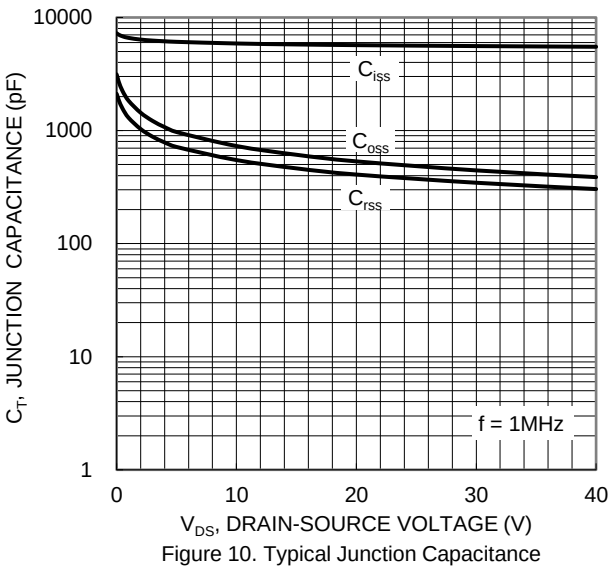


Figure 10. Typical Junction Capacitance

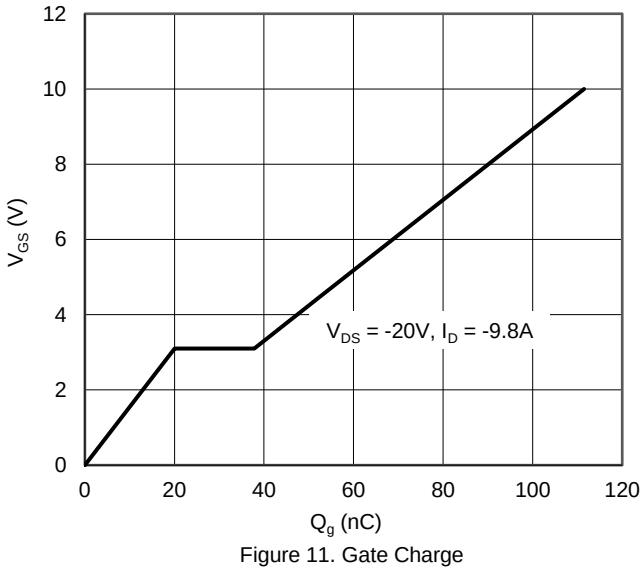


Figure 11. Gate Charge

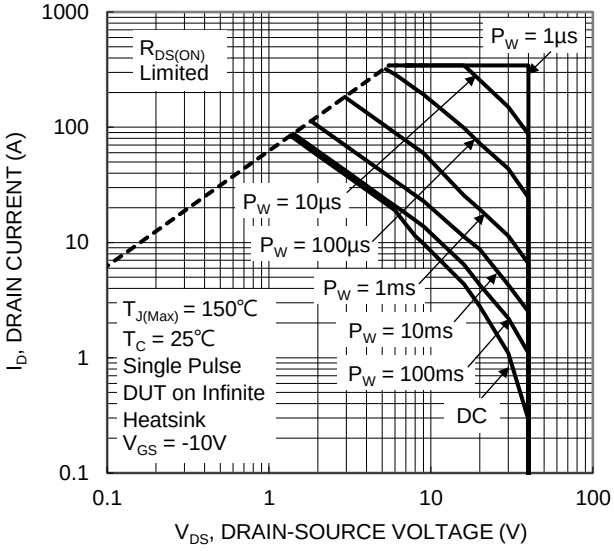


Figure 12. SOA, Safe Operation Area

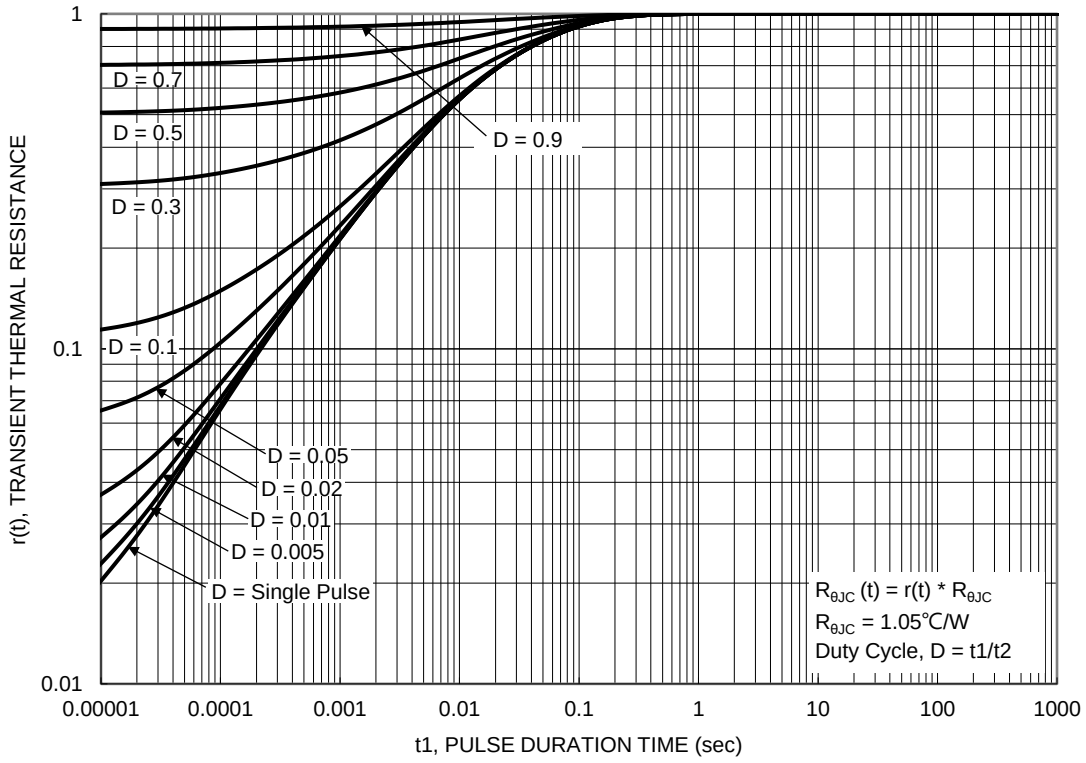
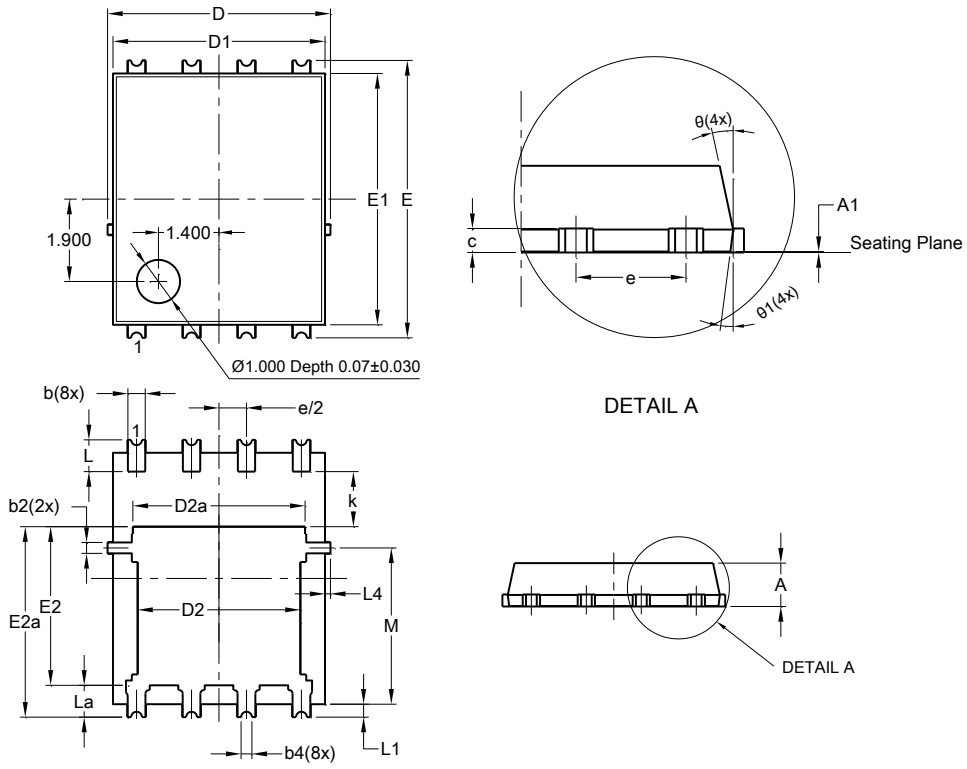


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8/SWP (Type UX)



PowerDI5060-8/SWP (Type UX)			
Dim	**Min**	**Max**	**Typ**
A	0.90	1.10	1.00
A1	0	0.05	--
b	0.30	0.50	0.41
b2	0.20	0.35	0.25
b4	0.25REF		
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	3.56	3.96	3.76
D2a	3.78	4.18	3.98
E	6.40 BSC		
E1	5.60	6.00	5.80
E2	3.46	3.86	3.66
E2a	4.195	4.595	4.395
e	1.27BSC		
k	1.05	--	--
L	0.635	0.835	0.735
La	0.635	0.835	0.735
L1	0.200	0.400	0.300
L1a	0.050REF		
L4	0.025	0.225	0.125
M	3.205	4.005	3.605
θ	10°	12°	11°
θ1	6°	8°	7°
All Dimensions in mm			

Suggested Pad Layout

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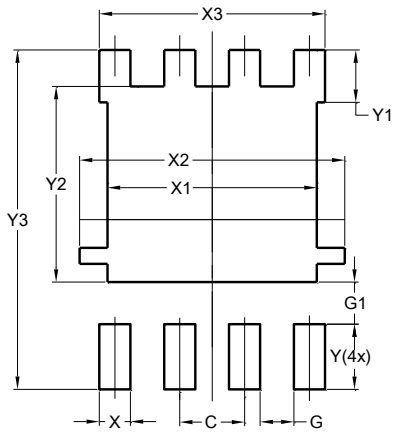
PowerDI5060-8/SWP (Type UX)



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	4.100
X2	5.190
X3	4.420
Y	1.270
Y1	1.020
Y2	3.810
Y3	6.610

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