175°C P-CHANNEL ENHANCEMENT MODE MOSFET
PowerDI5060-8

Product Summary

BV_{DSS}	$R_{DS(ON)\ Max}$	I_D T_C = +25°C
-40V	10mΩ @V_{GS} = -10V	-50A
	14mΩ @V_{GS} = -4.5V	-40A

Features and Benefits

- Rated to +175°C – Ideal for High Ambient Temperature Environments
- 100% Unclamped Inductive Switch (UIS) Test in Production Low On-Resistance
- Fast Switching Speed
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The DMPH4015SPSQ is suitable for automotive applications requiring specific change control; this part is AEC-Q101 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**
  https://www.diodes.com/quality/product-definitions/

Description and Applications

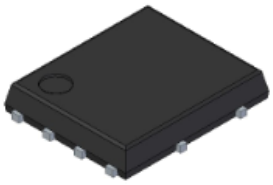
This MOSFET is designed to meet the stringent requirements of automotive applications. It is qualified to AEC-Q101, supported by a PPAP and is ideal for use in:

- Reverse-polarity protections
- BLDC motor controls
- Power-management functions

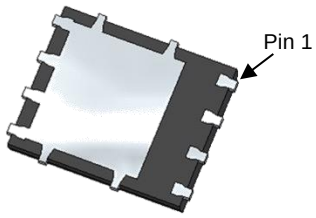
Mechanical Data

- Package: PowerDI®5060-8
- Package Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish – 100% Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.097 grams (Approximate)

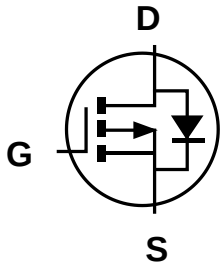
PowerDI5060-8



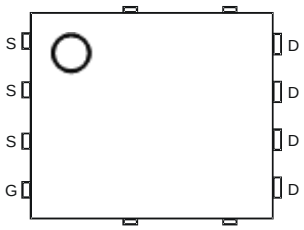
Top View



Bottom View



Internal Schematic



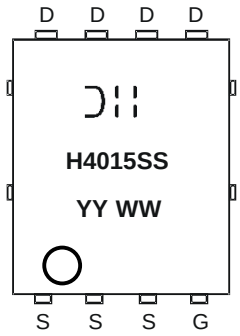
Top View
Pin Configuration

Ordering Information (Note 4)

Part Number	Package	Packing	
		Qty.	Carrier
DMPH4015SPSQ	PowerDI5060-8	2500	Reel

Notes:
1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



= Manufacturer's Marking
H4015SS = Product Type Marking Code
YYWW = Date Code Marking
YY = Year (ex: 24 = 2024)
WW = Week (01 to 53)

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	-40	V
Gate-Source Voltage			V_{GSS}	±25	V
Continuous Drain Current V_{GS} = -10V (Note 7)	Steady State	T_C = +25°C T_C = +100°C	I_D	-50 -35	A
Continuous Drain Current V_{GS} = -10V (Note 6)	Steady State	T_A = +25°C T_A = +100°C	I_D	-12.0 -9.0	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I_{DM}	-100	A
Maximum Body Diode Continuous Current (Note 7)			I_S	-50	A
Avalanche Current L = 1mH			I_{AS}	-22	A
Avalanche Energy L = 1mH			E_{AS}	260	mJ

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	T_A = +25°C	P_D	1.5	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	98	°C/W
Total Power Dissipation (Note 6)	T_A = +25°C	P_D	2.6	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	57	°C/W
Thermal Resistance, Junction to Case (Note 7)		$R_{\theta JC}$	0.9	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +175	°C

Notes: 5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.
7. Thermal resistance from junction to soldering point (on the exposed drain pad).

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	-40	—	—	V	V_{GS} = 0, I_D = -250µA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	µA	V_{DS} = -40V, V_{GS} = 0
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±25V, V_{DS} = 0
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(TH)}$	-1.5	-2	-2.5	V	V_{DS} = V_{GS}, I_D = -250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	8	10	mΩ	V_{GS} = -10V, I_D = -9.8A
		—	11	14		V_{GS} = -4.5V, I_D = -9.8A
Diode Forward Voltage	V_{SD}	—	-0.7	-1	V	V_{GS} = 0, I_S = -1A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	4234	—	pF	V_{DS} = -20V, V_{GS} = 0, f = 1MHz
Output Capacitance	C_{oss}	—	1036	—		
Reverse Transfer Capacitance	C_{rss}	—	526	—		
Gate Resistance	R_g	—	7.8	—	Ω	V_{DS} = 0, V_{GS} = 0, f = 1MHz
Total Gate Charge (V_{GS} = -4.5V)	Q_g	—	42.7	—	nC	V_{DS} = -20V, I_D = -9.8A
Total Gate Charge (V_{GS} = -10V)	Q_g	—	91	—		
Gate-Source Charge	Q_{gs}	—	14.2	—		
Gate-Drain Charge	Q_{gd}	—	13.5	—		
Turn-On Delay Time	$t_{D(ON)}$	—	13.2	—	ns	V_{GS} = -10V, V_{DD} = -20V, R_G = 6Ω, I_D = -1A
Turn-On Rise Time	t_R	—	10	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	303	—		
Turn-Off Fall Time	t_F	—	138	—		
Reverse-Recovery Time	t_{RR}	—	26	—	ns	I_F = -9.8A, di/dt = -100A/µs
Reverse-Recovery Charge	Q_{RR}	—	20	—	nC	I_F = -9.8A, di/dt = -100A/µs

Notes: 8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to product testing.

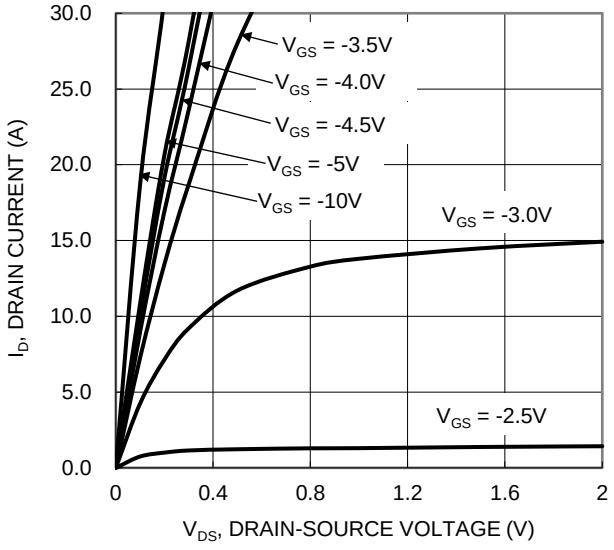


Figure 1. Typical Output Characteristic

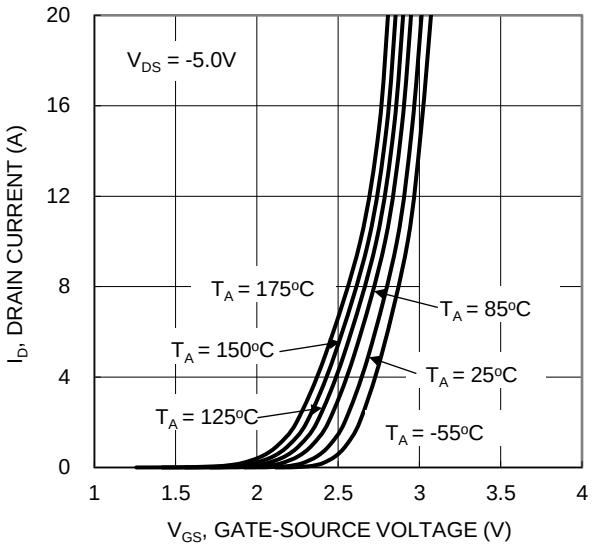


Figure 2. Typical Transfer Characteristic

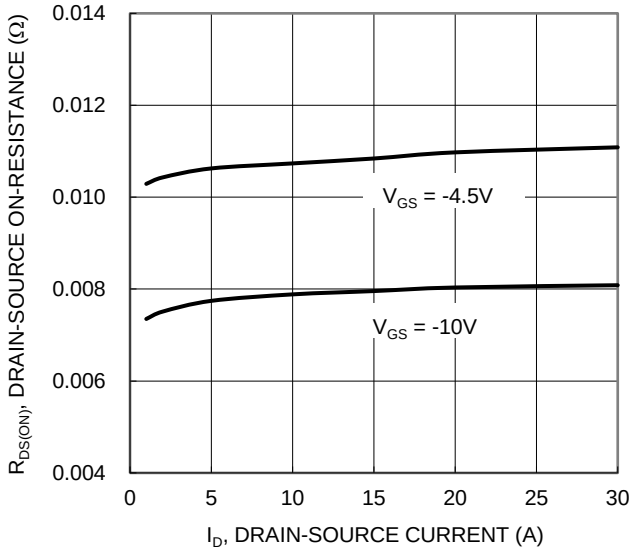


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

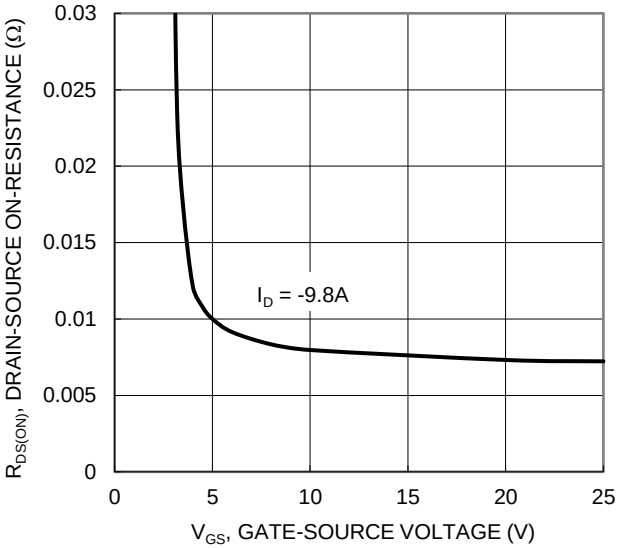


Figure 4. Typical Transfer Characteristic

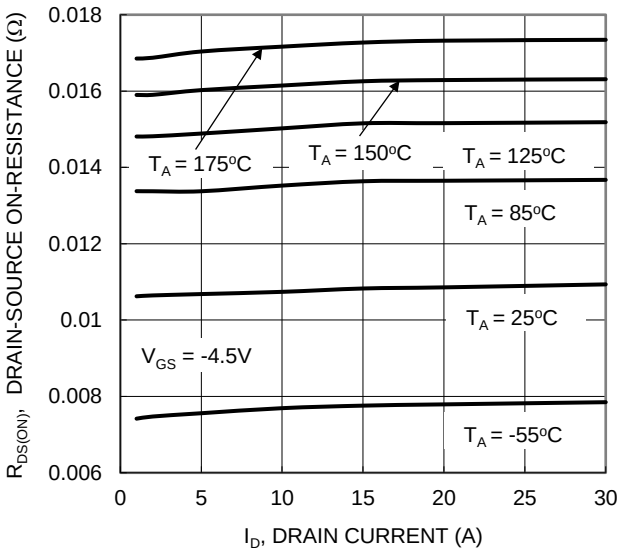


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

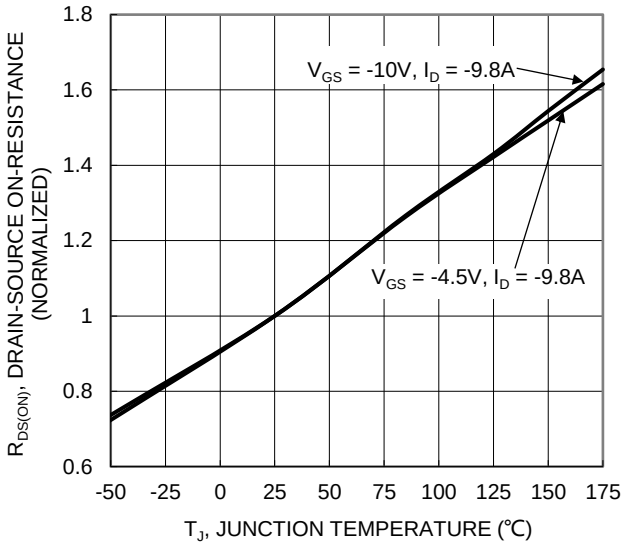


Figure 6. On-Resistance Variation with Temperature

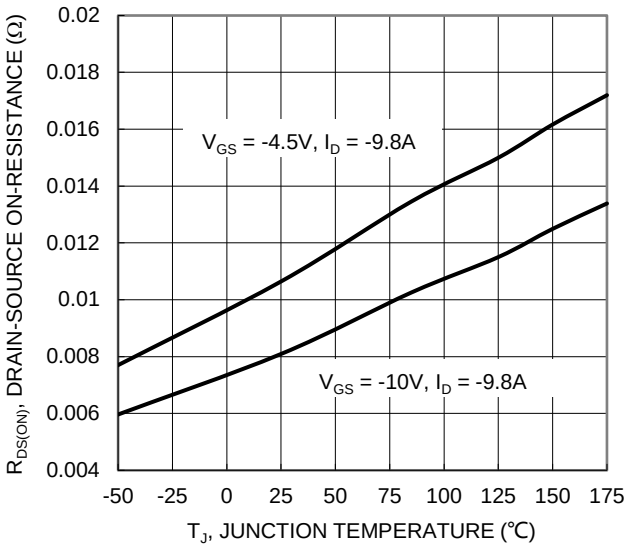


Figure 7. On-Resistance Variation with Temperature

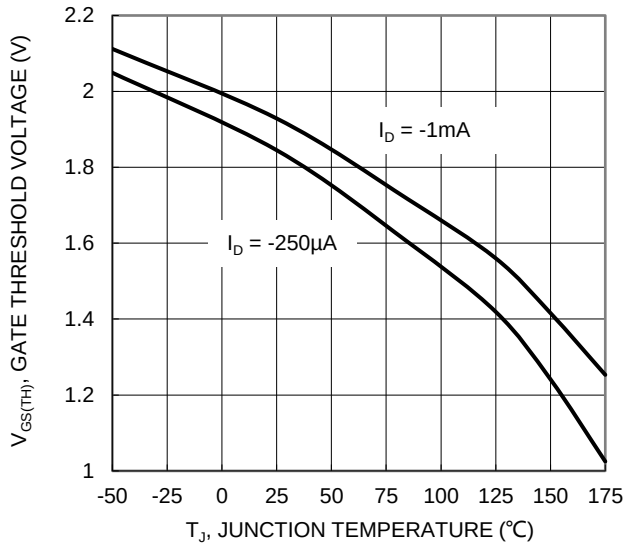


Figure 8. Gate Threshold Variation vs. Junction Temperature

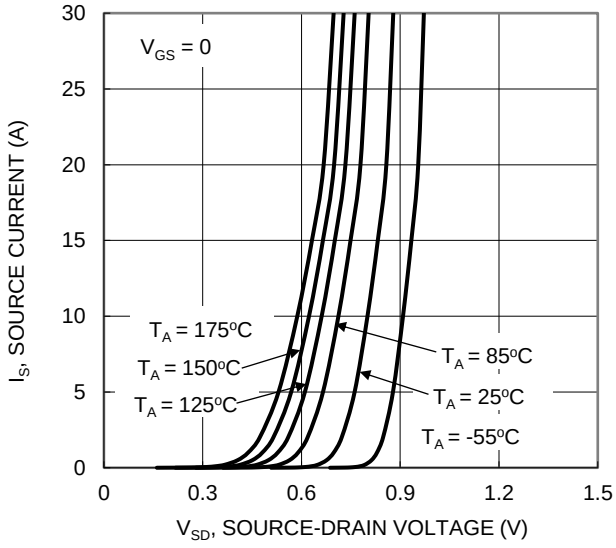


Figure 9. Diode Forward Voltage vs. Current

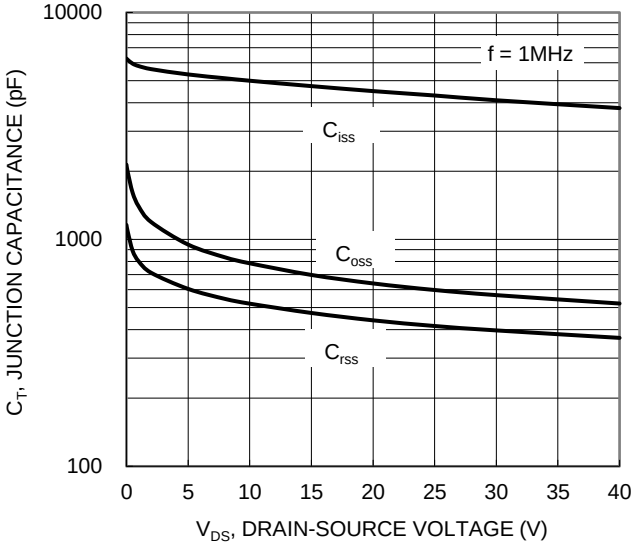


Figure 10. Typical Junction Capacitance

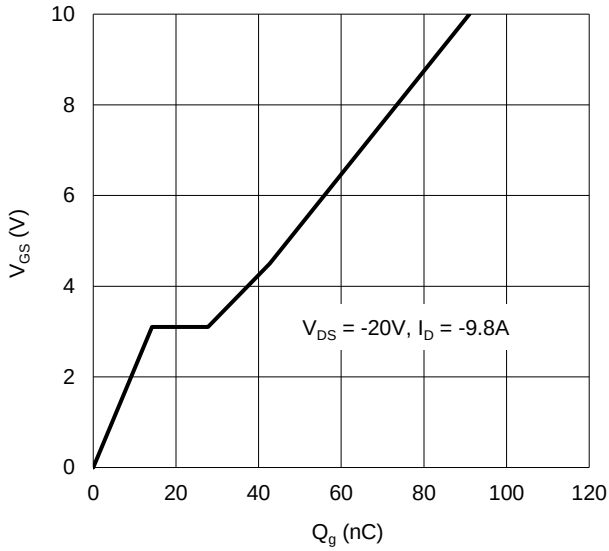


Figure 11. Gate Charge

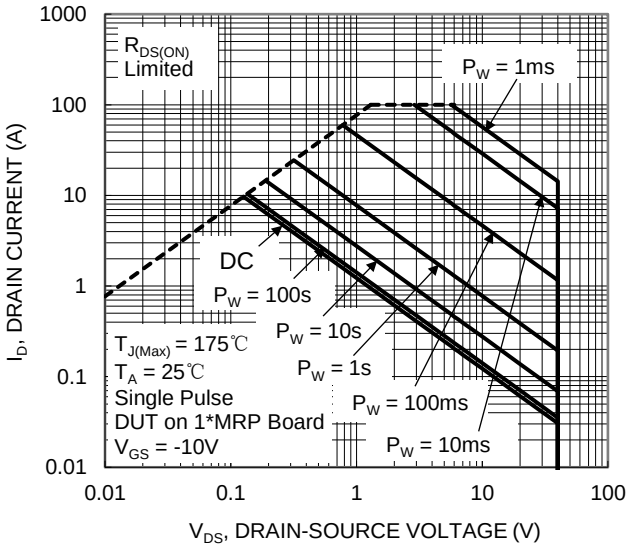


Figure 12. SOA, Safe Operation Area

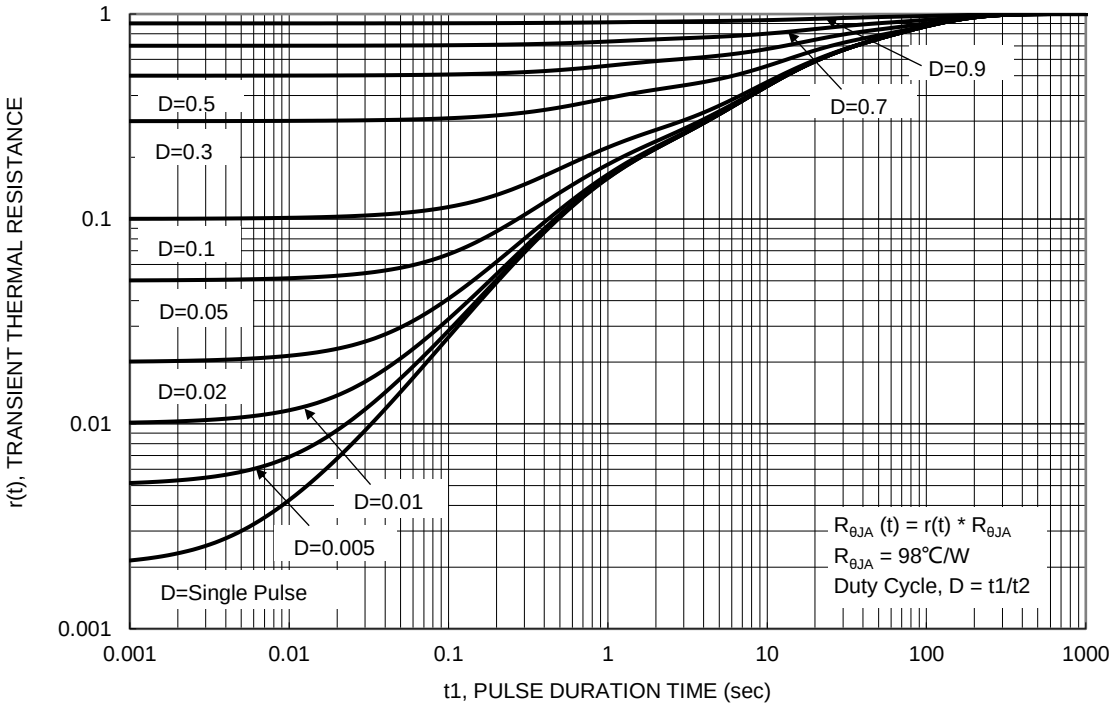
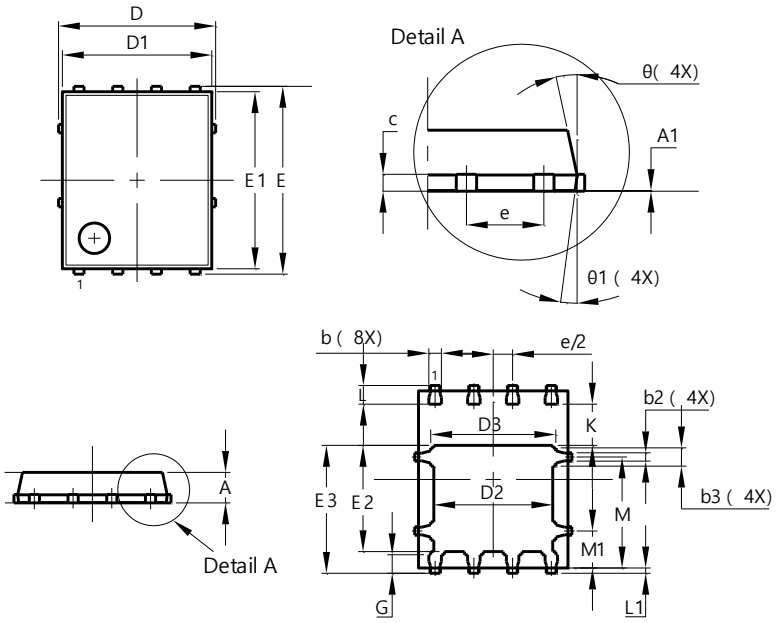


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8

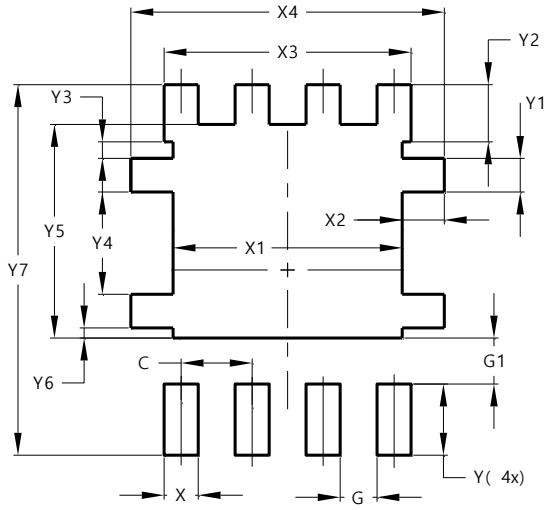


PowerDI5060-8			
Dim	**Min**	**Max**	**Typ**
A	0.90	1.10	1.00
A1	0.00	0.05	–
b	0.33	0.51	0.41
b2	0.200	0.350	0.273
b3	0.40	0.80	0.60
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	3.70	4.10	3.90
D3	3.90	4.30	4.10
E	6.15 BSC		
E1	5.60	6.00	5.80
E2	3.28	3.68	3.48
E3	3.99	4.39	4.19
e	1.27 BSC		
G	0.51	0.71	0.61
K	0.51	–	–
L	0.51	0.71	0.61
L1	0.100	0.200	0.175
M	3.235	4.035	3.635
M1	1.00	1.40	1.21
Θ	10°	12°	11°
Θ1	6°	8°	7°
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	4.100
X2	0.755
X3	4.420
X4	5.610
Y	1.270
Y1	0.600
Y2	1.020
Y3	0.295
Y4	1.825
Y5	3.810
Y6	0.180
Y7	6.610

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