40V +175°C DUAL P-CHANNEL ENHANCEMENT MODE MOSFET
PowerDI5060-8

Product Summary

BV_{DSS}	$R_{DS(ON)}$ Max	I_D Max T_C = +25°C
-40V	26mΩ @ V_{GS} = -10V	-27A

Features and Benefits

- Rated to +175°C – Ideal for High Ambient Temperature Environments
- High Conversion Efficiency
- Low $R_{DS(ON)}$ – Minimizes On-State Losses
- Low Input Capacitance
- Fast Switching Speed
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **This part is qualified to JEDEC standards (as references in AEC-Q) for High Reliability. https://www.diodes.com/quality/product-definitions/**
- **An automotive-compliant part is available under separate datasheet (DMPH4023SPDWQ)**

Description and Applications

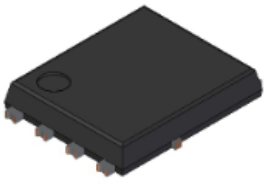
This MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) yet maintain superior switching performance, making it ideal for high-efficiency power-management applications.

- Backlighting
- Power-management functions
- DC-DC converters

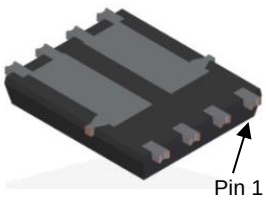
Mechanical Data

- Package: PowerDI®5060-8
- Package Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Diagram
- Terminals: Finish — Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.097 grams (Approximate)

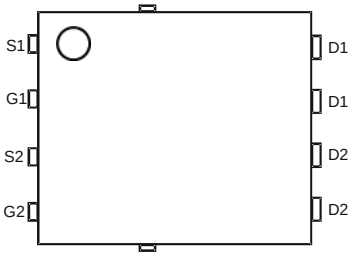
PowerDI5060-8/SWP (Type UXD)



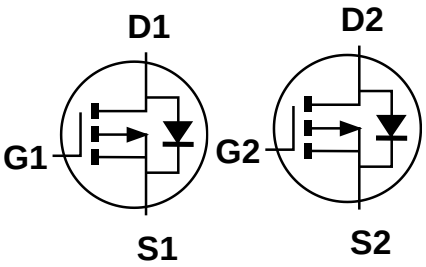
Top View



Bottom View



Pinout
Top View



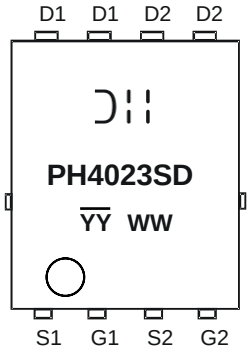
Equivalent Circuit

Ordering Information (Note 4)

Orderable Part Number	Package	Packing	
		Qty.	Carrier
DMPH4023SPDW-13	PowerDI5060-8/SWP (Type UXD)	2500	Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



= Manufacturer's Marking
PH4023SD = Product Type Marking Code
YYWW = Date Code Marking
YY = Year (ex: 24 = 2024)
WW = Week (01 to 53)

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	-40	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current (Note 5) V_{GS} = -10V	T_C = +25°C T_C = +100°C	I_D	-27 -20	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)		I_{DM}	-50	A
Maximum Continuous Body Diode Forward Current (Note 5)		I_S	-3	A
Pulsed Body Diode Forward Current (10µs Pulse, Duty Cycle = 1%)		I_{SM}	-50	A
Avalanche Current, L = 0.1mH (Note 6)		I_{AS}	-40	A
Avalanche Energy, L = 0.1mH (Note 6)		E_{AS}	85	mJ

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 7)		P_D	1.5	W
Thermal Resistance, Junction to Ambient (Note 7)	Steady State	$R_{\theta JA}$	99	°C/W
	t < 10s		52	
Total Power Dissipation (Note 5)		P_D	3.1	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	49	°C/W
	t < 10s		26	
Thermal Resistance, Junction to Case		$R_{\theta JC}$	5	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +175	°C

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.
6. I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep T_J = +25°C.
7. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	-40	—	—	V	V_{GS} = 0V, I_D = -250μA
Zero Gate Voltage Drain Current T_J = +25°C	I_{DSS}	—	—	-1	μA	V_{DS} = -40V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(TH)}$	-1	—	-3	V	V_{DS} = V_{GS}, I_D = -250μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	22	26	mΩ	V_{GS} = -10V, I_D = -10A
Diode Forward Voltage	V_{SD}	—	-0.75	-1.2	V	V_{GS} = 0V, I_S = -1.0A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	1091	—	pF	V_{DS} = -20V, V_{GS} = 0V f = 1MHz
Output Capacitance	C_{oss}	—	288	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	111	—	pF	
Gate Resistance	R_g	—	14	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge	Q_g	—	18.7	—	nC	V_{DS} = -20V, I_D = -10A V_{GS} = -10V
Gate-Source Charge	Q_{gs}	—	4.2	—	nC	
Gate-Drain Charge	Q_{gd}	—	5.0	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	5.3	—	ns	V_{DD} = -20V, V_{GS} = -10V R_g = 6Ω, , I_D = -10A
Turn-On Rise Time	t_R	—	4.8	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	30.7	—	ns	
Turn-Off Fall Time	t_F	—	23.4	—	ns	
Body Diode Reverse-Recovery Time	t_{RR}	—	17.8	—	ns	I_F = -10A, di/dt = -100A/μs
Body Diode Reverse-Recovery Charge	Q_{RR}	—	9.2	—	nC	

Notes: 8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to product testing.

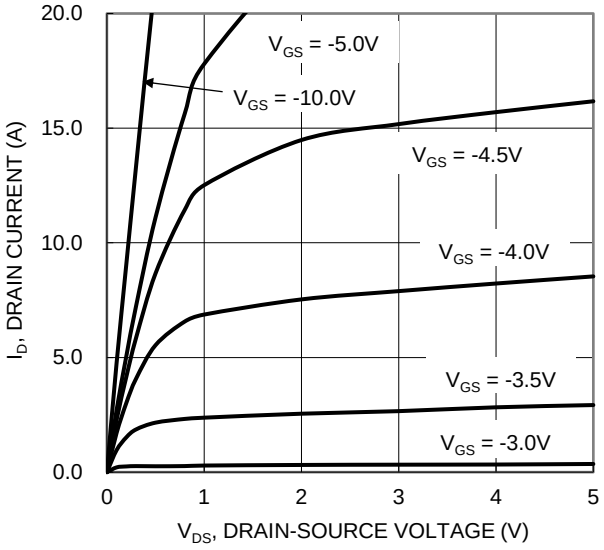


Figure 1. Typical Output Characteristic

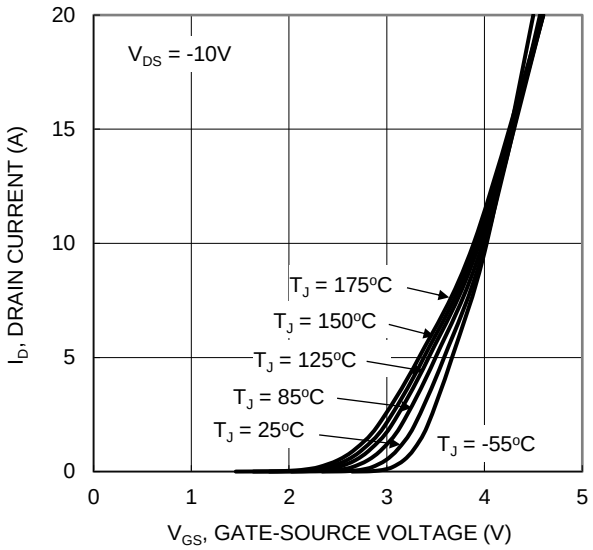


Figure 2. Typical Transfer Characteristic

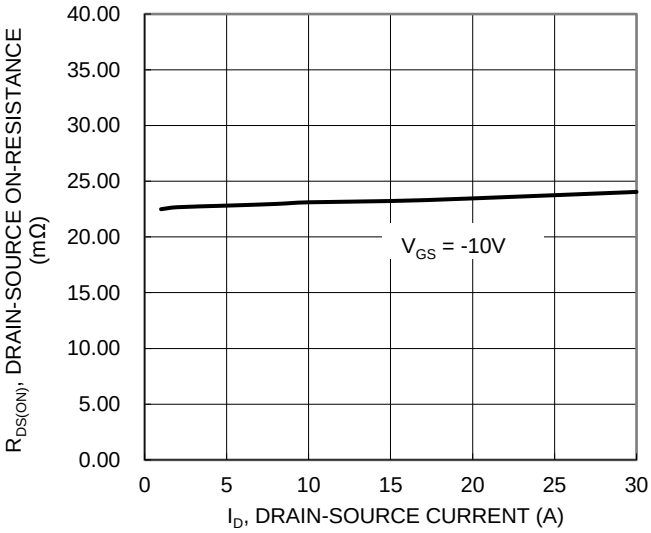


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

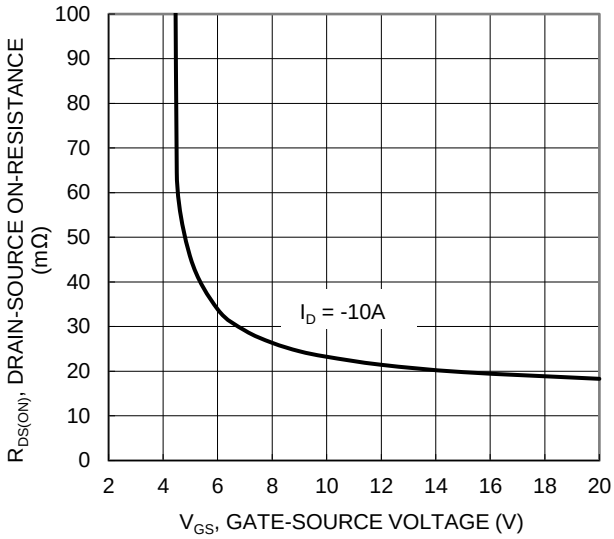


Figure 4. Typical Transfer Characteristic

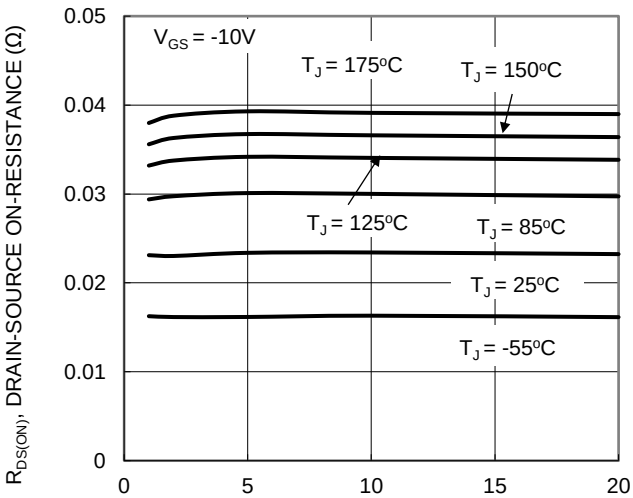


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

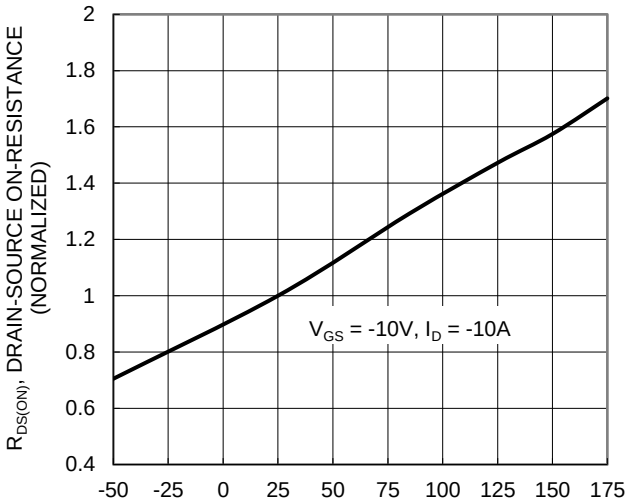


Figure 6. On-Resistance Variation with Junction Temperature

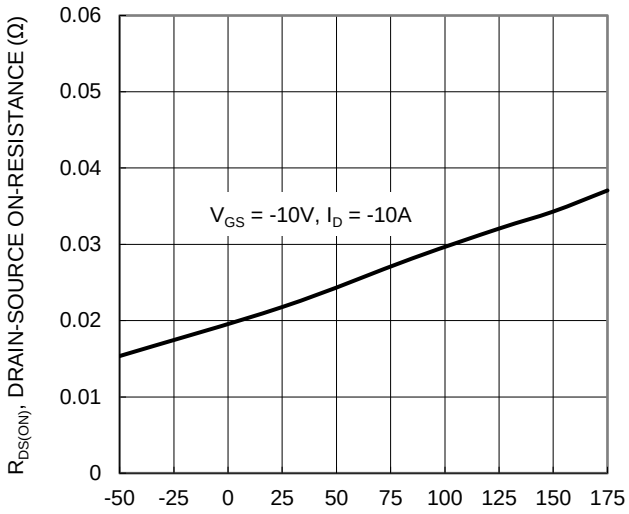


Figure 7. On-Resistance Variation with Junction Temperature

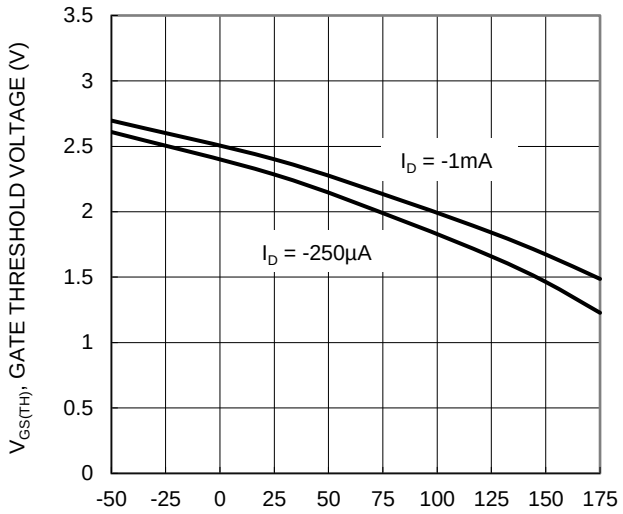


Figure 8. Gate Threshold Variation vs. Junction Temperature

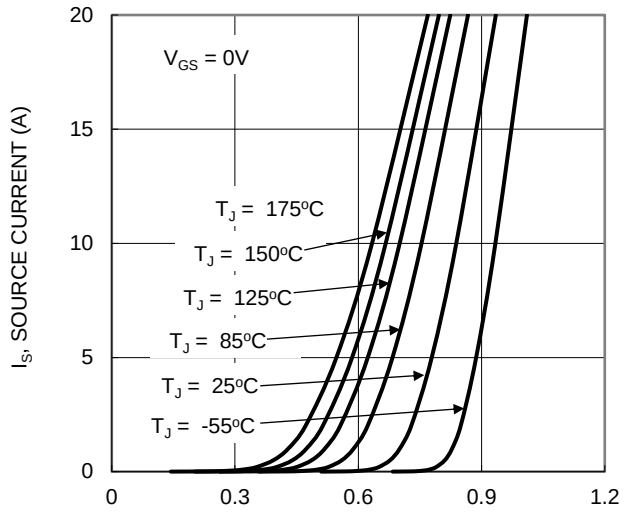


Figure 9. Diode Forward Voltage vs. Current

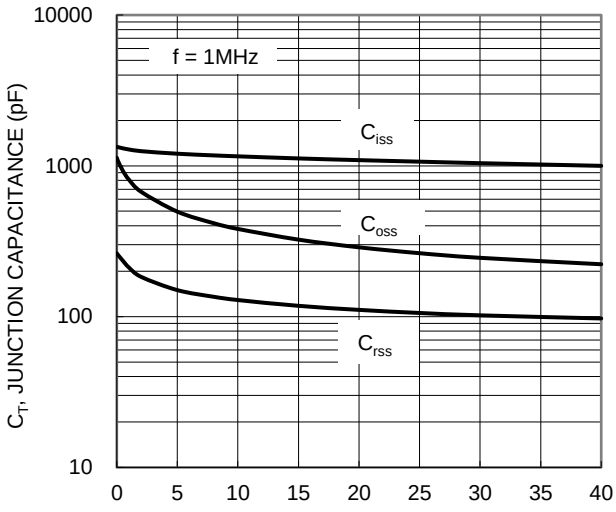


Figure 10. Typical Junction Capacitance

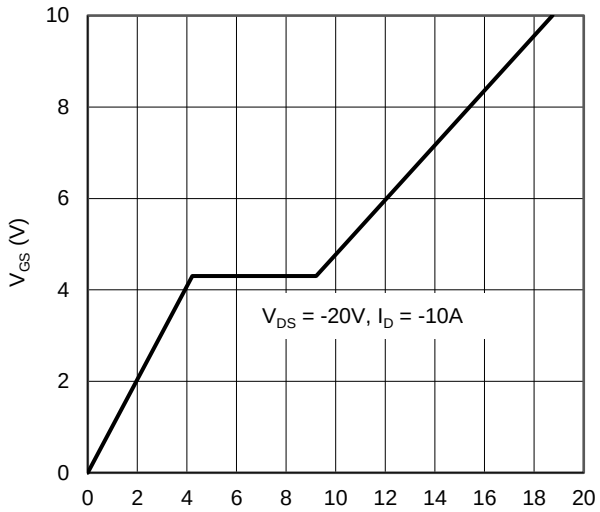


Figure 11. Gate Charge

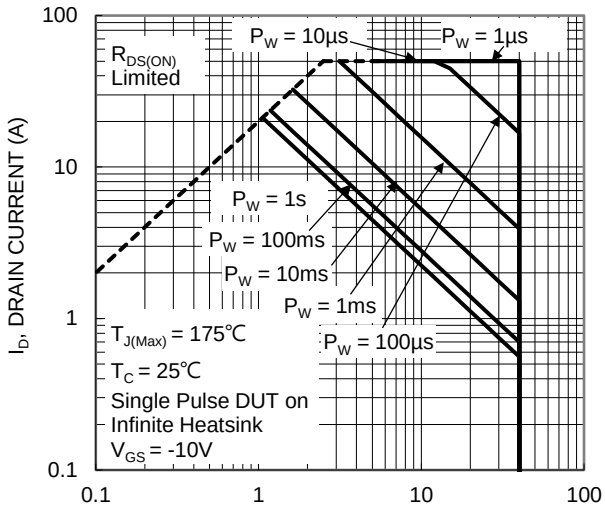


Figure 12. SOA, Safe Operation Area

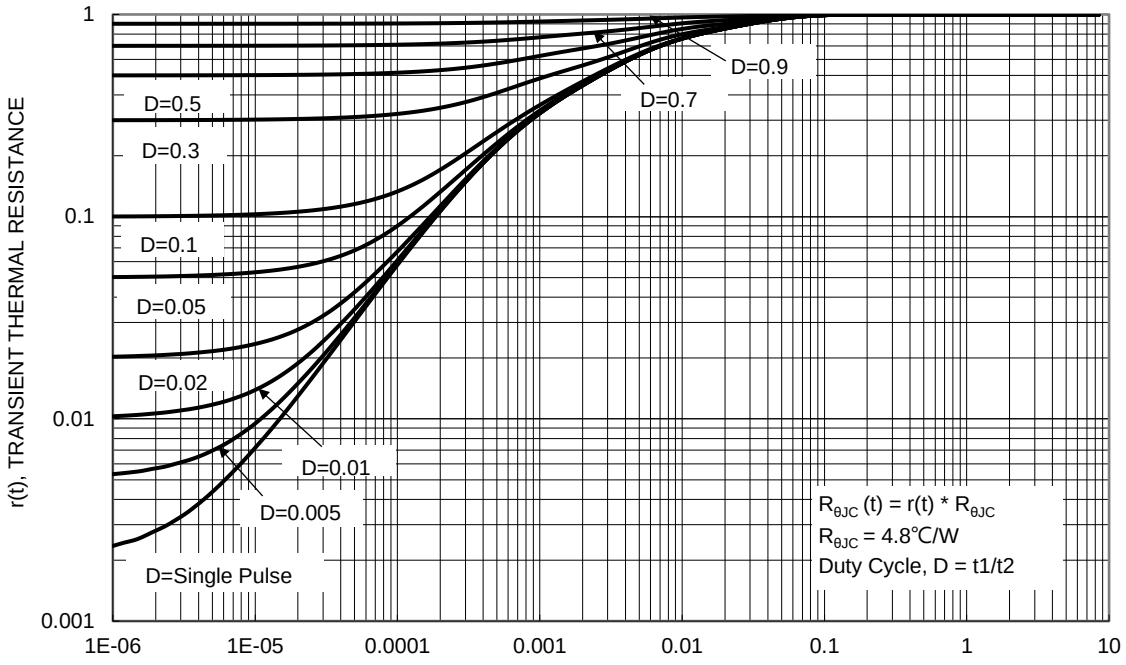
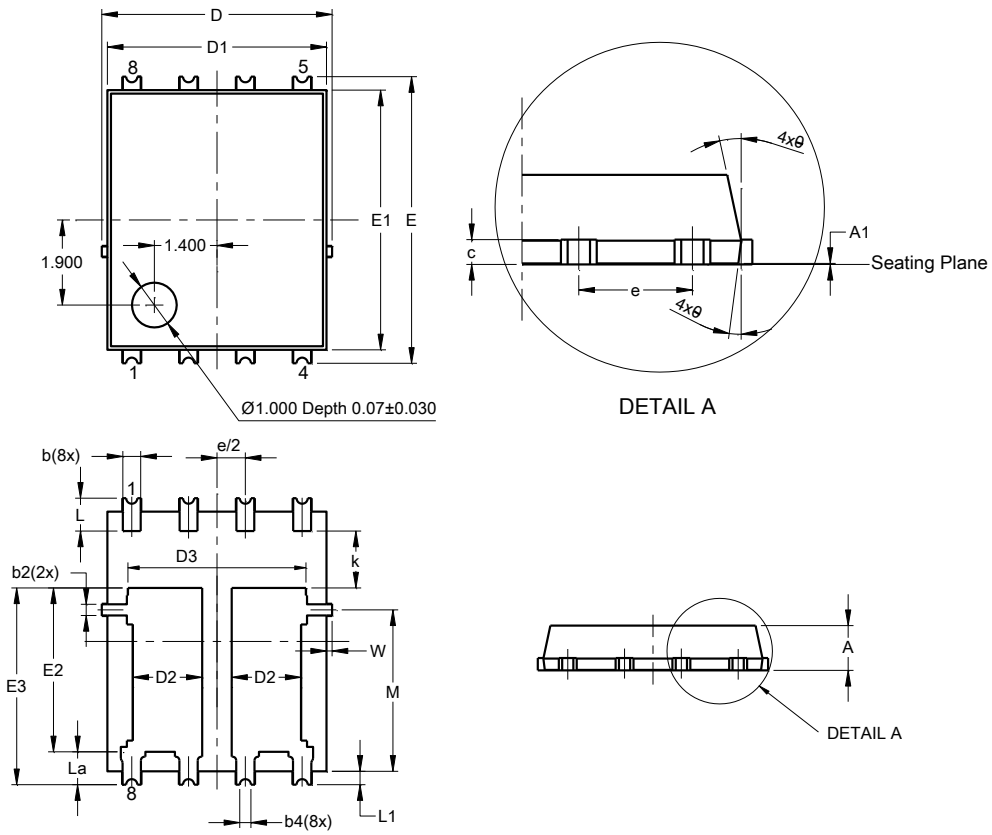


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8/SWP (Type UXD)

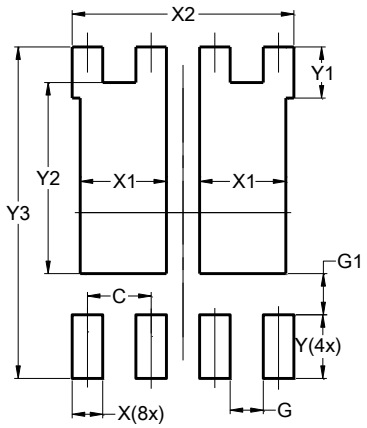


PowerDI5060-8/SWP (Type UXD)			
Dim	**Min**	**Max**	**Typ**
A	0.90	1.10	1.00
A1	0.00	0.05	--
b	0.30	0.50	0.41
b2	0.20	0.35	0.25
b4	0.25REF		
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	1.46	1.66	1.55
D3	3.78	4.18	3.98
E	6.40 BSC		
E1	5.60	6.00	5.80
E2	3.46	3.86	3.66
E2a	4.195	4.595	4.395
e	1.27BSC		
k	1.05	--	--
L	0.635	0.835	0.735
La	0.635	0.835	0.735
L1	0.200	0.400	0.300
M	3.205	4.005	3.605
W	0.025	0.225	0.125
θ	10°	12°	11°
θ1	6°	8°	7°
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8/SWP (Type UXD)



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	1.720
X2	4.420
Y	1.270
Y1	1.020
Y2	3.810
Y3	6.610

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