

Product Summary

BV _{DSS}	R _{DS(ON)} Max	I _D Max T _c = +25°C
150V	66mΩ @ V _{GS} = 10V	24A

Features and Benefits

- 100% Unclamped Inductive Switching (UIS) Test in Production – Ensures More Reliable and Robust End Application
- Thermally Efficient Package-Cooler Running Applications
- Low R_{DS(ON)} – Minimizes On-State Losses
- Low Q_g – Minimizes Switching Losses
- < 1.1mm Package Profile – Ideal for Thin Applications (PowerDI®)
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. “Green” Device (Note 3)**
- **This part is qualified to JEDEC standards (as references in AEC-Q) for High Reliability.**
<https://www.diodes.com/quality/product-definitions/>
- **An automotive-compliant part is available under separate datasheet (DMT15H053SPSWQ)**

Description and Applications

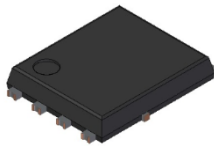
This new generation MOSFET features low on-resistance and fast switching, making it ideal for high-efficiency power-management applications.

- Power-management functions
- DC-DC converters
- Backlighting

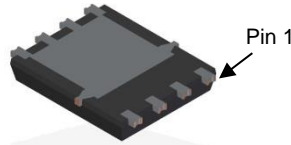
Mechanical Data

- Package: PowerDI5060-8
- Package Material: Molded Plastic, “Green” Molding Compound
UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram Below
- Terminals: Finish – Matte Tin Annealed over Copper Lead-Frame.
Solderable per MIL-STD-202, Method 208 Ⓔ3
- Weight: 0.097 grams (Approximate)

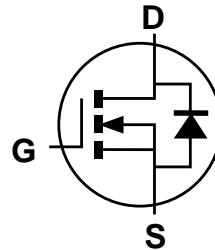
PowerDI5060-8/SWP (Type UX)



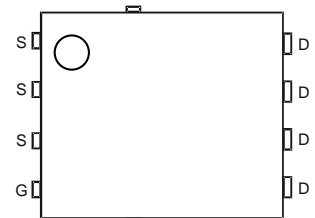
Top View



Bottom View



Internal Schematic



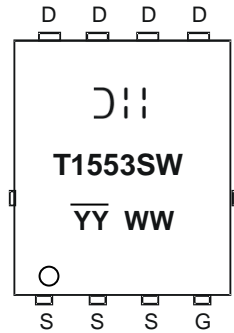
Top View
Pin Configuration


Ordering Information (Note 4)

Part Number	Package	Packing	
		Qty.	Carrier
DMT15H053SPSW-13	PowerDI5060-8/SWP (Type UX)	2,500	Tape & Reel

- Notes:
1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information



 = Manufacturer's Marking
 T1553SW = Product Type Marking Code
 YYWW = Date Code Marking
 YY = Last Two Digits of Year (ex: 23 = 2023)
 WW = Week Code (01 to 53)

Maximum Ratings (@ T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V _{DSS}	150	V
Gate-Source Voltage		V _{GSS}	±20	V
Continuous Drain Current V _{GS} = 10V (Note 5)	Steady State	I _D	T _C = +25°C	24
			T _C = +70°C	19
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)		I _{DM}	96	A
Maximum Continuous Body Diode Forward Current (Note 5)		I _S	24	A
Pulsed Body Diode Current (10µs Pulse, Duty Cycle = 1%)		I _{SM}	96	A
Avalanche Current, L = 1mH		I _{AS}	11.7	A
Avalanche Energy, L = 1mH		E _{AS}	68.4	mJ

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 6)	T _A = +25°C	P _D	1.9	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	R _{θJA}	65	°C/W
Total Power Dissipation (Note 7)	T _A = +25°C	P _D	3.3	W
Thermal Resistance, Junction to Ambient (Note 7)	Steady State	R _{θJA}	38	°C/W
Total Power Dissipation (Note 5)	T _C = +25°C	P _D	90	W
Thermal Resistance, Junction to Case (Note 5)		R _{θJC}	1.4	°C/W
Operating and Storage Temperature Range		T _J , T _{STG}	-55 to +150	°C

- Notes:
5. Thermal resistance from junction to soldering point (on the exposed drain pad).
 6. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
 7. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.

Electrical Characteristics (@ T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	B _V D _{SS}	150	—	—	V	V _{GS} = 0V, I _D = 10mA
Zero Gate Voltage Drain Current	I _{DSS}	—	—	1	μA	V _{DS} = 120V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	V _{GS(TH)}	2	3.2	4	V	V _{DS} = V _{GS} , I _D = 250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	46	66	mΩ	V _{GS} = 10V, I _D = 20A
Diode Forward Voltage	V _{SD}	—	0.9	1	V	V _{GS} = 0V, I _S = 20A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C _{iss}	—	814	—	pF	V _{DS} = 75V, V _{GS} = 0V f = 1MHz
Output Capacitance	C _{oss}	—	84	—		
Reverse Transfer Capacitance	C _{rss}	—	3.7	—		
Gate Resistance	R _g	—	0.6	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Total Gate Charge	Q _g	—	11.5	—	nC	V _{DS} = 75V, I _D = 4.1A V _{GS} = 10V
Gate-Source Charge	Q _{gs}	—	4.6	—		
Gate-Drain Charge	Q _{gd}	—	2.8	—		
Turn-On Delay Time	t _{D(ON)}	—	5.7	—	ns	V _{DS} = 75V, V _{GS} = 10V I _D = 4.1A, R _g = 6Ω
Turn-On Rise Time	t _r	—	17.7	—		
Turn-Off Delay Time	t _{D(OFF)}	—	15.7	—		
Turn-Off Fall Time	t _f	—	12.7	—		
Reverse Recovery Time	t _{RR}	—	47	—	ns	I _F = 4.1A, di/dt = 100A/μs
Reverse Recovery Charge	Q _{RR}	—	87	—	nC	

Notes: 8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to product testing.

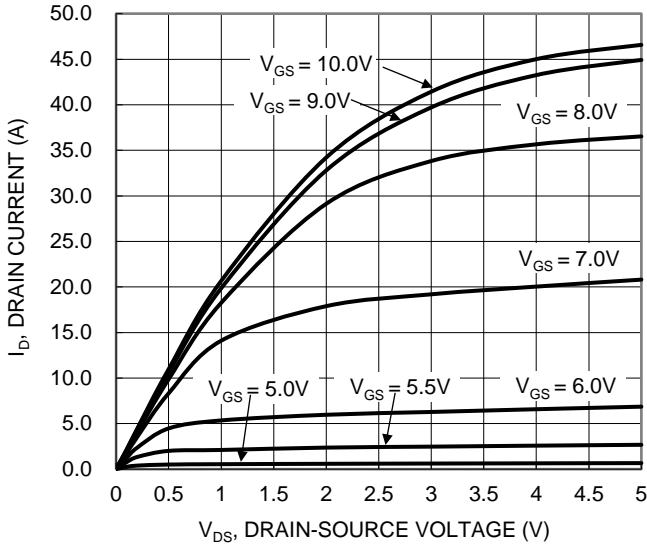


Figure 1. Typical Output Characteristic

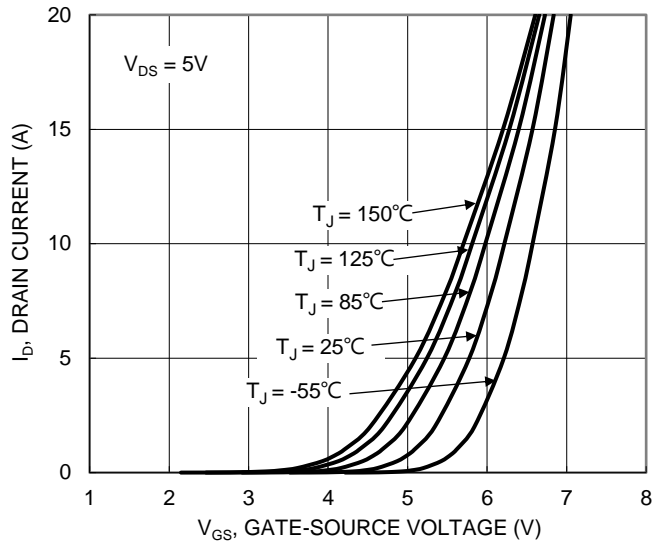


Figure 2. Typical Transfer Characteristic

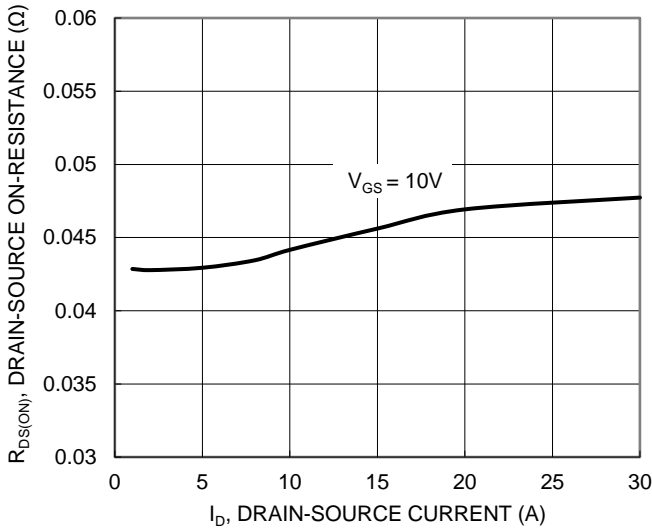


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

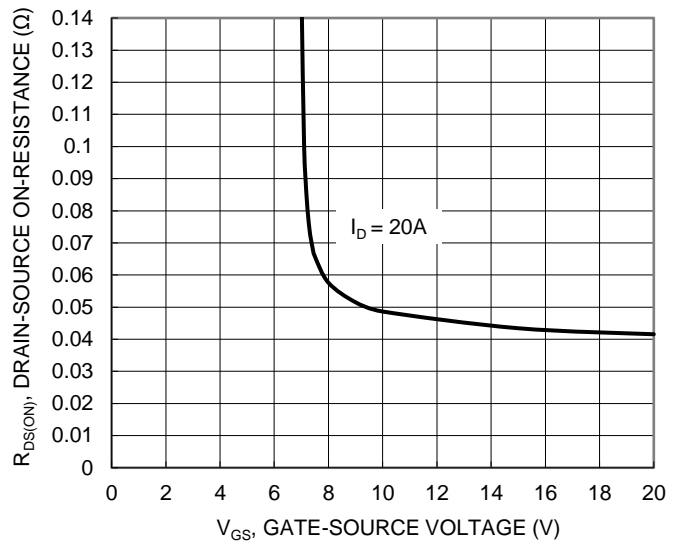


Figure 4. Typical Transfer Characteristic

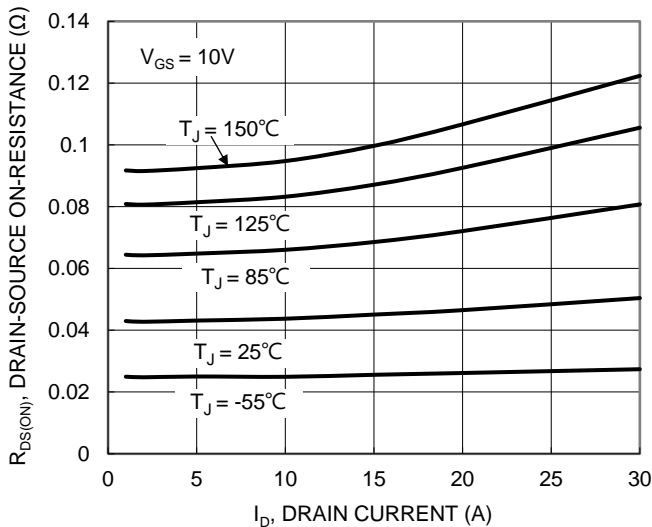


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

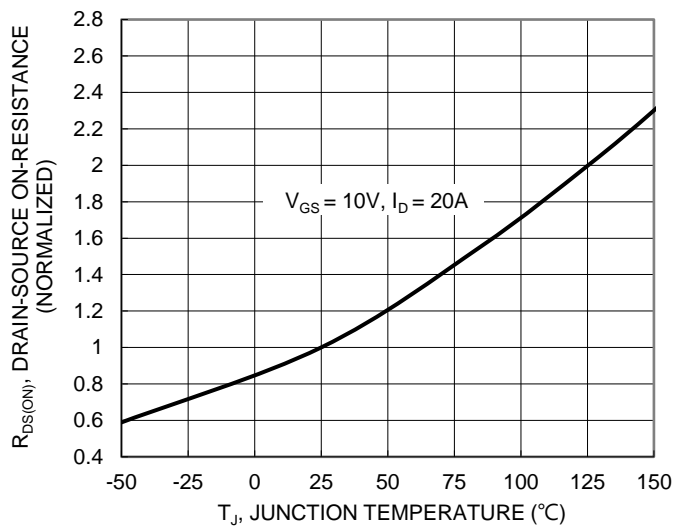


Figure 6. On-Resistance Variation with Junction Temperature

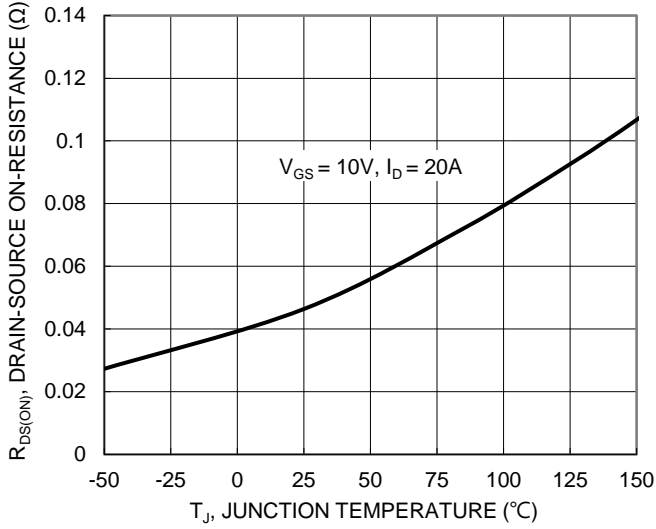


Figure 7. On-Resistance Variation with Junction Temperature

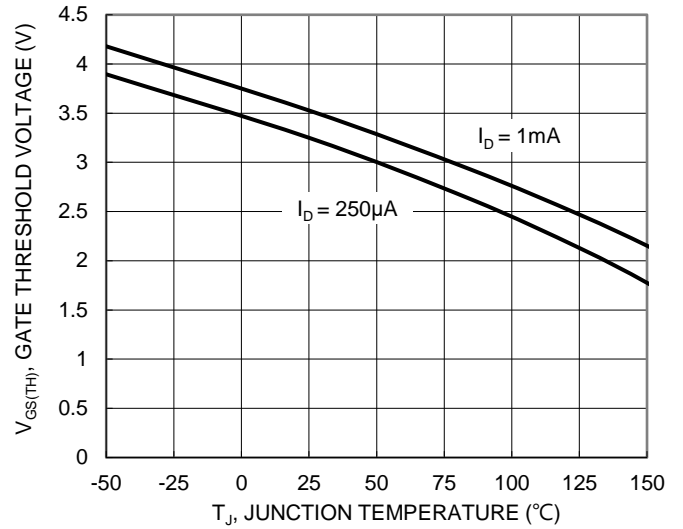


Figure 8. Gate Threshold Variation vs. Junction Temperature

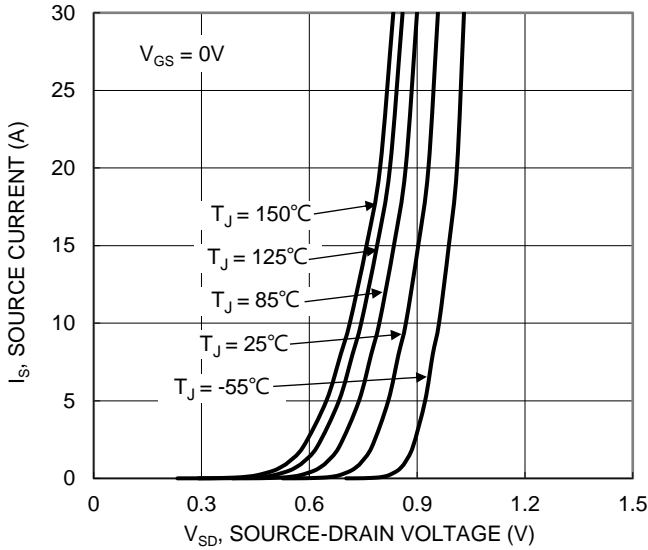


Figure 9. Diode Forward Voltage vs. Current

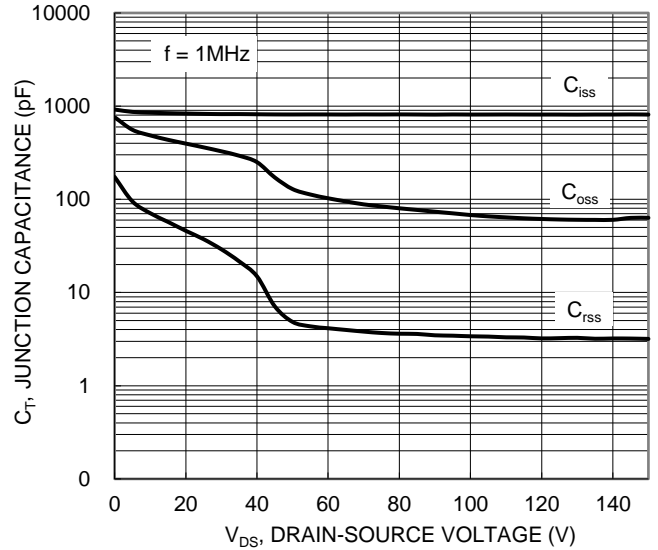


Figure 10. Typical Junction Capacitance

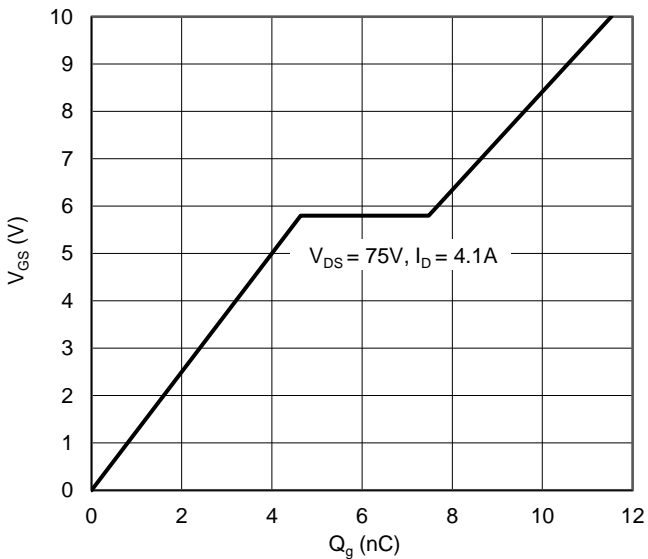


Figure 11. Gate Charge

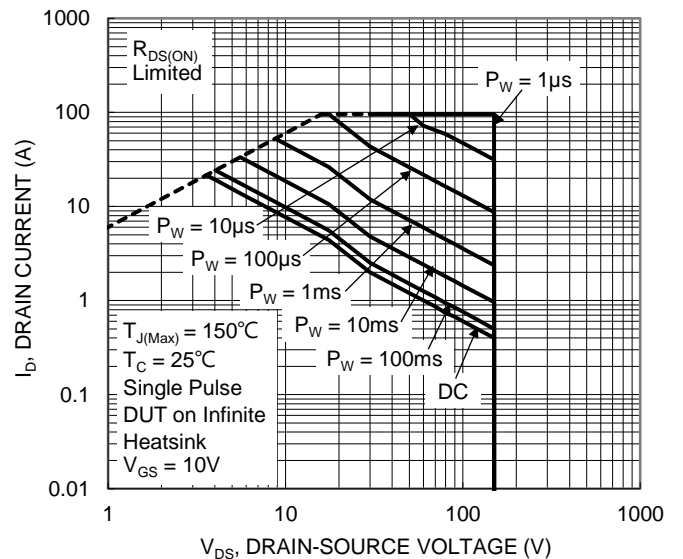


Figure 12. SOA, Safe Operation Area

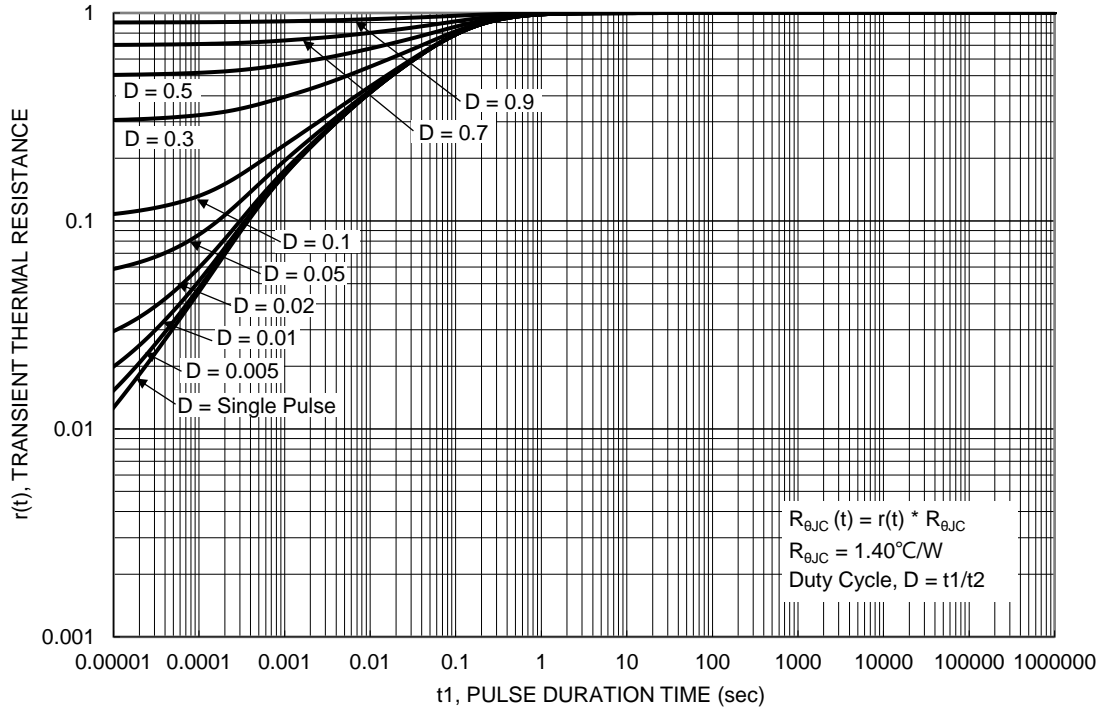
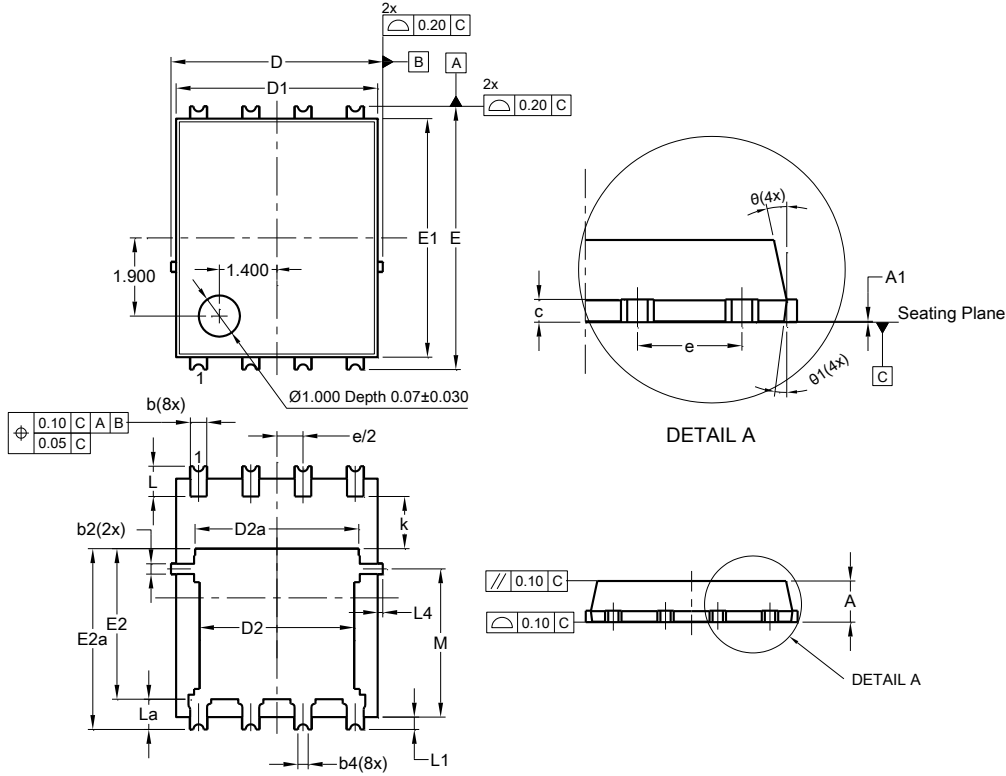


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

PowerDI5060-8/SWP (Type UX)

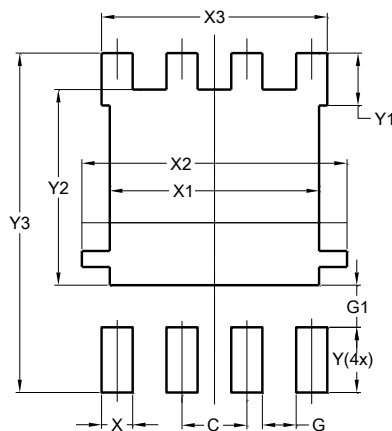


PowerDI5060-8/SWP (Type UX)			
Dim	Min	Max	Typ
A	0.90	1.10	1.00
A1	0	0.05	--
b	0.30	0.50	0.41
b2	0.20	0.35	0.25
b4	0.25REF		
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	3.56	3.96	3.76
D2a	3.78	4.18	3.98
E	6.40 BSC		
E1	5.60	6.00	5.80
E2	3.46	3.86	3.66
E2a	4.195	4.595	4.395
e	1.27BSC		
k	1.05	--	--
L	0.635	0.835	0.735
La	0.635	0.835	0.735
L1	0.200	0.400	0.300
L4	0.025	0.225	0.125
M	3.205	4.005	3.605
θ	10°	12°	11°
θ1	6°	8°	7°
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

PowerDI5060-8/SWP (Type UX)



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	4.100
X2	5.190
X3	4.420
Y	1.270
Y1	1.020
Y2	3.810
Y3	6.610

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