## 100V 175°C N-CHANNEL ENHANCEMENT MODE MOSFET

## Product Summary

| $BV_{DSS}$ | $R_{DS(ON)}$ Max | $I_D$ $T_C$ = +25°C |
|---|---|---|
| 100V | 30mΩ @ $V_{GS}$ = 10V | 28A |
| | 45mΩ @ $V_{GS}$ = 6.0V | 23A |

## Description

This new generation MOSFET features low on-resistance and fast switching, making it ideal for high efficiency power management applications.

## Applications

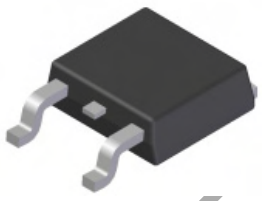
- Power Management Functions
- DC-DC Converters
- Backlighting

## Features

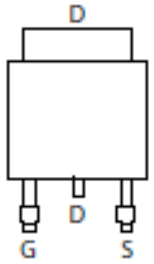
- Rated to +175°C – Ideal for High Ambient Temperature Environments
- 100% Unclamped Inductive Switching – Ensures More Reliable and Robust End Application
- Low $R_{DS(ON)}$ – Minimizes Power Losses
- Low $Q_G$ – Minimizes Switching Losses
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

## Mechanical Data

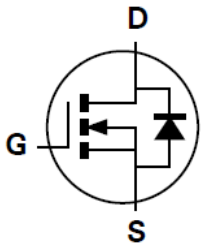
- Case: TO252 (DPAK)
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish – Matte Tin Annealed over Copper Leadframe Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.33 grams (Approximate)



Top View




Pin Out Top View



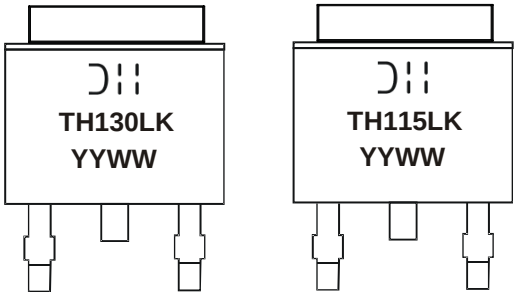

Equivalent Circuit

## Ordering Information (Note 4)

| Part Number | Case | Packaging |
|---|---|---|
| DMTH10H030LK3-13 | TO252 (DPAK) | 2,500/Tape & Reel |

Notes:
1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

## Marking Information




= Manufacturer's Marking
TH130LK or TH115LK = Product Type Marking Code
YYWW = Date Code Marking
YY = Last Two Digits of Year (ex: 17 = 2017)
WW = Week Code (01 to 53)

## Maximum Ratings (@$T_A$ = +25°C, unless otherwise specified.)

| Characteristic | | Symbol | Value | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DSS}$ | 100 | V |
| Gate-Source Voltage | | $V_{GSS}$ | ±20 | V |
| Continuous Drain Current, $V_{GS}$ = 10V | $T_C$ = +25°C<br>$T_C$ = +100°C | $I_D$ | 28<br>18 | A |
| Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%) | | $I_{DM}$ | 150 | A |
| Pulsed Body Diode Forward Current (10µs Pulse, Duty Cycle = 1%) | | $I_{SM}$ | 150 | A |
| Maximum Continuous Body Diode Forward Current (Note 6) | | $I_S$ | 2.6 | A |
| Avalanche Current, L = 3mH | | $I_{AS}$ | 7.5 | A |
| Avalanche Energy, L = 3mH | | $E_{AS}$ | 85 | mJ |

## Thermal Characteristics (@$T_A$ = +25°C, unless otherwise specified.)

| Characteristic | | Symbol | Value | Unit |
|---|---|---|---|---|
| Total Power Dissipation (Note 5) | | $P_D$ | 2.1 | W |
| Thermal Resistance, Junction to Ambient (Note 5) | Steady State | $R_{\theta JA}$ | 69 | °C/W |
| Total Power Dissipation (Note 6) | | $P_D$ | 3.5 | W |
| Thermal Resistance, Junction to Ambient (Note 6) | Steady State | $R_{\theta JA}$ | 42 | °C/W |
| Thermal Resistance, Junction to Case | | $R_{\theta JC}$ | 2 | |
| Operating and Storage Temperature Range | | $T_J$, $T_{STG}$ | -55 to +175 | °C |

## Electrical Characteristics (@$T_A$ = +25°C, unless otherwise specified.)

| Characteristic | Symbol | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** (Note 7) | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | 100 | — | — | V | $V_{GS}$ = 0V, $I_D$ = 1mA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | — | — | 1 | µA | $V_{DS}$ = 80V, $V_{GS}$ = 0V |
| Gate-Source Leakage | $I_{GSS}$ | — | — | ±100 | nA | $V_{GS}$ = ±20V, $V_{DS}$ = 0V |
| **ON CHARACTERISTICS** (Note 7) | | | | | | |
| Gate Threshold Voltage | $V_{GS(TH)}$ | 1.4 | — | 3.5 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 250µA |
| Static Drain-Source On-Resistance | $R_{DS(ON)}$ | — | — | 30 | mΩ | $V_{GS}$ = 10V, $I_D$ = 20A |
| | | — | — | 45 | | $V_{GS}$ = 6.0V, $I_D$ = 20A |
| Diode Forward Voltage | $V_{SD}$ | — | — | 1.3 | V | $V_{GS}$ = 0V, $I_S$ = 20A |
| **DYNAMIC CHARACTERISTICS** (Note 8) | | | | | | |
| Input Capacitance | $C_{iss}$ | — | 1,871 | — | pF | $V_{DS}$ = 50V, $V_{GS}$ = 0V<br>f = 1MHz |
| Output Capacitance | $C_{oss}$ | — | 261 | — | | |
| Reverse Transfer Capacitance | $C_{rss}$ | — | 6.9 | — | | |
| Gate Resistance | $R_G$ | — | 0.75 | — | Ω | $V_{DS}$ = 0V, $V_{GS}$ = 0V, f = 1MHz |
| Total Gate Charge | $Q_G$ | — | 33.3 | — | nC | $V_{DD}$ = 50V, $I_D$ = 10A,<br>$V_{GS}$ = 10V |
| Gate-Source Charge | $Q_{GS}$ | — | 6.9 | — | | |
| Gate-Drain Charge | $Q_{GD}$ | — | 5.1 | — | | |
| Turn-On Delay Time | $t_{D(ON)}$ | — | 6.5 | — | ns | $V_{DD}$ = 50V, $V_{GS}$ = 10V,<br>$I_D$ = 10A, $R_G$ = 6Ω |
| Turn-On Rise Time | $t_R$ | — | 7.0 | — | | |
| Turn-Off Delay Time | $t_{D(OFF)}$ | — | 19.7 | — | | |
| Turn-Off Fall Time | $t_F$ | — | 8.1 | — | | |
| Reverse Recovery Time | $t_{RR}$ | — | 37.9 | — | ns | $I_F$ = 10A, di/dt = 100A/µs |
| Reverse Recovery Charge | $Q_{RR}$ | — | 51.9 | — | nC | |

Notes:
5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

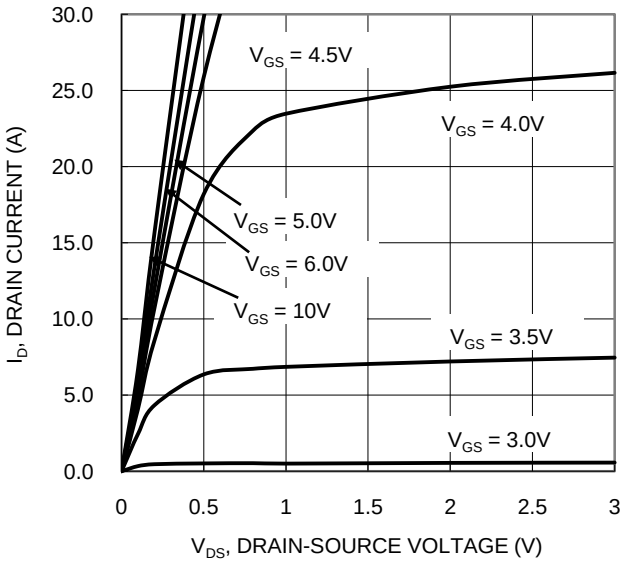



Figure 1. Typical Output Characteristic

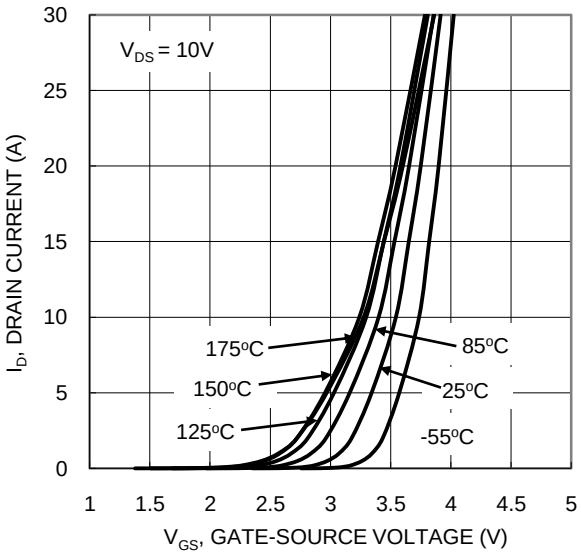



Figure 2. Typical Transfer Characteristic

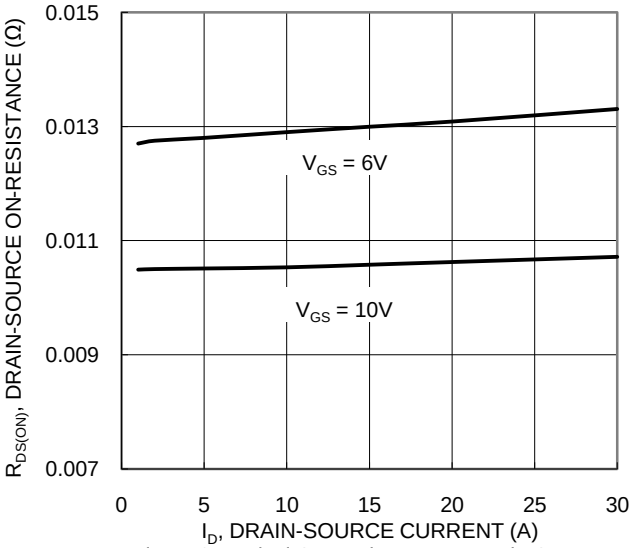



Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

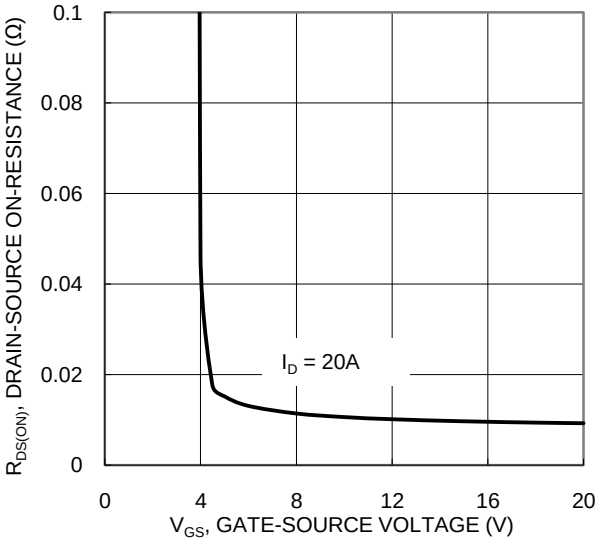



Figure 4. Typical Transfer Characteristic

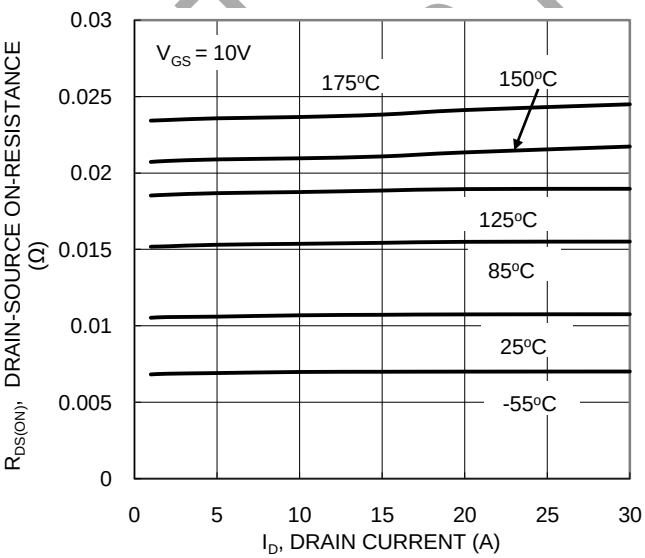



Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

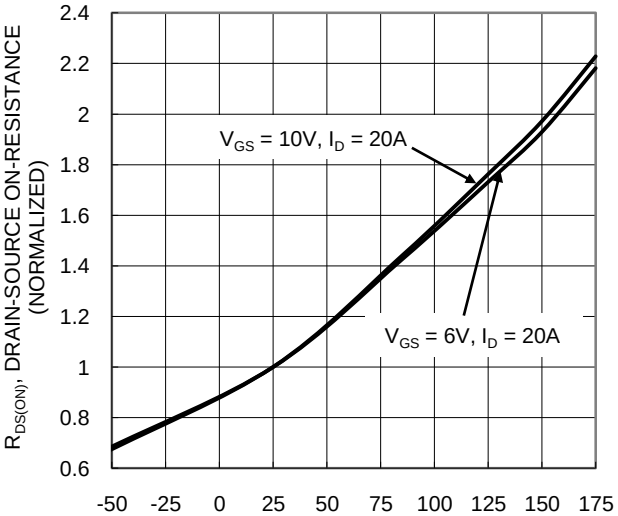



Figure 6. On-Resistance Variation with Junction Temperature

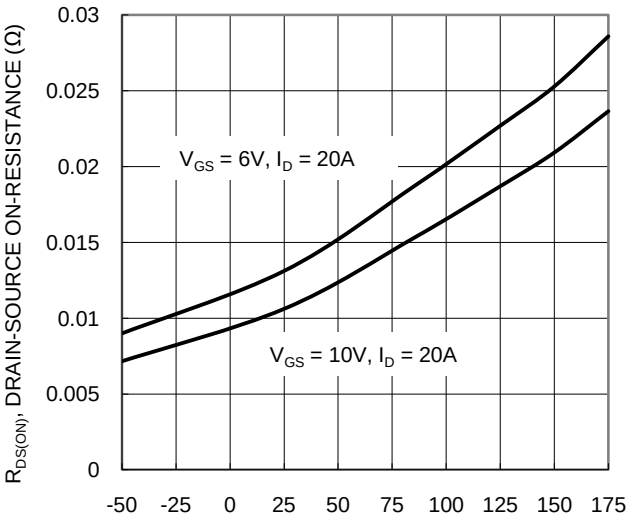



Figure 7. On-Resistance Variation with Junction Temperature

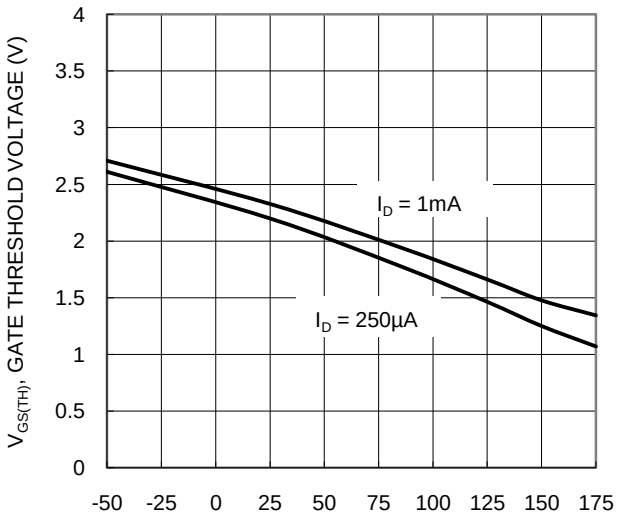



Figure 8. Gate Threshold Variation vs. Junction Temperature

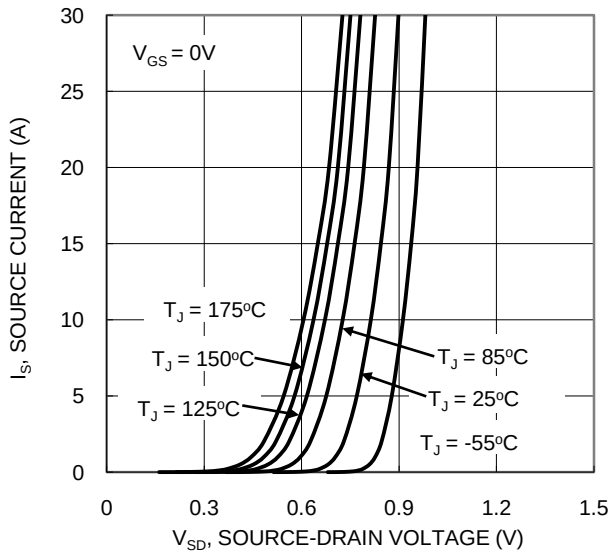



Figure 9. Diode Forward Voltage vs. Current

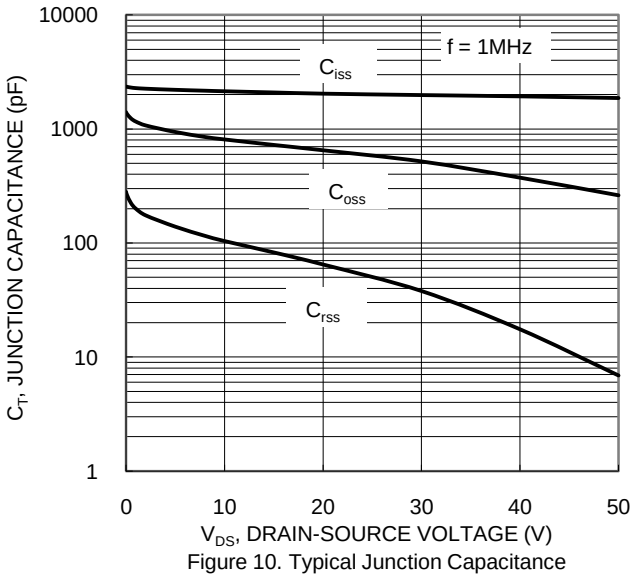



Figure 10. Typical Junction Capacitance

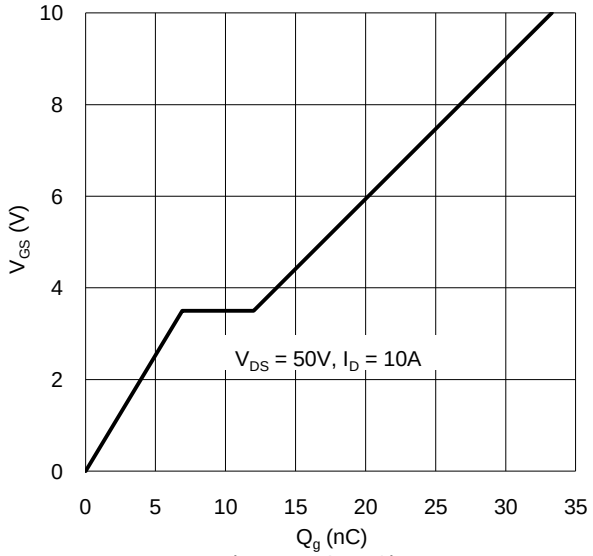



Figure 11. Gate Charge

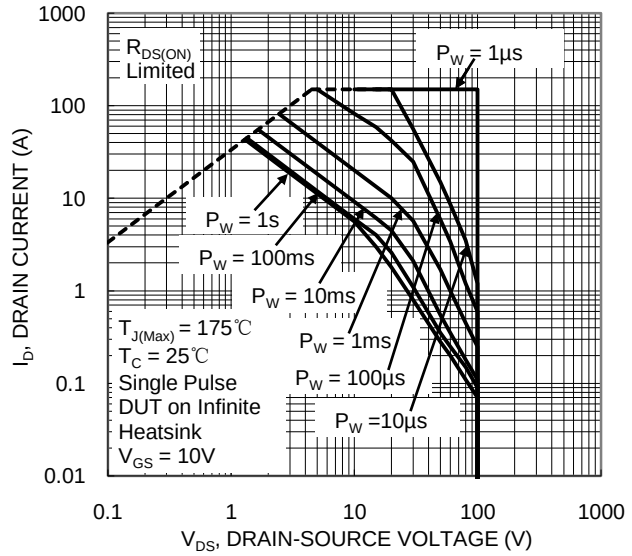



Figure 12. SOA, Safe Operation Area

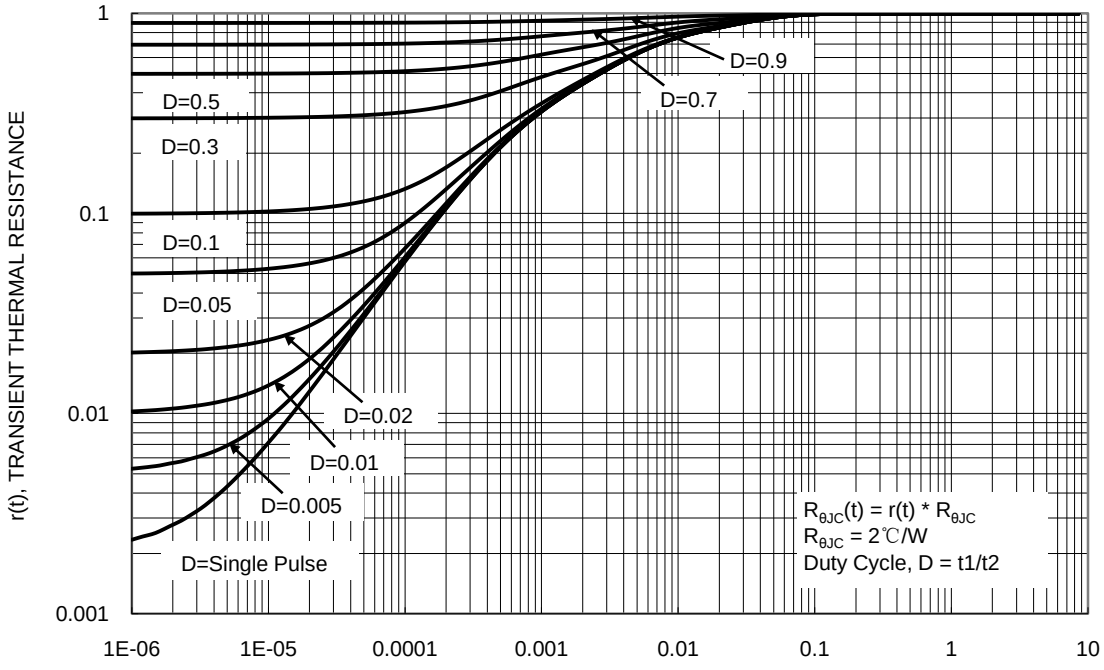
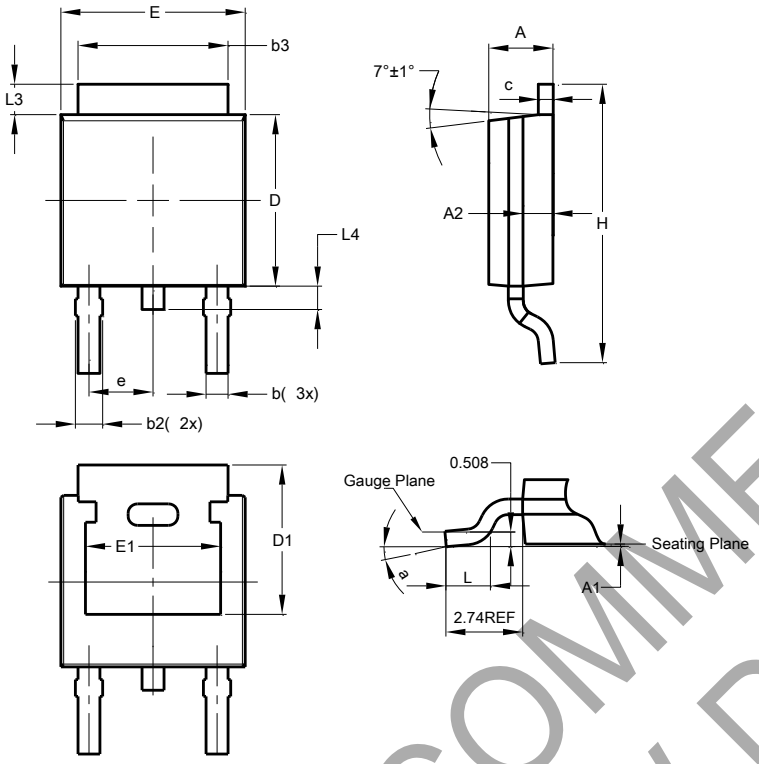



Figure 13. Transient Thermal Resistance

## Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

**TO252 (DPAK)**

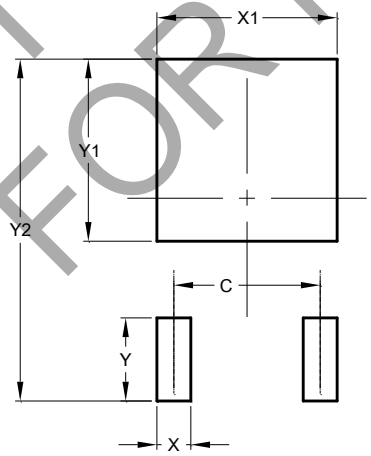



| TO252 (DPAK) | | | |
|---|---|---|---|
| Dim | Min | Max | Typ |
| A | 2.19 | 2.39 | 2.29 |
| A1 | 0.00 | 0.13 | 0.08 |
| A2 | 0.97 | 1.17 | 1.07 |
| b | 0.64 | 0.88 | 0.783 |
| b2 | 0.76 | 1.14 | 0.95 |
| b3 | 5.21 | 5.46 | 5.33 |
| c | 0.45 | 0.58 | 0.531 |
| D | 6.00 | 6.20 | 6.10 |
| D1 | 5.21 | - | - |
| e | - | - | 2.286 |
| E | 6.45 | 6.70 | 6.58 |
| E1 | 4.32 | - | - |
| H | 9.40 | 10.41 | 9.91 |
| L | 1.40 | 1.78 | 1.59 |
| L3 | 0.88 | 1.27 | 1.08 |
| L4 | 0.64 | 1.02 | 0.83 |
| a | 0° | 10° | - |
| All Dimensions in mm | | | |

## Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

**TO252 (DPAK)**




| Dimensions | Value (in mm) |
|---|---|
| C | 4.572 |
| X | 1.060 |
| X1 | 5.632 |
| Y | 2.600 |
| Y1 | 5.700 |
| Y2 | 10.700 |

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