4-CHANNEL LOW CAPACITANCE TVS DIODE ARRAY

Features

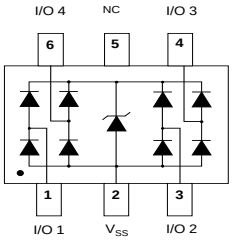
- Low Clamping Voltage
- Typical 9V at 10A 100ns, TLP
- Typical 9V at 10A 8μs/20μs
- IEC 61000-4-2 (ESD): Air – ±30kV, Contact – ±30kV
- IEC 61000-4-4 (EFT): 60A (5/50ns, I/O to V_{SS})
- IEC 61000-4-5 (Lightning): ±10A
- 4 Channels of ESD Protection
- Low Channel Input Capacitance of 1.2pF Typical
- TLP Dynamic Resistance: 0.25Ω
- Typically Used for High Speed Ports such as USB 2.0, IEEE 1394, LVDS, Ethernet 10/100M/1000M BASE-T Flat Panel Displays, Video Graphics Displays, SIM Ports
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The DT2042-04SOQ is suitable for automotive applications requiring specific change control; this part is AEC-Q101 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**
  https://www.diodes.com/quality/product-definitions/

Mechanical Data

- Package: SOT26
- Package Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Matte Tin Finish Annealed over Copper Leadframe (Lead Free Plating). Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.016 grams (Approximate)

SOT26

Top View



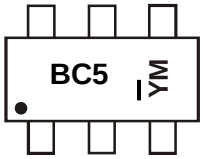
Device Schematic

Ordering Information (Note 4)

Part Number	Package	Marking	Reel Size (inches)	Tape Width (mm)	Packing	
					Qty.	Carrier
DT2042-04SOQ-7	SOT26	BC5	7	8	3,000	Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



BC5 = Product Type Marking Code
YM = Date Code Marking
Y = Year (ex: K = 2023)
M = Month (ex: 9 = September)

Date Code Key

Year	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034
Code	K	L	M	N	P	R	S	T	U	V	W	X

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	Conditions
Peak Pulse Current, per IEC 61000-4-5	I_{PP}	±10	A	I/O to V_{SS}, 8/20 µs
Peak Pulse Power, per IEC 61000-4-5	P_{PP}	105	W	I/O to V_{SS}, 8/20 µs
Operating Voltage (DC)	V_{DC}	5.5	V	I/O to V_{SS}
ESD Protection – Contact Discharge, per IEC61000-4-2	$V_{ESD\_contact}$	±30	kV	I/O to V_{SS}
ESD Protection – Air Discharge, per IEC 61000-4-2	V_{ESD_air}	±30	kV	I/O to V_{SS}
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C	—

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation Typical (Note 5)	P_D	300	mW
Thermal Resistance, Junction to Ambient Typical (Note 5)	$R_{\theta JA}$	417	°C/W

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Conditions
Reverse Working Voltage	V_{RWM}	—	—	5.5	V	I/O to V_{SS}
Reverse Current (Note 6)	I_R	—	—	1	µA	V_R = 5V, any I/O to V_{SS}
Reverse Breakdown Voltage	V_{BR}	6	—	9	V	I_R = 1mA, I/O to V_{SS}
Forward Clamping Voltage	V_F	-1.0	-0.8	—	V	I_F = -15mA, I/O to V_{SS}
Holding Voltage	V_H	5.5	—	—	V	—
Trigger Voltage	V_{TRIG}	—	9	9.5	V	—
Reverse Clamping Voltage (Note 7)	V_{C_5A}	—	7.5	—	V	I_{PP} = 5A, I/O to V_{SS}, 8/20 µs
Reverse Clamping Voltage (Note 7)	V_{C_10A}	—	9	10.5	V	I_{PP} = 10A, I/O to V_{SS}, 8/20 µs
ESD Clamping Voltage (Note 8)	V_{ESD}	—	9	—	V	TLP, 10A, tp = 100ns, I/O to V_{SS}, per Figure 7
Dynamic Resistance (Note 8)	R_{DIF}	—	0.25	—	Ω	TLP, 10A, tp = 100ns, I/O to V_{SS}
Channel Input Capacitance	$C_{I/O}$	—	1.2	1.5	pF	V_R = 2.5V, f = 1MHz

Notes:
5. Device mounted on FR-4 PCB pad layout (2oz copper) as shown on Diodes Incorporated's suggested pad layout, which can be found on our website at http://www.diodes.com.
6. Short duration pulse test used to minimize self-heating effect.
7. Clamping voltage value is based on an 8x20µs peak pulse current (I_{pp}) waveform.
8. Transmission Line Pulse (TLP) test settings: t_P = 100ns, t_R = 10ns, I_{TLP} and V_{TLP} averaging window is from 70ns to 90ns.

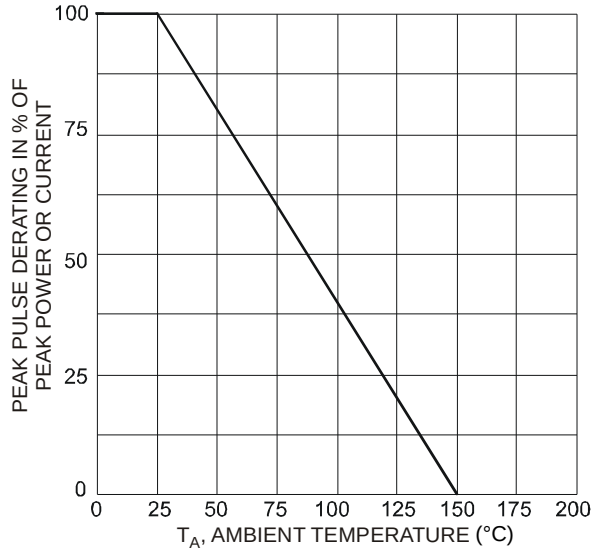


Figure 1 Pulse Derating Curve

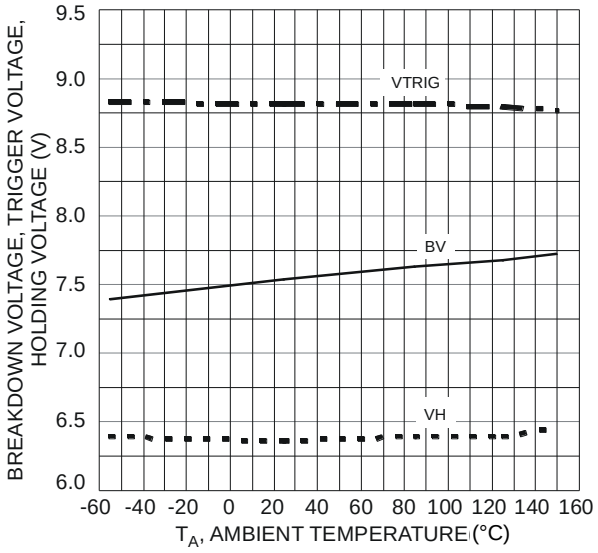


Figure 2 BV, Trigger Voltage, Holding Voltage vs. Ambient Temperature

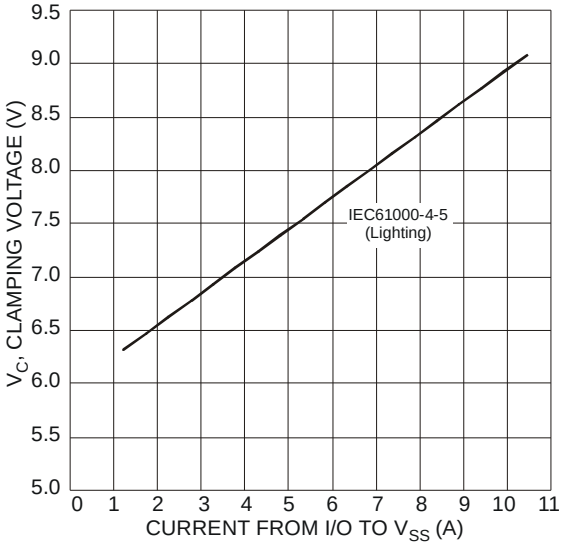


Figure 3 Clamping Voltage Characteristic

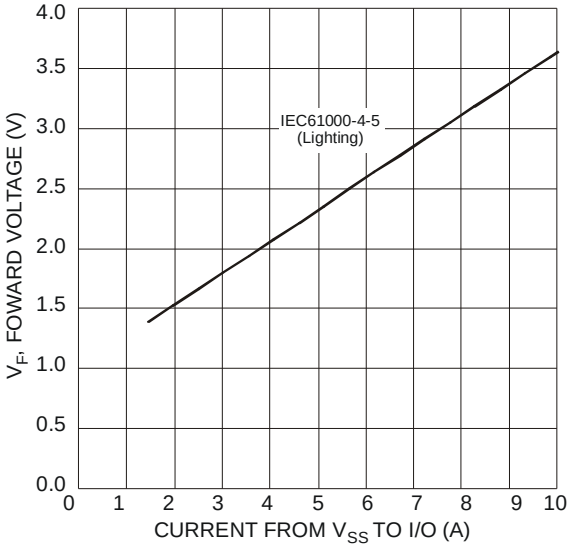


Figure 4 Forward Voltage Characteristic

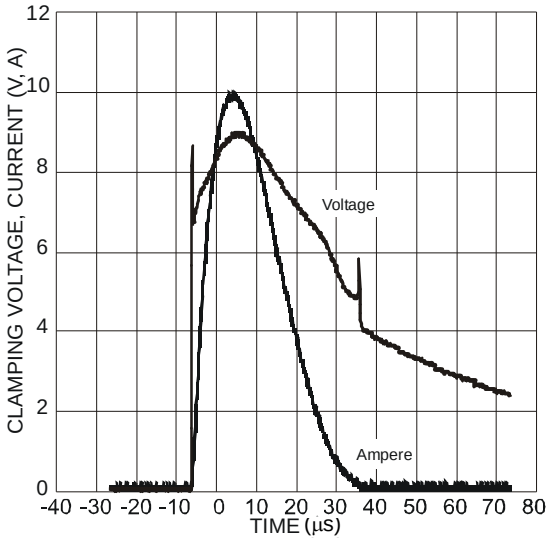


Figure 5 Waveform of Clamping Voltage, Current vs. Time (8/20µs, I/O to V_{SS})

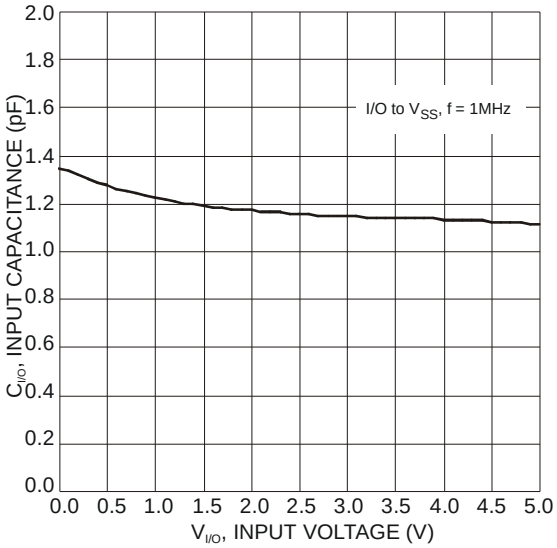


Figure 6 Input Capacitance vs. Input Voltage

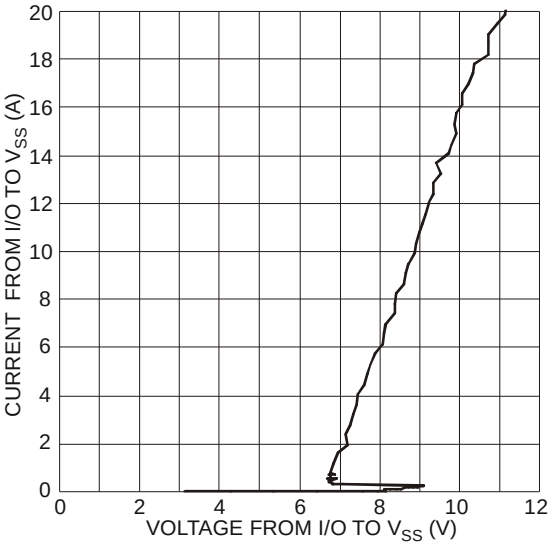


Figure 7 Current vs. Voltage

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

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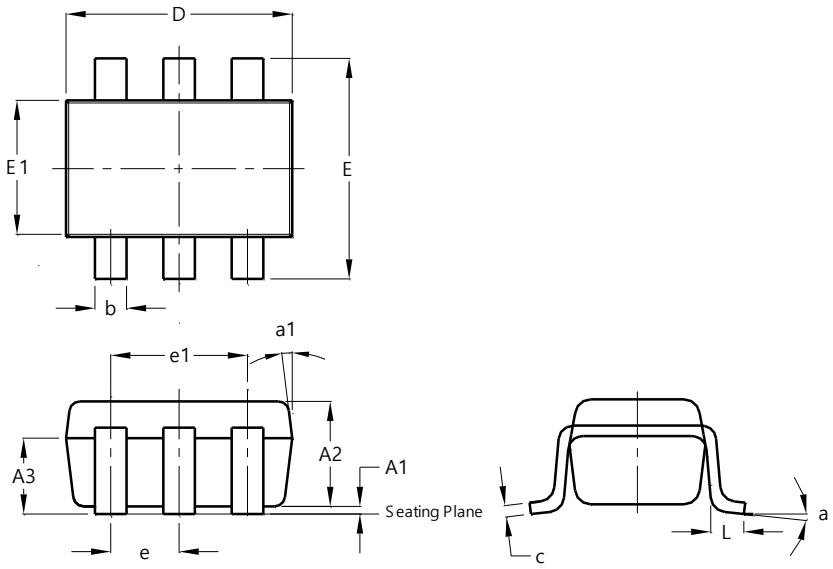
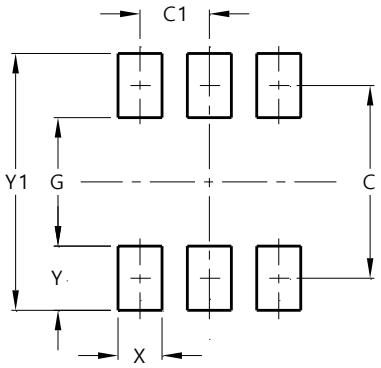


SOT26			
Dim	**Min**	**Max**	**Typ**
A1	0.013	0.10	0.05
A2	1.00	1.30	1.10
A3	0.70	0.80	0.75
b	0.35	0.50	0.38
c	0.10	0.20	0.15
D	2.90	3.10	3.00
e	-	-	0.95
e1	-	-	1.90
E	2.70	3.00	2.80
E1	1.50	1.70	1.60
L	0.35	0.55	0.40
a	-	-	8°
a1	-	-	7°
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT26



Dimensions	Value (in mm)
C	2.40
C1	0.95
G	1.60
X	0.55
Y	0.80
Y1	3.20

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