PERICOM®

PI3EQX1204-B

12.5Gbps 4-channel SAS3 ReDriver™ with Equalization, De-emphasis & Pre-shoot

Features

- Support up to 12.5Gbps serial link
- Support SATA Gen1/Gen2/Gen3 and SAS2/3 protocol
- Supporting 4 differential channels
- Independent channel configuration of receiver equalization, output swing and pre-shoot/de-emphasis
- Per Channel Activity Detector with selectable input termination between 50Ω to V_{CC} and 200KΩ to V_{CC}
- Pin strap and I^2C selectable device programming
- 3-bit selectable address bit for I^2C
- Supply Voltage: 3.3V±0.3V
- Industrial Temperature Range: -40°C to 85°C
- Packaging (Pb-free & Green):
  - 42-contact TQFN (9mm x3.5mm)

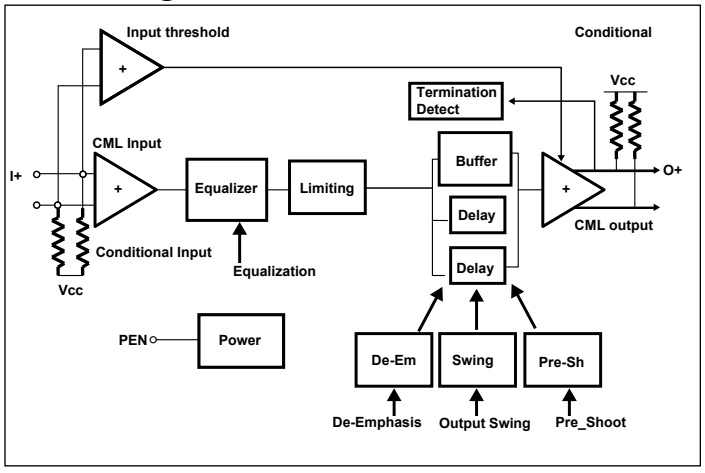
Description

Pericom Semiconductor's PI3EQX1204-B is a SAS3/10Gigabit Ethernet, 4 differential channels ReDriver™. The device provides programmable equalization, output swing, pre-shoot, and de-emphasis by either pin strapping option or I^2C Control, to optimize performance over a variety of physical mediums by reducing Inter-symbol interference.

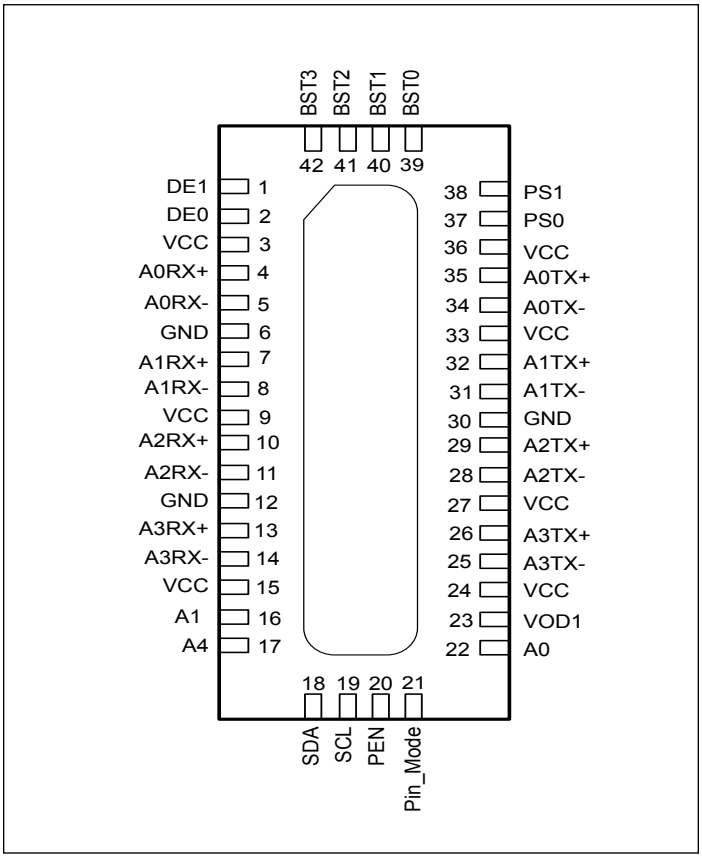
PI3EQX1204-B supports four 100-Ohm Differential CML data I/O's and extends the signals across other distant data pathways on the user's platform.

The integrated equalization circuitry provides flexibility with signal integrity of the signal before the ReDriver, whereas the integrated de-emphasis and pre-shoot circuitry provides flexibility with signal integrity of the signal after the ReDriver.

Block Diagram



Pin Configuration (Top-Side View)



Pin Description

Pin #	Pin Name	Type	Description
Data Signals			
4 5	A0RX+ A0RX-	I I	CML inputs for Channel A0, with internal 50-Ohm pull-up and ~200k-Ohm pull-up otherwise.
35 34	A0TX+, A0TX-	O O	CML outputs for Channel A0, with internal 50-Ohm pull-up and ~2k-Ohm pull-up otherwise.
7 8	A1RX+, A1RX-	I I	CML inputs for Channel A1, with internal 50-Ohm pull-up and ~200k-Ohm pull-up otherwise.
32 31	A1TX+, A1TX-	O O	CML outputs for Channel A1, with internal 50-Ohm pull-up and ~2k-Ohm pull-up otherwise.
10 11	A2RX+, A2RX-	I I	CML inputs for Channel A2, with internal 50-Ohm pull-up and ~200k-Ohm pull-up otherwise.
29 28	A2TX+, A2TX-	O O	CML outputs for Channel A2, with internal 50-Ohm pull-up and ~2k-Ohm pull-up otherwise.
13 14	A3RX+, A3RX-	I I	CML inputs for Channel A3, with internal 50-Ohm pull-up and ~200k-Ohm pull-up otherwise.
26 25	A3TX+, A3TX-	O O	CML outputs for Channel A3, with internal 50-Ohm pull-up and ~2k-Ohm pull-up otherwise.
Control Signals			
19	SCL	I	I^2C SCL clock input.
18	SDA	I/O	I^2C SDA data input/output.
17, 16, 22	A4, A1, A0	I	I^2C programmable address bits, with internal 100k-Ohm pull-up.
20	PEN	I	Power Enable with internal 100k-Ohm pull-up
21	Pin_Mode	I	Input with internal 100k-Ohm pull-up. When HIGH, each channel is programmed by the external pin voltage. When LOW, each channel is programmed by the data stored in the I^2C bus.
42, 41, 40, 39	BST[3:0]	I	Inputs with internal 100k-Ohm pull-up. This pins set the amount of Equalizer Boost in all channel when Pin_mode is HIGH.
23	VOD1	I	Inputs with internal 100k-Ohm pull-up. This pin sets the output Voltage Level in all channel when Pin_mode is HIGH.
1, 2	DE[1:0]	I	Inputs with internal 100k-Ohm pull-up. This pins set the output De-Emphasis Level in all channel when Pin_mode is HIGH.
38, 37	PS[1:0]	I	Inputs with internal 100k-Ohm pull-up. This pins set the output Pre-Shoot Level in all channel when Pin_mode is HIGH.
Power Pins			
6, 12, 30, Center Pad	GND	PWR	Supply GND
3, 9, 15, 24, 27, 33, 36	V_{CC}	PWR	3.3V ± 0.3V Supply Voltage

Description of Operation

Output Termination Detector:

On power up or when PEN becomes true, the output resistance is set to 2K ohms, and the input resistance is set to 200K ohms. The device continually looks to detect an external 50 ohm termination resistor on a per channel basis. If no 50 ohms is detected in the first 5ms of time, the channel is continually polled with 5ms detection cycle until detection occurs.

Input Activity Detector:

When the input voltage on individual channel basis falls below de-assert threshhold VTH-, the output is driven to the common mode voltage so as to eliminate output chatter. When the input voltage is higher than assert threshhold VTH+, the channel is resumed immediately.

Power Enable function: One pin control or I2C control, when PEN is set to low, the IC goes into power down mode, both input and output termination set to 200K and 2K respectively. Individual Channel Enabling is done through the I2C register programming.

Equalization Setting:

BST[3:0] are the selection pins for the equalization selection for each channel.

Table 1. Equalization Setting

Equalizer setting							
BST3	**BST2**	**BST1**	**BST0**	**@ 8GHz**	**@ 6.5GHz**	**@ 4GHz**	**@ 2.5GHz**
0	0	0	0	0.7 dB	0.64 dB	0.4 dB	0.2 dB
0	0	0	1	2.4 dB	2.0 dB	1.1 dB	0.6 dB
0	0	1	0	3.3 dB	2.7 dB	1.6 dB	0.8 dB
0	0	1	1	5.7 dB	4.9 dB	3.1 dB	1.8 dB
0	1	0	0	8.8 dB	7.8 dB	5.4 dB	3.3 dB
0	1	0	1	13.0 dB	11.8 dB	8.9 dB	6.1 dB
0	1	1	0	15.0 dB	13.8 dB	10.8 dB	7.8 dB
0	1	1	1	16.6 dB	15.4 dB	12.2 dB	9.1 dB
1	0	0	0	18.3 dB	17.1 dB	13.8 dB	10.6 dB
1	0	0	1	20.3 dB	19.0 dB	15.8 dB	12.6 dB
1	0	1	0	21.8 dB	20.6 dB	17.3 dB	14.0 dB
1	0	1	1	23.5 dB	22.2 dB	19.0 dB	15.6 dB
1	1	0	0	24.7 dB	23.4 dB	20.0 dB	16.5 dB
1	1	0	1	26.1 dB	24.7 dB	21.3 dB	17.8 dB
1	1	1	0	27.4 dB	26.0 dB	22.6 dB	19.1 dB
1	1	1	1	28.8 dB	27.6 dB	24.3 dB	20.8 dB

De-emphasis Setting:

De-emphasis Setting: DE[1:0] are the selection bits for the de-emphasis value.

Table 2. Output De-emphasis Setting

Output de-emphasis setting		
DE1	**DE0**	**@ VOD1 = 0**
0	0	0dB
0	1	3.5dB
1	0	6dB
1	1	9.5dB

Pre-Shoot Settings:

Pre-shoot Setting: PS[1:0] are the selection bits for the pre-shoot value.

Table 3. Pre-Shoot Setting

Output pre-shoot setting		
PS1	**PS0**	**@ VOD1 = 0**
0	0	0dB
0	1	1.6dB
1	0	3.5dB
1	1	6dB

Combined Pre-Shoot and De-emphasis Settings should be followed based on the table below.

		De-emphasis setting DE[1:0]			
	PS/DE	**00**	**01**	**10**	**11**
Pre-shoot setting PS[1:0]	00	0.0/0.0	0.0/-3.5	0.0/-6.0	0.0/-9.5
	01	1.6/0.0	3.5/-3.5	3.5/-6.0	NA
	10	3.5/0.0	6.0/-6.0	NA	NA
	11	6.0/0.0	NA	NA	NA

Swing Setting:

Swing Setting: VOD[1:0] are the selection bits for the output swing value.

Table 4. Swing Setting

VOD1	VOD0	Swing
0	0	0.8Vppd
0	1	0.95Vppd
1	0	1.15Vppd
1	1	1.3Vppd

Note: Posssible output swings in Pin strap mode are 0.95Vppd and 1.3Vppd.

Activity Detector Threshold:

Threshold Setting: VTH[1:0] are the selection bits for the activity detector threshhold.

Table 5. Activity Detector Threshold Setting

VTH1	VTH0	VTH+ (Assert threshhold), mVppd	VTH- (De-assert threshhold), mVppd
0	0	130	30
0	1	150	50
1	0	170	70
1	1	210	110

I²C Programming

Address assignment							
A6	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**R/W**
1	1	Program	0	0	Program	Program	1=R, 0=W

BYTE 0				
Bit	**Type**	**Power up condition**	**Control affected**	**Comment**
7	R		Ch3 Activity Detector	1= Activity 0=no activity
6	R		Ch2 Activity Detector	
5	R		Ch1 Activity Detector	
4	R		Ch0 Activity Detector	
3	R	0	Not used	
2	R	0	Not used	
1	R	0	Not used	
0	R	0	Not used	
BYTE 1				
Bit	**Type**	**Power up condition**	**Control affected**	**Comment**
[7:0]	R	0	Not used	
BYTE 2				
Bit	**Type**	**Power up condition**	**Control affected**	**Comment**
7	R/W	Latch from PEN input at startup	Ch3 Enable	1 = Enable
6	R/W		Ch2 Enable	
5	R/W		Ch1 Enable	
4	R/W		Ch0 Enable	
3	R/W	0	Not used	
2	R/W	0	Not used	
1	R/W	0	Not used	
0	R/W	0	Not used	

I²C Programming cont..

BYTE 3				
Bit	**Type**	**Power up condition**	**Control affected**	Comment
7	R/W	Latch from BST<3:0> at startup	BST3 Ch1	Refer to Table 1 RX EQ Setting
6	R/W		BST2 Ch1	
5	R/W		BST1 Ch1	
4	R/W		BST0 Ch1	
3	R/W		BST3 Ch0	
2	R/W		BST2 Ch0	
1	R/W		BST1 Ch0	
0	R/W		BST0 Ch0	
BYTE 4				
Bit	**Type**	**Power up condition**	**Control affected**	Comment
7	R/W	Latch from BST<3:0> at startup	BST3 Ch3	Refer to Table 1 RX EQ Setting
6	R/W		BST2 Ch3	
5	R/W		BST1 Ch3	
4	R/W		BST0 Ch3	
3	R/W		BST3 Ch2	
2	R/W		BST2 Ch2	
1	R/W		BST1 Ch2	
0	R/W		BST0 Ch2	
BYTE 5				
Bit	**Type**	**Power up condition**	**Control affected**	Comment
7	R/W	Latch from VOD1 at startup	VOD1 Ch3	Refer to Table 4 Output Swing Setting
6	R/W	VOD0 = 1	VOD0 Ch3	
5	R/W	Latch from VOD1 at startup	VOD1 Ch2	
4	R/W	VOD0 = 1	VOD0 Ch2	
3	R/W	Latch from VOD1 at startup	VOD1 Ch1	
2	R/W	VOD0 = 1	VOD0 Ch1	
1	R/W	Latch from VOD1 at startup	VOD1 Ch0	
0	R/W	VOD0 = 1	VOD0 Ch0	

I²C Programming cont..

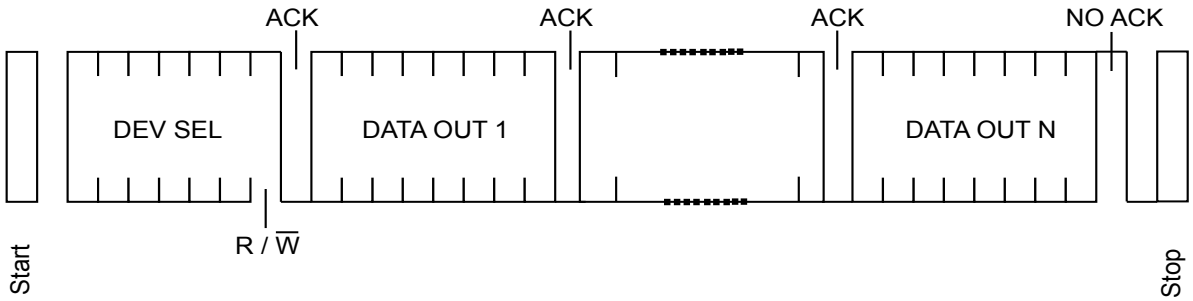
BYTE 6				
Bit	**Type**	**Power up condition**	**Control affected**	Comment
7	R/W	Latch from DE<1:0> at startup	DE1 Ch3	Refer to Table 2 De-emphasis Setting
6	R/W		DE0 Ch3	
5	R/W		DE1 Ch2	
4	R/W		DE0 Ch2	
3	R/W		DE1 Ch1	
2	R/W		DE0 Ch1	
1	R/W		DE1 Ch0	
0	R/W		DE0 Ch0	
BYTE 7				
Bit	**Type**	**Power up condition**	**Control affected**	Comment
7	R/W	Latch from PS<1:0> at startup	PS1 Ch3	Refer to Table 3 Pre-shoot Setting
6	R/W		PS0 Ch3	
5	R/W		PS1 Ch2	
4	R/W		PS0 Ch2	
3	R/W		PS1 Ch1	
2	R/W		PS0 Ch1	
1	R/W		PS1 Ch0	
0	R/W		PS0 Ch0	
BYTE 8				
Bit	**Type**	**Power up condition**	**Control affected**	Comment
7	R/W	1	Ch3 RX detect	1 = inactive 0 = active
6	R/W	1	Ch2 RX detect	
5	R/W	1	Ch1 RX detect	
4	R/W	1	Ch0 RX detect	
3	R/W	0	Ch3 RX reset	1=reset
2	R/W	0	Ch2 RX reset	
1	R/W	0	Ch1 RX reset	
0	R/W	0	Ch0 RX reset	

I²C Programming cont..

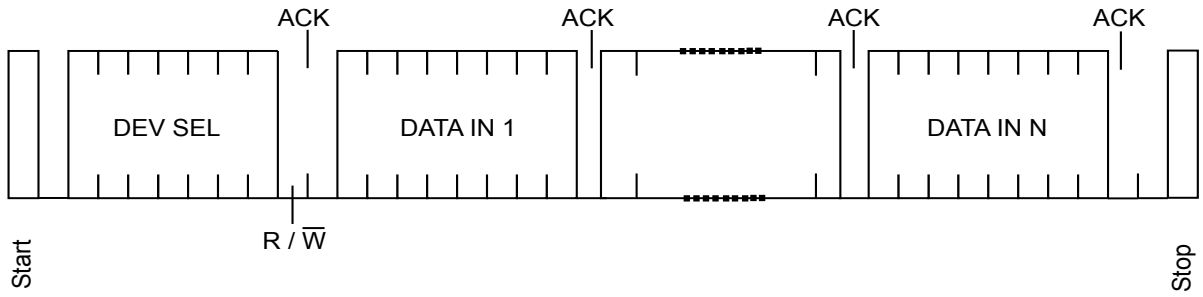
BYTE 9				
Bit	**Type**	**Power up condition**	**Control affected**	Comment
7	R/W	0	Ch3 Activity Detector Enable	1=inactive
6	R/W	0	Ch2 Activity Detector Enable	
5	R/W	0	Ch1 Activity Detector Enable	
4	R/W	0	Ch0 Activity Detector Enable	
3	R/W	0	Not use	
2	R/W	0	Not use	
1	R/W	0	Not use	
0	R/W	0	Not use	
BYTE 10				
Bit	**Type**	**Power up condition**	**Control affected**	Comment
7	R/W	0	Ch3 Activity Detector Threshold VTH1	Refer to Table 5
6	R/W	0	Ch3 Activity Detector ThresholdVTH0	
5	R/W	0	Ch2 Activity Detector ThresholdVTH1	
4	R/W	0	Ch2 Activity Detector ThresholdVTH0	
3	R/W	0	Ch1 Activity Detector ThresholdVTH1	
2	R/W	0	Ch1 Activity Detector ThresholdVTH0	
1	R/W	0	Ch0 Activity Detector ThresholdVTH1	
0	R/W	0	Ch0 Activity Detector ThresholdVTH0	
BYTE 11-15 - RESERVED				

I²C Data Transfer

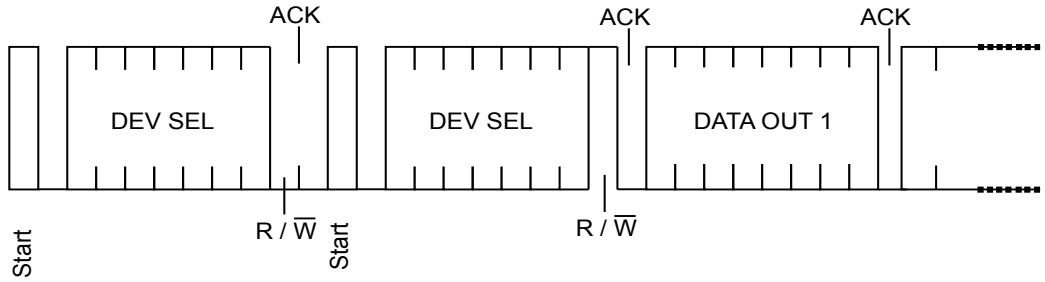
1.Read Sequence

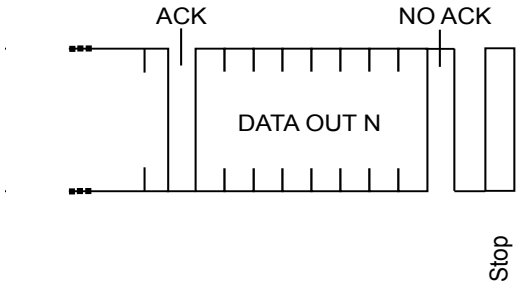


2.Write Sequence



3.Combined Sequence





Notes:

1.Only block read and block write from the lowest byte are supported for this application.

2.For some I2C application, an offset address byte will be presented at the second byte in write command, which is called dummy byte here and will be simply ignored in this application for correct interoperation.

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C
Supply Voltage to Ground Potential ..... –0.5V to +4.6V
DC SIG Voltage ..... –0.5V to V_{CC}+0.5V
Current Output ..... –25mA to +25mA
Power Dissipation Continuous 2.1W
Operating Temperature ..... -40 to +85°C
ESD, HBM ..... –2kV to +2kV
ESD, CDM ..... –500V to +500V

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Common Specification:

(V_{CC} = 3.3 ± 0.3V, T_A = -40 to 85°C)

Pwer and Current Consumption

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
VCC	Power supply voltage			3.3	3.6	V
P_{max}	Max Supply power	PEN=1			1.26	W
Imax	Max Supply current				350	mA
P_{idle}	Supply power	PEN=0			3	mW

Inputs DC Specifications

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{IH}	DC input logic high		V_{CC}/2 + 0.7	V_{CC} + 0.3	V
V_{IL}	DC input logic low		-0.3	V_{CC}/2 - 0.7	V

SAC/DC Specifications - SCL/SDA for I2C BUS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	DC input logic high		V_{DD}/2+0.7		V_{DD}+0.3	V
V_{IL}	DC input logic low		-0.3		V_{DD}/2-0.7	V
V_{OL}	DC output logic low	I_{OL}=3mA			0.4	V
Ipullup	"Current Through Pull-Up Resistor or Current Source"	High Power specification	4			mA
V_{DD}	Nominal Bus Voltage		3.0		3.6	V
Ileak-bus	Input leakage per bus segment		-200		200	uA
Ileak-pin	Input leakage per device pin			-15		uA
CI	Capacitance for SDA/SCL				10	pF
Freq	Bus Operation Frequency				400k	Hz
TBUF	"Bus Free Time Between Stop and Start condition"		1.3			us

THD:STA	Hold time after (Repeated) Start condition. After this period, the first clock is generated.	At Ipull-up, Max	0.6			us
TSU:STA	Repeated start conidtion setup time		0.6			us
TSU:STO	Stop condition setup time		0.6			us
THD:DAT	Data hold time		0			ns
TSU:DAT	Data setup time		100			ns
Tlow	Clock low period		1.3			us
Thigh	Clock high period		0.6		50	us
tF	Clock/Data fall time				300	ns
tR	Clock/Data rise time				300	ns
tpor	"Time in which a device must be operation after power-on reset"				500	ms

Note: (1) Recommended value.

(2) Recommended maximum capacitance load per bus segment is 400pF.

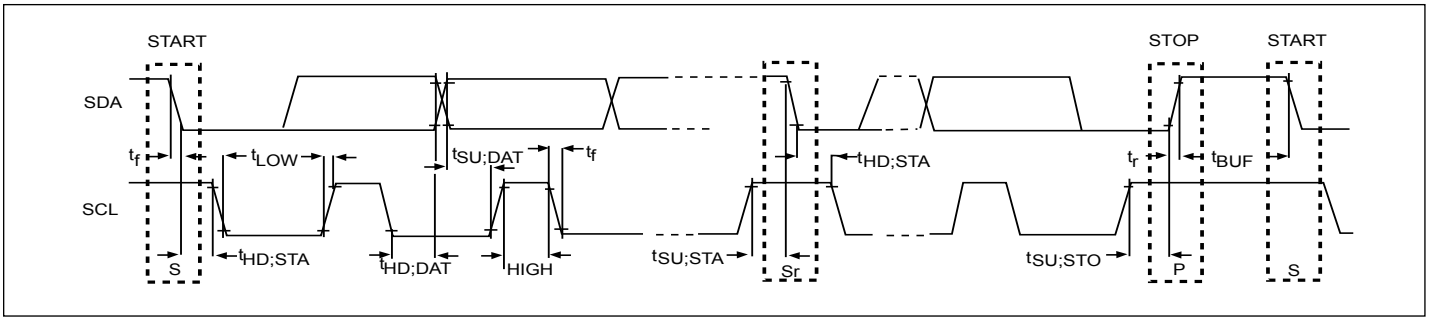
(3) Compliant to I2C physical layer specification.

(4) Ensured by Design. Parameter not tested in production.

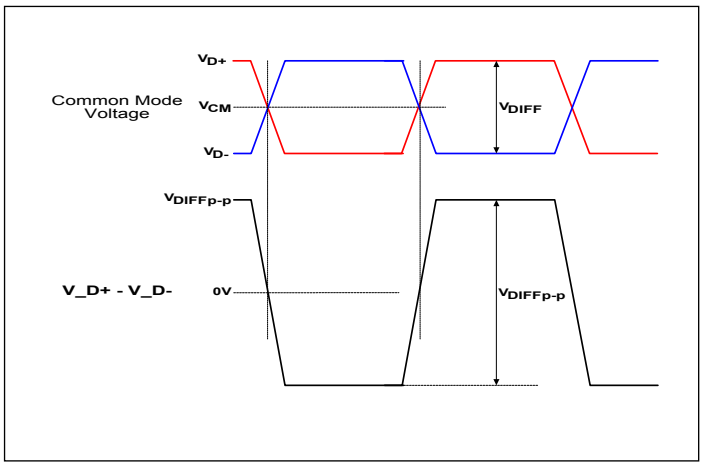
AC/DC Specifications

CML Receiver Input (100Ω differential)						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ.**	**Max**	**Units**
C_{RX}	RX AC coupling capacitance		2		12	nF
Z_{RX-DC}	DC single ended input impedance			50		Ω
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance			100		Ω
S_{dd11}_RX	L				-10	dB
	N				-7.9	dB
	H				0	dB
	S				13.3	dB/decade
	f_{min}				100	MHz
	f_{max}				6.0	GHz
S_{cc11}_RX	L				-6.0	dB
	N				-5.0	dB
	H				0	dB
	S				13.3	dB/decade
	f_{min}				100	MHz
	f_{max}				6.0	GHz
$V_{RX-DIFF-PP}$	Differential Input Peak-to-peak Voltage	Operational			1.2	Vppd

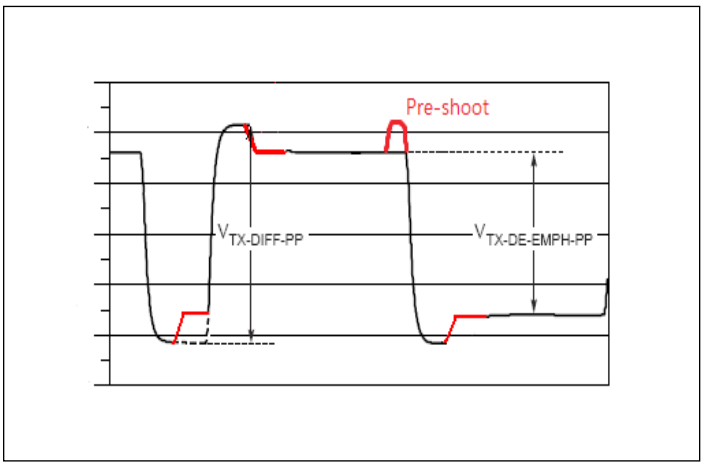
T_{RX-EYE}	Receiver eye time opening		0.4			UI
$T_{RX-Min-Pulse}$	Min width pulse at Rx		0.6			UI
CML Transmitter Output (100Ω differential)						
$V_{TX-DIFF-PP}$	Output Voltage Swing 2*|VTX-D+ - VTX-D-|	Normal Power mode Programmable 2 bits	800		1300	mVppd
$V_{TX-DE-Ratio}$	TX de-emphasis Level		0		9.5	dB
$V_{TX-Pre-Ratio}$	TX pre-shoot Level		0		6	dB
T_{tx_eye}	TX eye include all jitter sources		0.75			UI
$T_{TX-Rise-Fall}$	Transition Time 20-80%		20.8			ps
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance			100		Ω
I_{short}	The short circuit current limit			26		mA
$V_{TX-DC-CM}$	Common-Mode Voltage	| VTX-D+ + VTX-D- | /2	0		3.6	V
C_{TX}	TX AC coupling capacitance		2		12	nF
OOB Parameter						
FOOB	OOB burst data rate			1.5		Gbps
Ton	OOB On Time			4		ns
Toff	OOB Off Time			4		ns
Signal Detector						
Vth+	The assert threshold of signal detector	Signal swing @6GHz	130		210	mVppd
Vth-	The de-assert threshold of signal detector	Signal swing @100MHz	30		110	mVppd
Latency						
t_{pd}	Latency	From input to output		0.3		ns



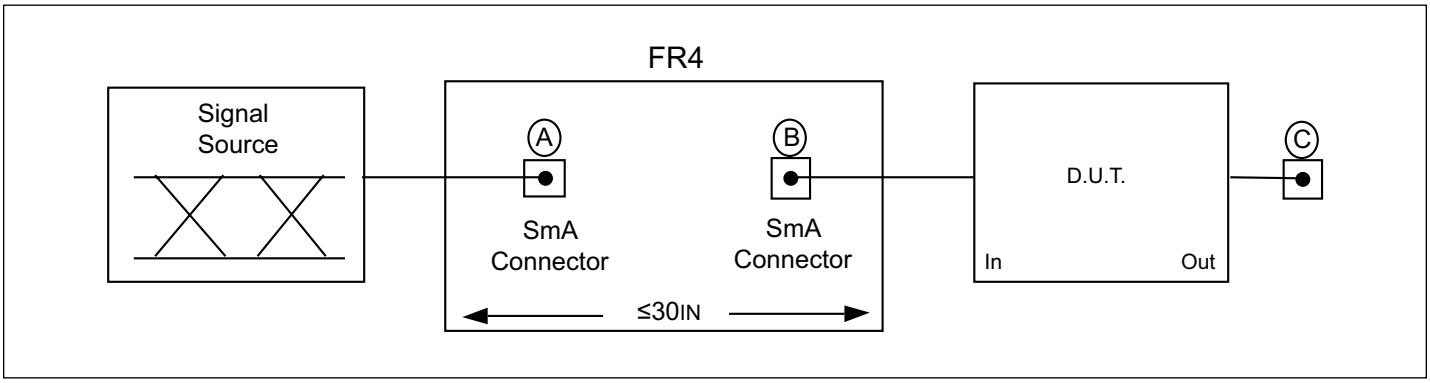
I²C Timing



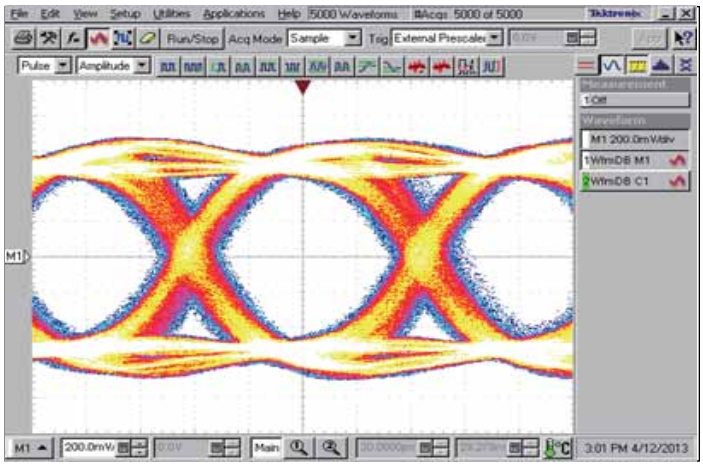
Definition of Differential Voltage and Differential Voltage Peak-to-Peak



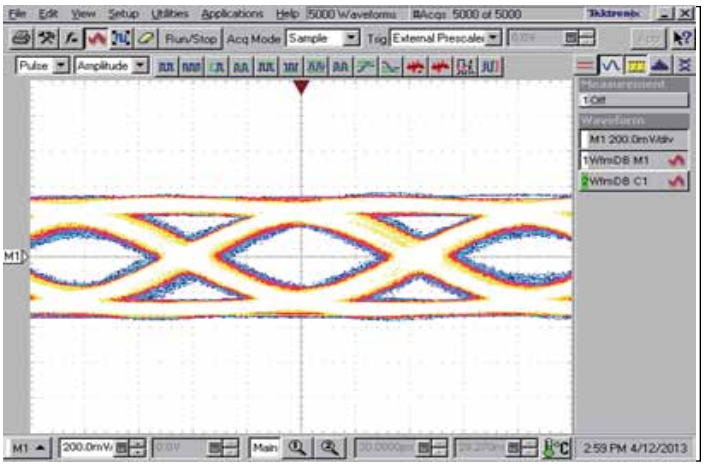
Definition of Pre-shoot and De-emphasis



AC Test Circuit Referenced in the Electrical Characteristic Table

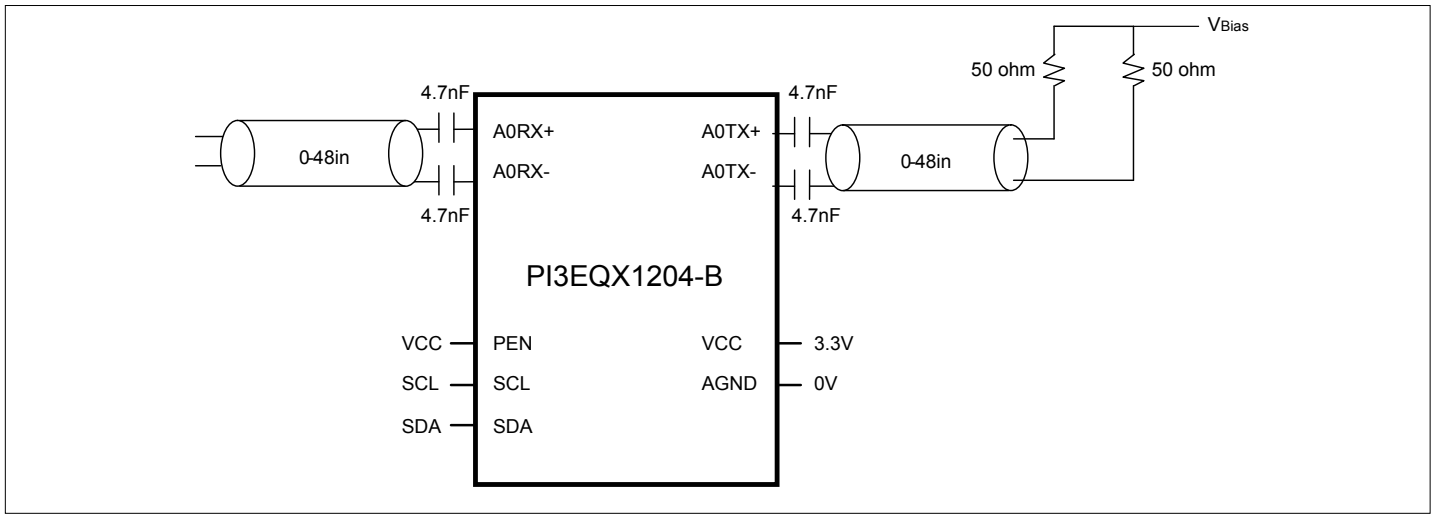


Eye Diagram at the output of PI3EQX1204-B @ 12Gb/s, PRBS 2^{15} Pattern – 36" input FR4 trace, VOD=1.15V, EQ=14dB, De-emphasis=min

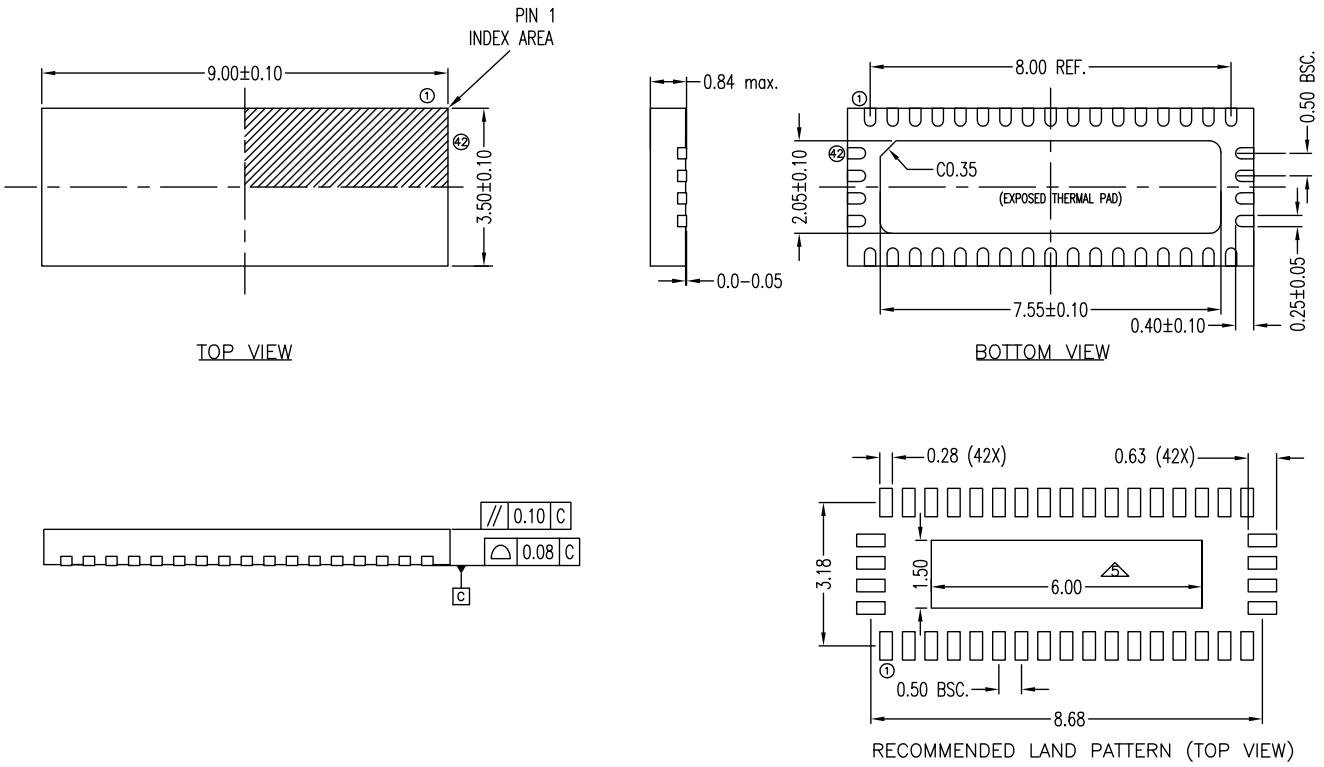


Eye Diagram at the end of output trace after PI3EQX1204-B @12Gb/s, PRBS 2^{15} Pattern – 36" input FR4 trace and 12" output trace, VOD=1.15V, EQ=16dB, De-emphasis=3.5dB

Application Diagram



Package Mechanical: 42-Contact TQFN (ZH)



Notes:
1. All dimensions are in millimeters. Angles in degrees.
2. Coplanarity applies to the exposed pad as well as the terminals.
3. Refer JEDEC MO-220.
4. Recommended land pattern is for reference only.
5. Thermal pad soldering area

PERICOM Enabling Serial Connectivity	DATE: 11/14/12
DESCRIPTION: 42-contact Thin Fine Pitch Quad Flat No-Lead (TQFN)	
PACKAGE CODE: ZH42	
DOCUMENT CONTROL #: PD-2035	REVISION:D

12-0529

Note: For latest package info, please check: http://www.pericom.com/support/packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Number	Package Code	Package Description
PI3EQX1204-BZHE	ZH	42-Contact, Thin Fine Pitch Quad Flat No-Lead (TQFN)

Notes:

- **Thermal characteristics can be found on the company web site at www.pericom.com/packaging/**
- **E = Pb-free and Green**
- **X suffix = Tape/Reel**