DIODES INCORPORATED

Pb Lead-free Green

A product Line of
Diodes Incorporated | **PERICOM**®

PI3EQX7502AI

5.0Gbps, 1-port, USB3.0 ReDriver™

Features

→ USB 3.0 compatible
→ Full Compliancy to USB3.0 Super Speed Standard
→ Two 5.0Gbps differential signal pairs
→ Adjustable Receiver Equalization
→ 100Ω Differential CML I/O's
→ Pin Configured Output Emphasis Control
→ Input signal level detect and squelch for each channel
→ Automatic Receiver Detect with digital enable/disable
→ Low Power : ~330mW
→ Auto "Slumber" mode for adaptive power management
→ Stand-by Mode – Power Down State
→ Industrial Temp Support (-40°C to 85°C)
→ Single Supply Voltage: 3.3V
→ Packaging: 24-Pin TQFN (4x4mm) (ZD)

Description

The PI3EQX7502AI is a low power, high performance 5.0 Gbps signal ReDriver™ designed specifically for the USB 3.0 protocol. The device provides programmable equalization, De-Emphasis, and input threshold controls to optimize performance over a variety of physical mediums by reducing Inter-Symbol Interference. PI3EQX7502AI supports two 100Ω Differential CML data I/O's between the Protocol ASIC to a switch fabric, over cable, or to extend the signals across other distant data pathways on the user's platform. The integrated equalization circuitry provides flexibility with signal integrity of the signal before the ReDriver. A low-level input signal detection and output squelch function is provided for each channel. Each channel operates fully independently. When the channels are enabled EN_x# = 0 and operating, that channels' input signal level (on xI+/-) determines whether the output is active. If the input signal level of the channel falls below the active threshold level (Vth-) then the outputs are driven to the common mode voltage. In addition to signal conditioning, when EN_x# = 1, the device enters a low power standby mode. The PI3EQX7502AI also includes a fully programmable receiver detect function. When the RXD-EN pin is pulled high, automatic receiver detection will be active. The receiver detection loop will be active again if the corresponding channel's signal detector is idle for longer than 7.3mS. The channel will then move to Unplug Mode if load not detected, or it will return to Low Power Mode (Slumber Mode) due to inactivity.

Figure1
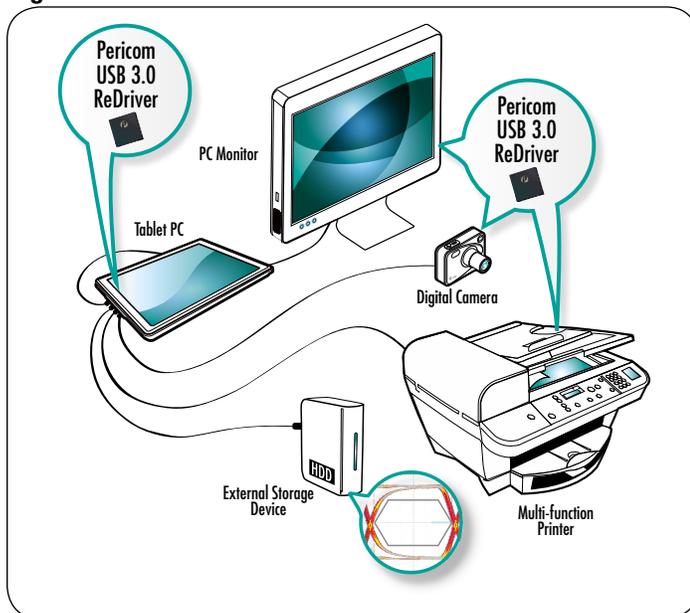
Block Diagram
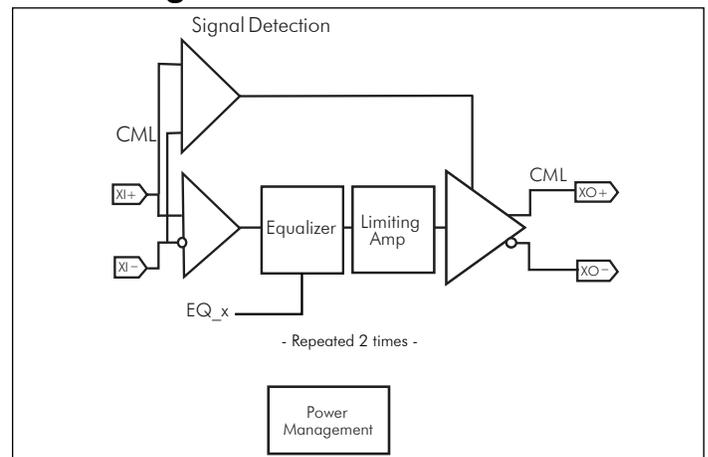
Signal Detection

CML

XI+

XI−

Equalizer | Limiting Amp

CML

XO+

XO−

EQ_x

- Repeated 2 times -

Power Management

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Diagram (Top Side View)
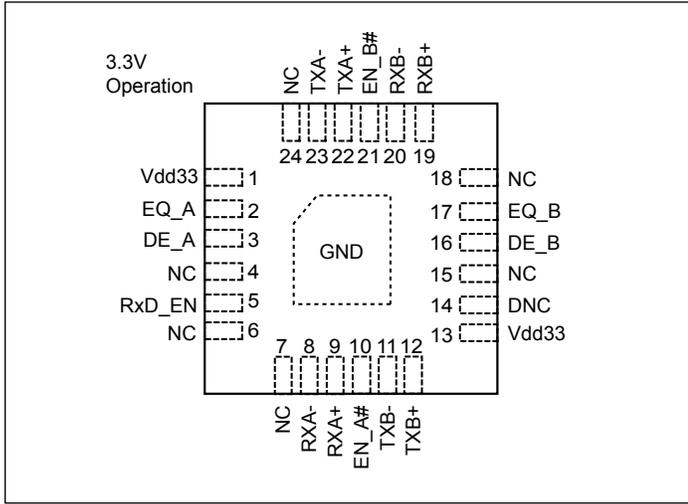
Pin Description

Pin #	Pin Name	Type	Description
2 17	EQ_A EQ_B	Input	Set the equalization of two channels. These are Tri-level input pins. When set to "HIGH" the pin becomes Logic "1"; when set to "open", the pin becomes "open", when set to "low", the pin becomes logic "0". Please refer to Mode Adjustment on page 3.
10	EN_A#	Input	Channel A Enable. When the pin is driven "Low" Channel A is in normal operation. When the pin is driven "High", Channel A is in power down mode. With internal 200kΩ pull-down resistor.
21	EN_B#	Input	Channel B Enable. When the pin is driven "Low" Channel B is in normal operation. When the pin is driven "High", Channel B is in power down mode. With internal 200kΩ pull-down resistor.
9 8 19 20	RXA+ RXA- RXB+ RXB-	Input	CML input channels. With Selectable input termination between 50Ω to internal V_{bias} and 60KΩ to GND. The input pins are pin polarity reversible.
22 23 12 11	TXA+ TXA- TXB+ TXB-	Output	Selectable output termination between 50Ω to internal V_{bias} and 2kΩ to internal V_{bias}. The output pins are pin polarity reversible.
4, 6,7, 14, 15, 18, 24	DNC	DNC	Do Not Connect
1 13	VDD33	Power	3.3V Voltage Supply
Center Pad	GND	GND	Supply Ground.
3 16	DE_A, DE_B	Input	Set the de-emphasis of the output CML buffer. These are Tri-level input pins. When set to "high", the pin becomes logic "1"; when set to "open", the pin becomes "open"; when set to "low", the pin becomes logic "0". Please refer to Mode Adjustment on page 3.
5	RxD_EN	Input	Set the state of receiver detection of two channels. "Low" means no receiver detection and "high" means the receiver detection is active. With internal 200kΩ pull-up resistor.

Power Management

Notebooks, netbooks, and other power sensitive consumer devices require judicious use of power in order to maximize battery life. In order to minimize the power consumption of our devices, Diodes has added an additional adaptive power management feature. When a signal detector is idle for longer than 1.3ms, the corresponding channel will move to low power mode ONLY. (It means both channels will move to low power mode individually).

In the slumber mode, the signal detector will still be monitoring the input channel. If a channel is in slumber mode and the input signal is detected, the corresponding channel will wake-up immediately. If a channel is in slumber mode and the signal detector is idle longer than 6ms, the receiver detection loop will be active again. If load is not detected, then the Channel will move to Device Unplug Mode and monitor the load continuously. If load is detected, it will return to Slumber Mode and receiver detection will be active again per 6ms.

The device can also be forced into low power standby mode through the use of the EN_x# pins however this would require the use of GPIO pins to control.

Configuration Table

EN_x#	R_XD_EN	Function	Input R	Output R
1	X	Channel disable if both EN_A#, EN_B# are high, chip is Powered Down	60kΩ to GND	Hi-Z
0	1	Chip and channel enabled, receiver detect is active	50Ω/60kΩ to GND	50Ω / 2kΩ
0	0	Chip and channel enabled, receiver detect is not active	50Ω	50Ω

* Refer to pin 19 description

Mode Adjustment

Equalization Setting:

EQ_A/B are the selection pins for the equalization selection for each direction.

Equalizer setting	
EQ_A/B	@ 2.5GHz
0	3 dB
open	6dB (Default)
1	9dB

De-emphasis Setting:

DE_A/B are the selection pins for the de-emphasis selection for each direction.

Output de-emphasis setting	
DE_A/B	De-emphasis
0	0 dB
open	-3.5 dB (default)
1	-6 dB

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature..−65°C to +150°C
Supply Voltage to Ground Potential ....−0.5V to +4.6V
DC SIG Voltage ....−0.5V to V_{DD} +0.5V
Output Current ....−25mA to +25mA
Power Dissipation Continuous 1.0W
Operating Temperature ....-40°C to +85°C
ESD, Human Body Model.....................................−7kv to +7kV
ESD, Machine Model.......................................−200V to +200V

Note:

Stresses greater than those listed under MAXI-MUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
DEVICE PARAMETERS						
maximum date rate					5	Gbps
t_{ENB}	Device enable time	ENA/B# H->L with Rx termination present		10	50	ms
t_{DIS}	Device disable time	ENA/B# L->H		7		ns
CONTROL LOGIC						
I_{IH}	Input High Current				50	uA
I_{IL}	Input LOW Current		-50			
Bi-level Cotrol Pins (Pin 5, 10, 21)						
V_{IH}	Input High Voltage		0.65Vdd			V
V_{IL}	Input Low Voltage				0.35Vdd	
Tri-level Control Pins (Pins: 2,3,16,17)						
V_{IH}	Input High Voltage		0.8Vdd33			V
V_{IL}	Input Low Voltage				0.2Vdd33	
$V_{I\,mid}$	Input Mid Level		0.4Vdd33	0.5Vdd33	0.6Vdd33	

AC/DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
3.3V Power Supply Characteristics						
V_{DD33}	Power Supply Voltage		3.0		3.6	V
$P_{STANDBY33}$	Supply Power Standby	EN_ [A:B]# = 1		0.15	1.8	mW
$P_{SLUMBER33}$	Supply Power Slumber	EN_ [A:B]# = 0, No Input Signal		58	65	
P_{DEVICE_UNPLUG}	Supply Power Device Unplug	EN_[A:B]# = 0, Output unterminated		7.3		
$P_{ACTIVE33}$	Supply Power Active	EN_[A:B]# = 0, $V_{RX-DIFF-P} \geq V_{TH-SD}$		328	450	
$I_{DD-STANDBY33}$	Supply Current Standby	EN_ [A:B]# = 1			0.5	mA
$I_{DD-SLUMBER33}$	Supply Current Slumber	EN_ [A:B]# = 0, No Input Signal			18	mA
$I_{DD-DEVICE\_UNPLUG}$	Supply Current Device Unplug	EN_[A:B]# = 0, Output unterminated		2.2		mA
$I_{DD-ACTIVE33}$	Supply Current Active	EN_x# = 0, $V_{RX-DIFFP-P} \geq V_{TH-SD}$			125	

AC/DC Electrical Characteristics Cont.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Receiver AC/DC						
$V_{RX-DIFFP-P}$	Differential Peak-to-Peak Input Voltage	AC coupled differential RX peak to peak signal	175		1200	mVppd
V_{RX-C}	Common Mode Voltage			1		V
V_{cm_ac}	RX AC Common Mode Voltage	Measured at Rx pins with termination enabled			150	mVP
Z_{DC_RX}	DC commmon mode inpedance		18		30	Ω
Z_{diff_RX}	DC differential input impendance		72	100	120	
$Z_{RX\_HIGH\_IMP+}$	DC Input high impedance	Device in unplug, standby modes RX termination not powered measured with respect to GND over 500mV max		67		kΩ
$RL_{RX-DIFF}$	Differential return loss	50 MHz-1.25GHz		23		db
		1.25 GH-2.5 GHz		13		
RL_{RX-CM}	Common mode return loss	50 MHz-2.5 GHz		8		db
TH-SD	Signal detect Threshold	EN_x# = 0	50		175	mVppd
Transmitter Output AC/DC (100Ω differential)[1]						
$V_{TX-DIFFP-P}$	Differential Peak-to-peak Output Voltage	$V_{TX-DIFFP-P} = 2 * \mid V_{TX-D+} - V_{TX-D-} \mid$	400		1200	mVppd
$V_{TX-LFPS}$	LFPS Differential Peak-to-peak Output Voltage		800			
V_{TX-C}	Common-Mode Voltage	$\mid V_{TX-D+} + V_{TX-D-} \mid /2$	0.5		1.2	V
DE		DEA/B = 0		0		dB
		DEA/B = NC	-3.0	-3.5	-4.0	
		DEA/B = 1		-6.0		
Z_{diff_TX}	DC differential impedance		72	90	120	Ω
Z_{CM_TX}	DC common mode impedance	Measured w.r.t to AC ground over 0-500mV	18	23	30	
RL_{diff_TX}	Differential return loss	f= 50MHz-1.25 GHz		12		dB
		f= 1.25 GHz-2.5 GHz		8		
RL_{CM_TX}	Common mode return loss	f= 50 MHz-2.5GHz		10		dB
I_{TX_SC}	TX short circuit current	TX± shorted to GND		26		mA
$V_{TX\_CM\_AC\_Active}$	TX AC common mode voltage active			30	100	mVpp

AC/DC Electrical Characteristics Cont.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Transmitter Output AC/DC (100Ω differential)[1]						
V_{detect}	Voltage change to allow receiver	Positive voltage to sense receiver termination			600	mV
t_R, t_F	Output rise/fall time	20%-80% of differental voltage measured 1" from the output pin		90		ps
T_{diff_LH}, T_{diff_HL}	Differential propagation delay	Propagation delay between 50% level at input and output		305	370	ps
Equalization						
T_{TX-EYE}[1][2]	Total jitter(Tj)			0.2	0.5	UI[3] p_P
DJ_{TX}[2]	Deterministic jitter(Dj)	with 36 inch of inputFR4 trace		0.1	0.3	
RJ_{TX}[2][4]	Random jitter(Rj)			0.09	0.2	

Note:

1. Includes RJ at 10^{-12} BER
2. Determininstic jitter measured with PRBS7 pattern, Random jitter measured with 1010 patter VID=1000mVpp, 5Gbps,
3. UI = 200ps
4. Rj calculated as 14.069 times the RMS random jitter for 10^{-12} BER

Eye Diagram
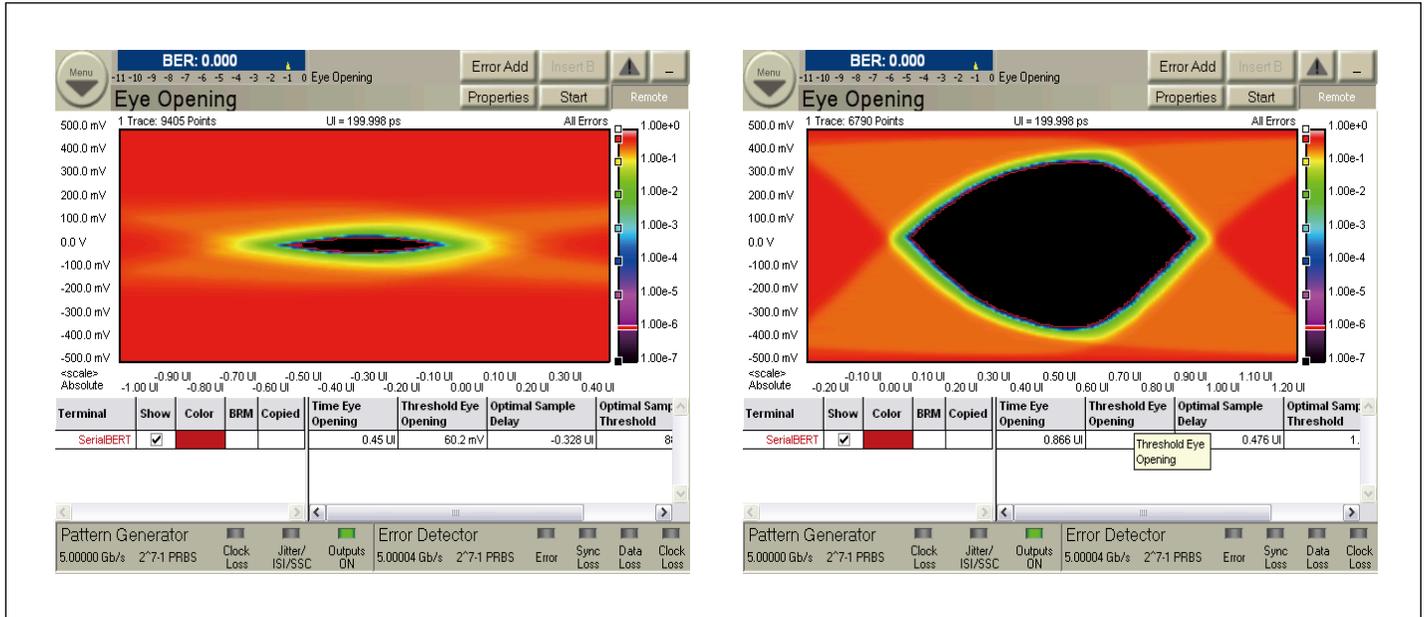
Left: Input Eye Diagram, Left: Output Eye Diagram, Trace length: 36-inch, 5.0 Gb/s

FR4

Signal
Source

Ⓐ

Ⓑ

D.U.T.

Ⓒ

SMA
Connector

SMA
Connector

In   Out

≤ 36IN
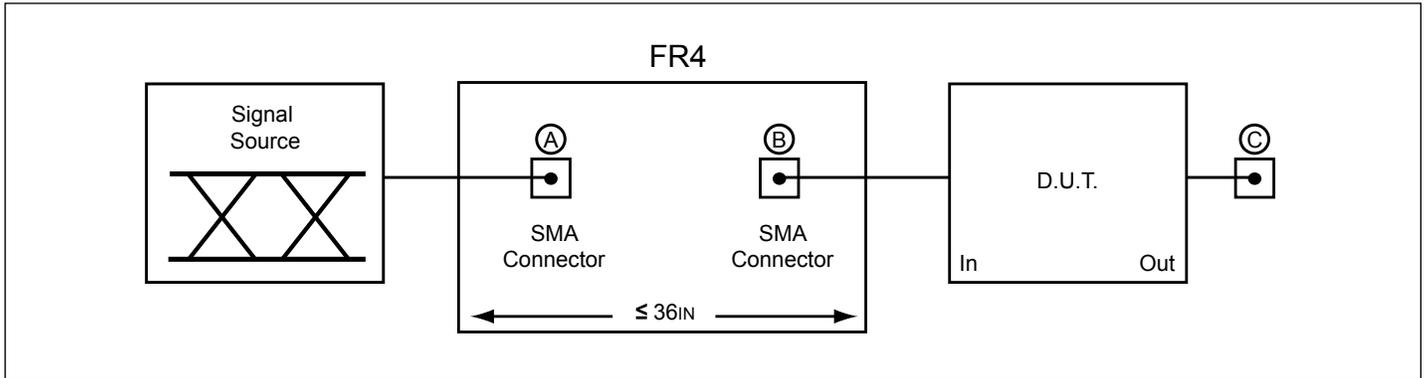
Test Condition Referenced in the Electrical Characteristic Table

Block Diagram

HOST

PI3EQX7502E
PI3EQX7502AI

DEVICE

Tx

AC coupling Caps

AC coupling Caps

Rx

Rx

AC coupling Caps

AC coupling Caps

Tx
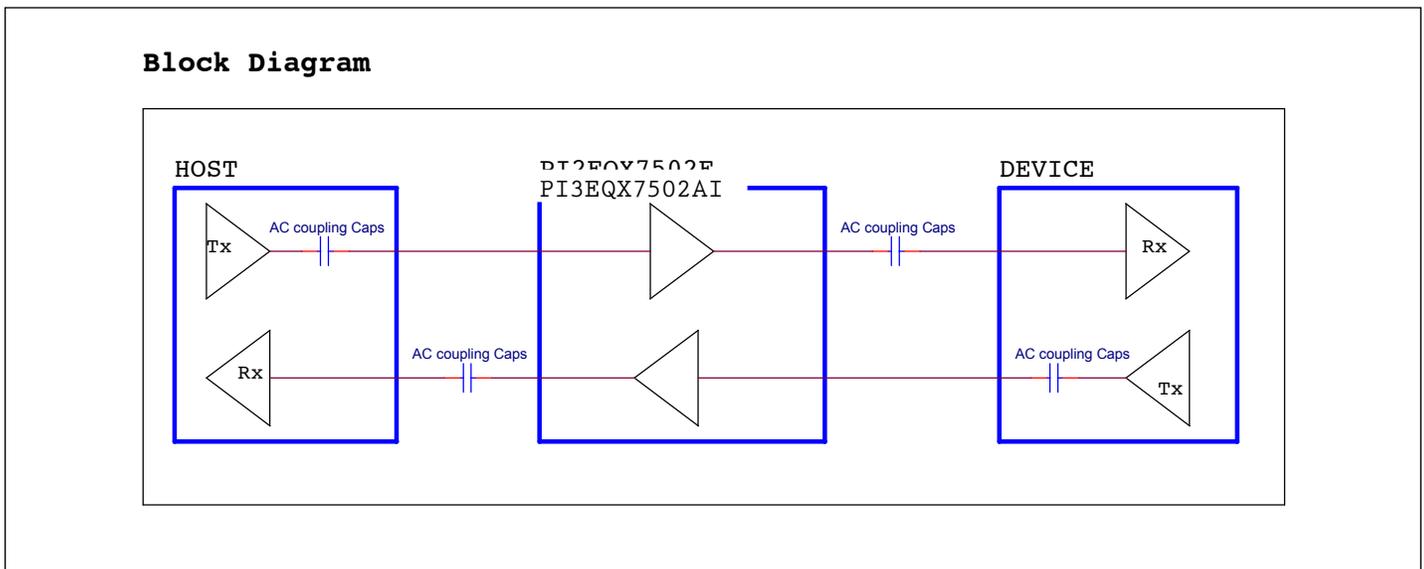
PI3EQX7502AI Application Schematics

Packaging Mechanical: 24-TQFN (ZD)

PIN1
INDEX AREA

TOP VIEW

SEATING PLANE

BOTTOM VIEW

EXPOSED THERMAL PAD

C0.35X45°

RECOMMENDED LAND PATTERN

3.86
2.30
2.30
3.86
0.70(24X)
0.28 (24X)
0.50 BSC.

SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.18	0.25	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
e		0.50 BSC	
D2	2.15	—	2.75
E2	2.15	—	2.75
L	0.35	0.40	0.45

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO−220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA
6. MAJOR EDAP D2XE2=2.25X2.25

17-0533

	DATE: 07/07/17
DIODES INCORPORATED / PERICOM — A PRODUCT LINE OF DIODES INCORPORATED — ENABLING SERIAL CONNECTIVITY	
DESCRIPTION: 24-Contact, Very Thin Quad Flat No-Lead (TQFN)	
PACKAGE CODE: ZD (ZD24)	
DOCUMENT CONTROL #: PD-2100	REVISION: C

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Number	Package Code	Package Description
PI3EQX7502AIZDEX	ZD	24-Contact, Very Thin Quad Flat No-Lead (TQFN)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
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3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

IMPORTANT NOTICE

LIFE SUPPORT