A Product Line of
Diodes Incorporated

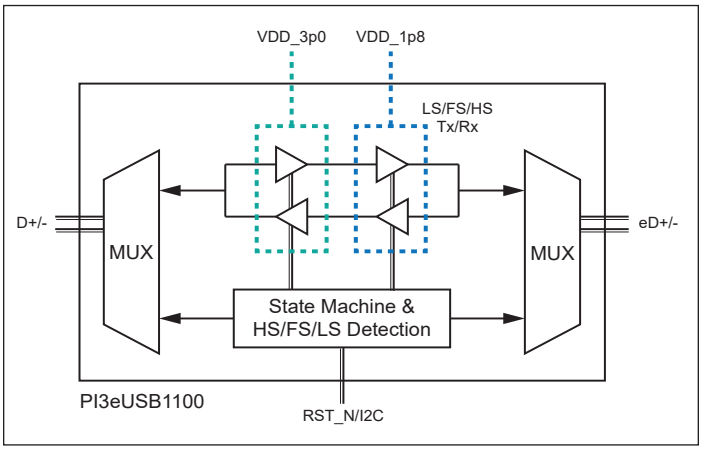
PI3EUSB1100

eUSB to USB 2.0 / USB 2.0 to eUSB 1.8V Digital I²C I/O Repeater

Description

The PI3EUSB1100 eUSB2 repeater is an interface between legacy USB 2.0 systems and lower voltage SoCs based on modern process geometries. The device is compliant with the Embedded USB 2.0 (eUSB2) Physical Layer Supplement to the USB Revision 2.0 Specification and supports eUSB2 operations and protocol.

Block Diagram



Features

- Low Skew Outputs: <80ps
- Compliant with the Latest USB 2.0 Specification
- Compliant with Embedded USB 2.0 (eUSB2) Physical Layer Specification Rev. 1.2
- Dual Role Capable
- Integrated and Configurable Pull-Down Resistors on Both eUSB2 and USB 2.0 Ends
- Integrated and Configurable Pull-Up Resistors on USB 2.0 Port
- Supports All USB 2.0 Speed Modes through Speed Detection and Negotiation
  - High Speed Operation (480Mb/s)
  - Full Speed Operation (12Mb/s)
  - Low Speed Operation (1.5Mb/s)
- Auto Resume (remote wake-up)
- Asynchronous Wake-Up
- Provides Bus-Keeper Function for Device Wake-Up at Host Mode
- Supports 1.8V I²C I/O
- Supports x4 I²C ID Address
- ESD Performance
  - HBM All Pins +/-8KV
  - CDM All Pins +/-1KV
  - Contact Discharge (IEC61000-4-2) for USB 2.0 D+/- +/-8KV
- Low Power Consumption
  - Typical = 87mW Nominal Power during HS USB 2.0/eUSB2 Communication
- Analog Trimming
  - Tx Amplitude Adjusts
  - Tx EQ Adjusts
  - Tx Drive Strength Adjusts
  - Rx Sensitivity Tuning
- Charger Compliance
  - Ability to Keep D+/D- Lines in Hi-Z for APSD
- Chirp Levels
  - Chirp J Differential Voltage (VCHIRPJ) is +700 to +1100 mV
  - Chirp K Differential Voltage (VCHIRPK) is -900 to -500 mV
- Squelch Detectors on Both eUSB2 and USB 2.0 Ports
- Configurable HS Disconnect Detector at USB 2.0 Port
- De-Glitch of ≥100ns on RST_N
- Ambient Temperature: -40°C to 85°C
- Packaging (Pb-free & Green):
  - 12-ball, WLCSP (GH) 1.65mm x 1.22mm x 0.35mm pitch
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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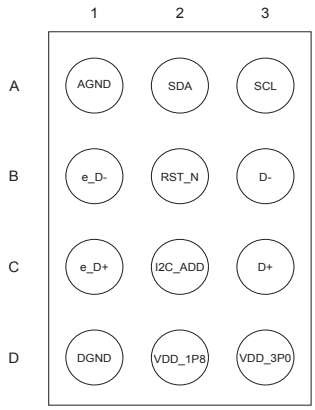
Pin Configuration



Pin Description

Pin Number	Pin Name	Signal Type	Description
D1	DGND	Ground	Digital ground
D2	VDD_1P8	Power	1.8V supply for analog circuitry
D3	VDD_3P0	Power	3.3V supply for analog circuitry
C1	e_D+	Analog	eUSB2 Positive signals
C2	I2C_ADD	Digital Input	I2C address setup. Refer to Table 2. VDD: 1.8V
C3	D+	Analog	USB 2.0 Positive signals
B1	e_D-	Analog	eUSB2 Negative signals
B2	RST_N	Digital Input	Active low reset with internal 20k pulled to 1.8V. When tied to low, disable 20k resistor
B3	D-	Analog	USB 2.0 Negative signals
A1	AGND	Ground	Analog ground
A2	SDA	Digital I/O	I2C data pin; TX/RX EQ initial setting
A3	SCL	Digital Input	I2C clock pin; TX/RX EQ initial setting

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Application Information

USB 2.0 Hi-Z During Reset

The eUSB2 repeater will often be used in a system where the USB 2.0 D+/D- lines will be connected both externally (to a device, or charger, say) and internally to another ASIC in the system. In such cases there is often a period of time where the USB 2.0 device and system ASIC will communicate to each other over the D+/D- lines. Because of this, the D+/D- lines must always be held in a high impedance (Hi-Z) state until RST_N is de-asserted, even while all supplies are actively enabled to the repeater.

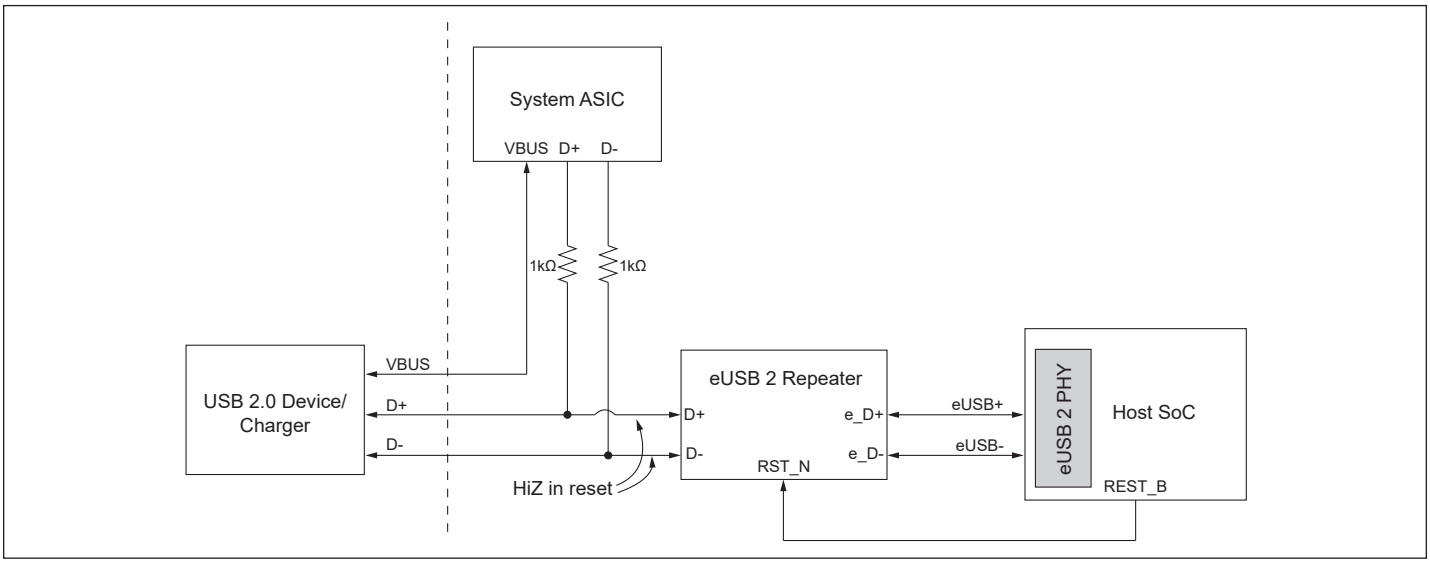

Figure 1. System Connectivity Example of eUSB2 Repeater

Auto Resume (Peripheral Initiated)

When a peripheral (such as a USB audio headset) is trying to resume active communication after the host has put the bus in suspend, it will assert a Resume K signal on the bus, which – depending on bus speed – will either be D+High and D-Low, or vice versa. However, the peripheral is only required to maintain the Resume K state for 1-15 ms, and if the device holds the state on the low end of this requirement (~1 ms), the Resume K state may not be held long enough by the peripheral for it to still be in the K state when the host responds, which may mean that the peripheral will not behave as intended once the host enters resume and it will instead go back to L2.

Therefore, bus keepers need to be employed in the repeater. These keepers will actively drive the state of the D+/D- lines even after the peripheral has stopped driving D+/D- in the Resume K state. The repeater needs to have the keepers active until the host resumes driving the bus so that host/peripheral communication can resume. The repeater will take the D+/D- lines out of Hi-Z when a control bit has been set via a PBUS register write. (Likewise, clearing this bit will force the D+/D- lines back to Hi-Z.)

This is depicted in Figure 2. The sequence of events is as follows (numbers correspond to arrows in Figure 2):

1. While in L2, the device wants to wake up the host, so it asserts the K state using D+/D-.
2. When the eUSB2 repeater sees the K state, it drives eD-High (bold line depicts eUSB2 repeater driving line state).
3. When the host sees eD-go high, it changes to K state and begins Wake.
4. When the host leaves the Wake state, it drives eD+High for the start of resume pulse (3a), at which time the eUSB2 repeater will release control of eD- (3b).
5. When the host TxData has changed and is valid in the SE0 state, it drives eD-/eD+ appropriately, which causes the eUSB2 repeater to drive a SE0 on the D+/D- lines and put the USB device back into L0.

NOTE:

Unless the USB 2.0 device still sees the K state when the SE0 is driven from the repeater, it will not necessarily understand that a wake-up has occurred and can remain in suspend. Therefore, the eUSB2 repeater needs to implement bus keepers to keep the D+/D- lines driven in the K state until the host drives eD+High (happens after TxValid goes back Low at the End of Resume (EOR)).

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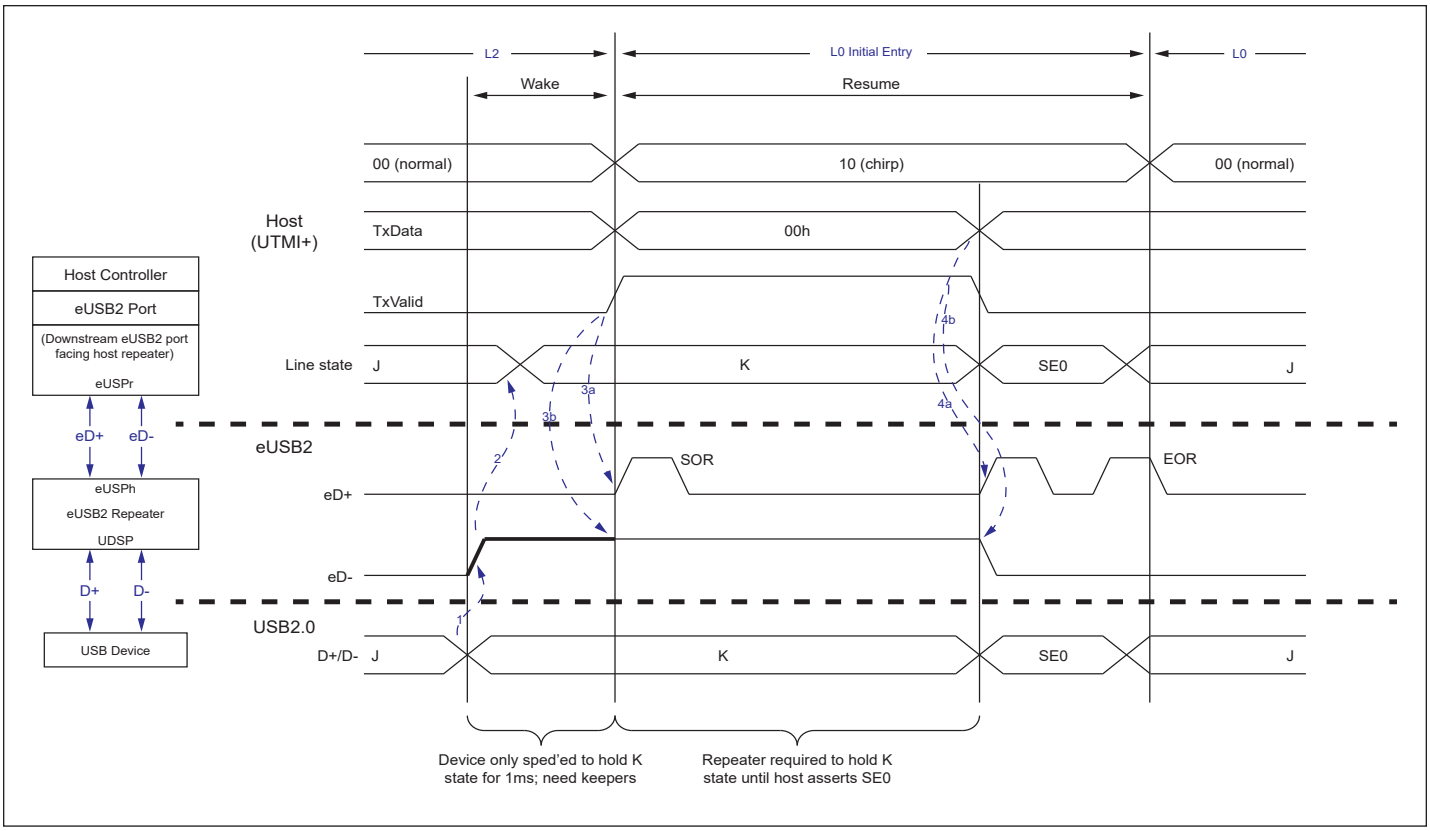

Figure 2. Auto Resume Signaling (Peripheral Initiated) in Host Repeater Mode

Auto Resume (Host Initiated)

Another auto resume case is where the SoC is the peripheral and has the eUSB2 repeater attached, and the host initiates the resume. This is depicted in below in Figure 3.

In this case, the host internal line state will transition from J to K and the host will drive D+/D- to the K state (arrow 1 in Figure 3). When it sees the K state on D+/D-, the eUSB2 repeater will drive the K state on eD+/eD- by driving eD-HIGH. After a short time, the host will drive a SE0 on D+/D- (arrow 3) and the repeater will drive eD+HIGH, eD-LOW, then eD- back low to the SE0 state at the EOR (arrow 4).

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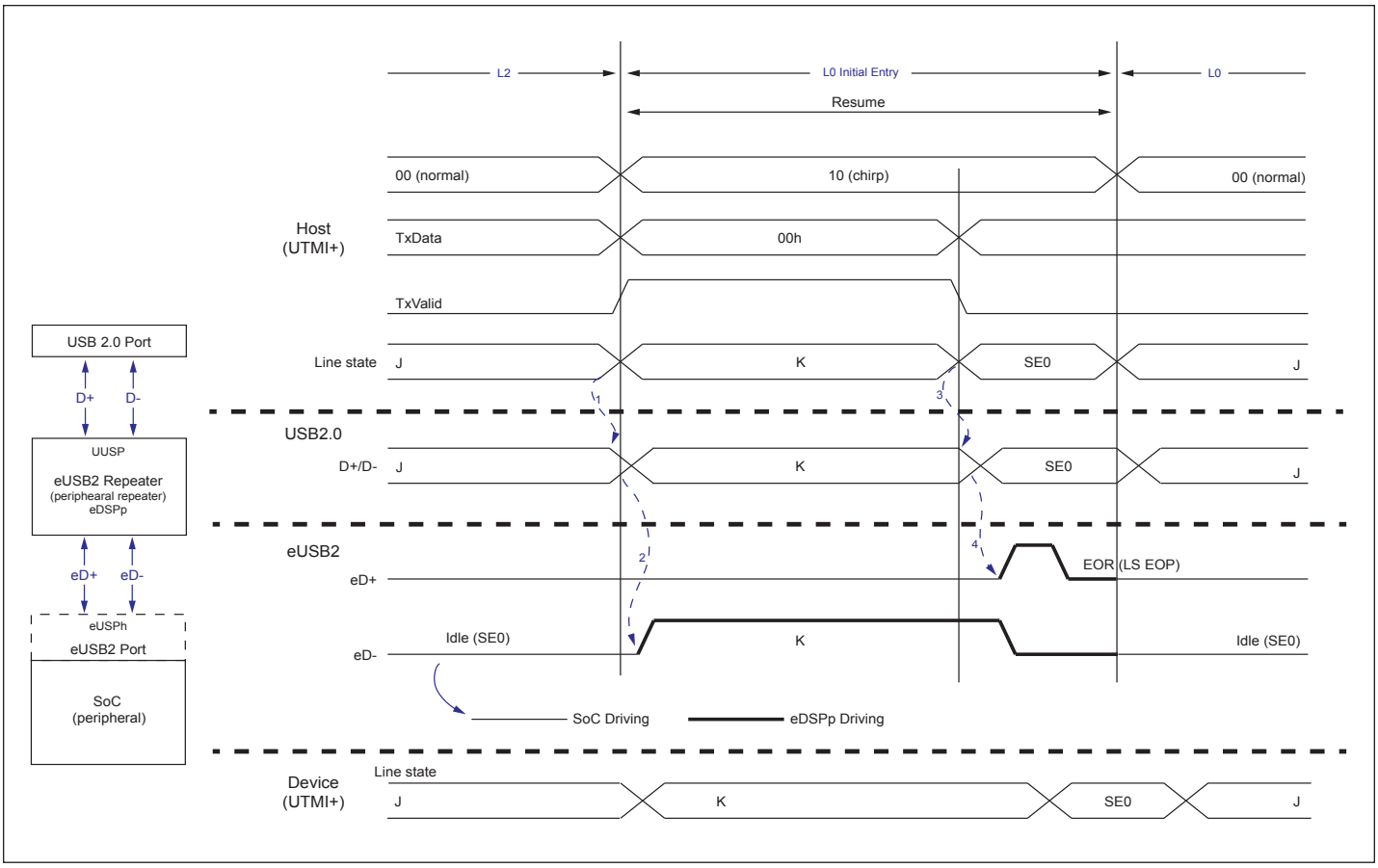

Figure 3. Auto Resume Signaling (Host Initiated) in Peripheral Repeater Mode

Asynchronous Wake-Up

During L2 suspend the system clock will be turned off for optimum power savings. However, the eUSB2 repeater must be able to propagate the Resume K signaling from the peripheral to the SoC's eUSB2 PHY during L2 suspend. Therefore, the eUSB2 repeater must have a mechanism for the repeater to respond to the Resume K signal asynchronously, or without the clock active.

This is shown in Figure 4. The USB 2.0 device will attempt to come out of L2 suspend by toggling the D+/D- lines from 'J' to 'K' state. Even with the clock off, the eUSB2 repeater needs to recognize this change of line state, turn on the system clock, and follow the normal resume protocol (as described in more detail above) by driving eD-High so that the eUSB2 PHY in the SoC can respond.

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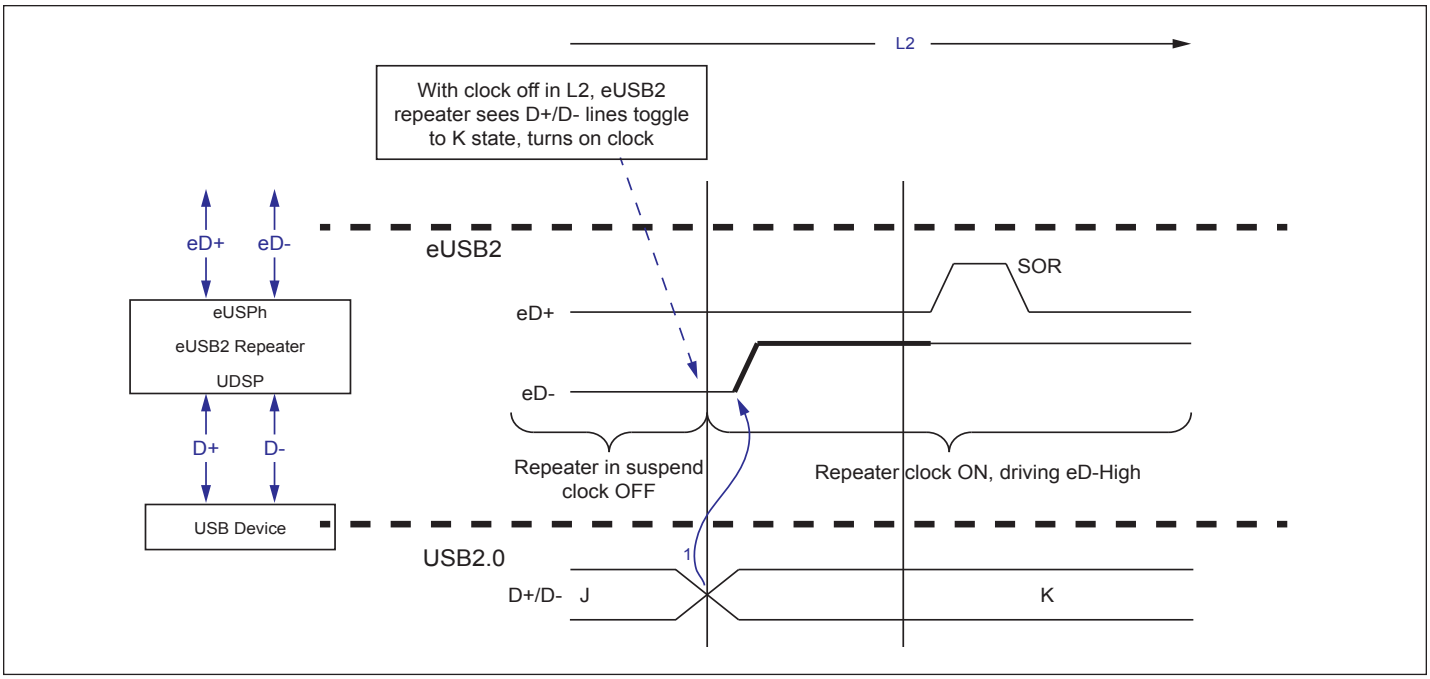

Figure 4. Asynchronous Wake-up Waveforms

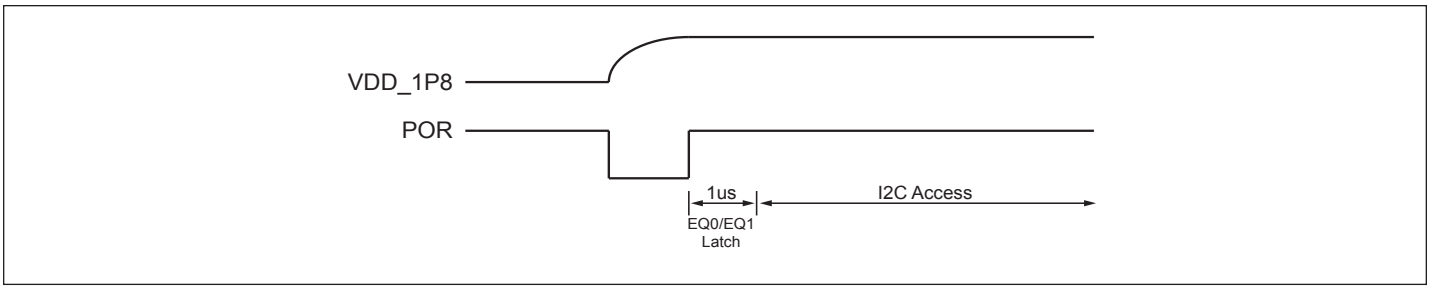

Figure 5. EQ0 and EQ1 Strapping Pin Latch Up Waveform

Device Function Modes

Repeater Mode

Table 1. Number of Hubs Supported with Host and/or Peripheral Repeater

Number of eUSB2 Repeaters	Number of Hubs Operating at HS	Number of Hubs Operating at FS	
1	4	2	Number of hubs operating at FS is reduced due to $T_{e\_to\_U\_DJ1}$ and T_{RJR1}.
2	3	1	
0	5	5	non-eUSB2 system for reference

Deep standby mode, RST_N could be used as a power down pin when asserted low, that will put device in lowest power mode.

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Register Map

The eUSB2 repeater shall have I2C-accessable 8-bit registers for setting analog tuning bits, mode setting, as well as for setting various test modes. The precise detail for each of these register settings will be provided in future releases of this document.

I2C_ADD pin is for I2C ID address setting, please direct connect to VDD (1.8V) or GND.

Table 2. I2C Address Selection Table

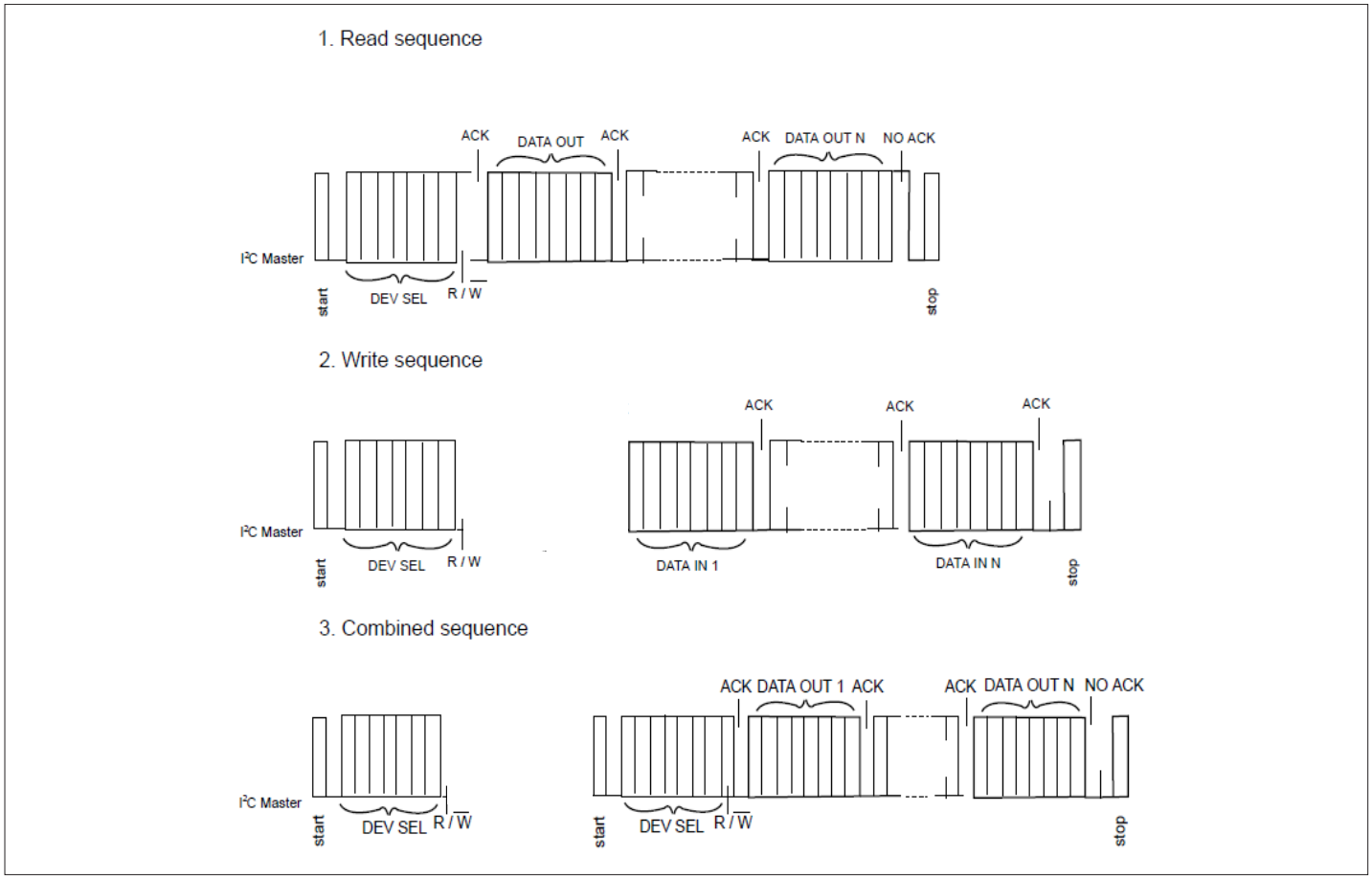
I2C ID Address			
GND	**VDD**	**200K Pull-up**	**56K Pull-up**
8'hDE	8'hDA	8'hD6	8'hDC

Table 3. TX/RX EQ Initial Setting

TX/RX EQ Initial Setting				
SCL	1	0	1	0
SDA	1	1	0	0
Default RX EQ of eUSB/USB	0dB/0dB	0dB/2dB	1dB/2dB	2dB/1dB
Default TX EQ of eUSB/USB	0dB/0dB	0dB/3dB	1dB/3dB	1.5dB/1.5dB

Note: When SCL and SDA are connected to I2C interface, please pull-up.

I2C Data Transfer



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SDA and SCL I/O for I²C-Bus

V_{CC} = 1.62 to 1.98V

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{IH}	DC input logic high		1.3	3.6	V
V_{IL}	DC input logic low		–0.3	0.6	V
V_{OL}	DC output logic low	I_{OL} = 3mA		0.4	V
V_{hys}	Hysteresis of Schmitt trigger input		0.05*V_{CC}		V
t_{of}	Output fall time from V_{IHmin} to V_{ILmax} with bus cap. 10-400pF			250	ns
f_{sCLK}	SCLK clock frequency			1000	kHz

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I2C Table

Byte 0: Mode Force Control 0				
Bit	**Name**	**Type**	**Control Function**	**Default**
7	D+ line state	R	D+ line indicate 3V CMOS level 0b: normal operation 1b: pull high >3V. Real time during LS/FS toggling	0
6	RESET	RW	0b: normal operation 1b: same behavior as RST_N pin	0
5	D+ bit 1.5K enable	RW	0b: D+ 1.5k disable 1b: D+ 1.5k pull high	0
4	Force D+ 1.5K engage	RW	0b: normal operation 1b: determines bit5 D+ bit 1.5k engage	0
3	SLEEP_FUN_BIT	RW	0b: normal operation 1b: lowest power possible and cannot be waked by USB2/ eUSB2 ports	0
2	USB_HI_Z	RW	0b: normal operation 1b: D+/D- HIZ	0
1	Reserved	RW	For internal usage	0
0	I2C_DISC_DET	RW	0b: normal operation 1b: enable TX EQ after 30 HS bit of uSOF's EOP	0

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Byte 1: USB2 TX EQ Control 1				
Bit	**Name**	**Type**	**Control Function**	**Default**
7 6	USB2_bias [1:0]	RW	Inside current bias for RX/TX-prebuffer LSFS buffer and HS detect buffer 00b: 50uA 01b: 45uA 10b: 55uA 11b: 60uA	00b
5	Reserved	RW	For internal usage	0
4	Reserved	RW	For internal usage	0
3	Reserved	RW	For internal usage	0
2 1 0	USB2_TX_EQ [2:0]	RW	D+/D- TX HS EQ 000b: 0.0dB (no EQ) 001b: 0.5dB 010b: 1.0dB 011b: 1.5dB 100b: 2.0dB 101b: 3.0dB 110b: 4.5dB 111b: 6.0dB The settings of USB2_TX_EQ [2:0] (Byte 1), USB2_TX_SWING [7:0] (Byte 6) and USB2_discon [2:0] registers may affect each other. Please see details and follow the guidelines in the application note.	000b

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Byte 2: eUSB2 TX EQ Output Current Control 2				
Bit	**Name**	**Type**	**Control Function**	**Default**
7 6 5	eUSB2_TX_SWING [2:0]	RW	eUSB2 TX output amplitude 000b: 200mv 001b: -10mv (190mv) 010b: +10mv (210mv) 011b: +20mv (220mv) 100b: +30mv (230mv) 101b: +40mv (240mv) 110b: +60mv (260mv) 111b: +80mv (280mv)	000b
4	RST_N PULL_HIGH	RW	0b: enable 20K/2M pull up 1b: disalbe 20K/2M pull high	0
3	RST_N PULL_DOWN	RW	0b: disable 100K pull down 1b: enalbe 100K pull down	0
2	BUS_KEPPER [0]	RW	Bus keeper [0] Bus_keeper[1:0] 00b: Hold bus at both of eUSB and USB 01b: Hold bus only at eUSB 10b: No bus keeper function 11b: reserved and should not be used	0
1 0	eUSB2_TX_EQ [1:0]	RW	eD+/eD- TX HS EQ 00b: 0.0dB (no EQ) 01b: 0.5dB 10b: 1.0dB 11b: 1.5dB	00b

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Byte 3: USB2 RX EQ Control 3				
Bit	**Name**	**Type**	**Control Function**	**Default**
7 6	USB2_Rup [1:0]	RW	USB2 LS/FS output pull high resistor 00b: 0% (36Ω) 01b: -20% (29Ω) 10b: -20% (29Ω) 11b: 0% (36Ω)	00b
5	Reserved	RW	For internal usage	0
4	Reserved	RW	For internal usage	0
3 2 1 0	USB2_RX_RQ	RW	USB2 RX EQ 0x0: 0.0dB (no EQ) 0x1: 0.5dB 0x2: 1.0dB 0x4: 2.0dB 0x8: 3.0dB others: reserved and should not be used.	0x0

Byte 4: eUSB2 RX EQ + Squelch Swing Selection Control 4				
Bit	**Name**	**Type**	**Control Function**	**Default**
7 6 5	eUSB2_squelch [2:0]	RW	eUSB2 squelch detection threshold 000b: 70mv 001b: -10mv (60mv) 010b: -20mv (50mv) 011b: -30mv (40mv) 100b: +10mv (80mv) 101b: +20mv (90mv) 110b: +30mv (100mv) 111b: +30mv (100mv)	0
4	BUS_KEPPER [1]	RW	Bus keeper [1] Bus_Keeper[1:0] 00b: Hold bus at both of eUSB and USB 01b: Hold bus only at eUSB 10b: No bus keeper function 11b: reserved and should not be used	0
3 2 1 0	eUSB2_RX_EQ [3:0]	RW	eUSB2 RX EQ 0x0: 0.0dB (no EQ) 0x1: 0.5dB 0x2: 1.0dB 0x4: 2.0dB 0x8: 3.0dB others: reserved and should not be used.	0x0

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Byte 5: USB2 Squelch Detection Offset Control 5				
Bit	**Name**	**Type**	**Control Function**	**Default**
7	REPEATER_REG [16]	RW	For digital EOP filter control 0b: disable filter 1b: enable filter	1
6	CHIRP_KJ_TEST	RW	1b: force into CHIRP test for High speed	0
5	USB2_squelch [5:0]	RW	USB2 RX squelch detection threshold 0x00: 110mv 0x01: -50mv (60mv) 0x02: -40mv (70mv) 0x04: -30mv (80mv) 0x08: -20mv (90mv) 0x10: -10mv (100mv) 0x20: +10mv (120mv) others: reserved and should not be used.	0x00
4				
3				
2				
1				
0				

Byte 6: USB2 TX Output Swing Control 6				
Bit	**Name**	**Type**	**Control Function**	**Default**
7	USB2_TX_SWING [7:0]	RW	USB2 TX output swing 0x00: 400mv 0x01: -50mv (350mv) 0x02: -25mv (375mv) 0x04: +25mv (425mv) 0x08: +50mv (450mv) 0x10: +75mv (475mv) 0x20: +100mv (500mv) 0x40: +125mv (525mv) 0x80: +175mv (575mv) others: reserved and should not be used. The settings of USB2_TX_EQ [2:0] (Byte 1), USB2_TX_SWING [7:0] (Byte 6) and USB2_discon [2:0] registers may affect each other. Please see details and follow the guidelines in the application note.	0x00
6				
5				
4				
3				
2				
1				
0				

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Byte 7: USB2 FS Output Res + Disconnection Detection Swing Setting Control 7				
Bit	**Name**	**Type**	**Control Function**	**Default**
7	Reserved	RW	For internal usage	0
6 5 4	USB2_discon [2:0]	RW	USB2 disconnect threshold voltage 000b: 575mv 001b: -50mv (525mv) 010b: -25mv (550mv) 011b: +25mv (600mv) 100b: +50mv (625mv) 101b: +100mv (675mv) 110b: +175mv (750mv) 111b: +250mv (825mv) The settings of USB2_TX_EQ [2:0] (Byte 1), USB2_TX_SWING [7:0] (Byte 6) and USB2_discon [2:0] registers may affect each other. Please see details and follow the guidelines in the application note.	000b
3 2 1 0	USB2_Rdn [3:0]	RW	USB2 LS/FS/HS output pull low resistor 0x0: 45Ω 0x1: -10% 0x2: -5% 0x4: +5% 0x8: +10% others: reserved and should not be used.	0x0

Byte 8 – Byte 19: Reserved for Factory Control

Byte 20: Revision ID, RO Bits				
Bit	**Name**	**Type**	**Control Function**	**Default**
7:0	Revision ID	RO	revision id	0x03

Byte 21: Device ID, Low Byte, RO Bits				
Bit	**Name**	**Type**	**Control Function**	**Default**
7:0	Device ID [7:0]	RO	device id low word	0x00

Byte 22: Device ID, High Byte, RO Bits				
Bit	**Name**	**Type**	**Control Function**	**Default**
7:0	Device ID [15:8]	RO	device id high word	0x11

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Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–55°C to +150°C
Junction Temperature	–40°C to +125°C
Ambient Temperature	–40°C to +85°C
Analog I/O (D+/-)	–0.5V to 5.5V
Analog I/O (eD+/-)	–0.5V to 2.2V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{DD_3P0}	USB 2.0 analog voltage		3.0	3.3	3.6	V
V_{DD_1P8}	Analog supply voltage		1.71	1.8	1.89	V
V_{IL}	Input voltage Low	VDD18 = 1.8V, RST_N			0.54	V
V_{IH}	Input voltage High	VDD18 = 1.8V, RST_N	1.26			V
I_{IL}	Low level input current	VDD33 = 3.3V or 0V, VDD18 = 1.8V or 0V, V_{IL} = 0V for SDA/SCL			2	uA
I_{IH}	High level input current	VDD33 = 3.3V or 0V, VDD18 = 1.8V or 0V, V_{IH} = 3.3V for SDA/SCL			2	uA
I_{IL}	Low level input current	VDD33 = 3.3V, VDD18 = 1.8V, V_{IL} = 0V for RST_N			2	uA
I_{IH}	High level input current	VDD33 = 3.3V, VDD18 = 1.8V, V_{IH} = 1.8V for RST_N			2	uA
Pstby	Deep standby mode	Repeater powered, in reset. I2C_ADD = GND or 1.8V		80		uW
PDET	Detach power	Repeater powered, connected to eUSB PHY and waiting to attach		131		uW
PL2S	L2 sleep power	Link in L2, waiting for wake event		131		uW
PL1S	L1 sleep power	USB link in L1, waiting for L1 exit event		131		uW
PLSA	LS active power	Repeater in LS mode		6.6		mW
PFSA	FS active power	Repeater in FS mode		13.2		mW
PHSA	HS active power	Repeater in HS mode, maximum data rate, EQ 0dB, 450mV swing		87		mW

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Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
USB 2.0 (D+/D-)						
Input Levels for LS/FS						
V_{IH}	Input High voltage (driven)		2.0			V
V_{IHZ}	Input High voltage (floating)		2.7		3.6	V
V_{IL}	Input Low voltage (driven)				0.8	V
V_{DI}	Differential input sensitivity	|(D+)-(D-)|	0.2			V
V_{CM}	Differential common mode range	Includes VDI range	0.8		2.5	V
Input Levels for HS						
V_{HSSQ}	HS squelch detection threshold (differential signal amplitude)		100		150	mV
V_{HSDSC}	HS disconnect detection threshold (differential signal amplitude)			575		mV
V_{HSDIFF}	HS differential input signal levels		Specified by eye pattern templates			
V_{HSCM}	HS data signaling common mode voltage range (guideline for receiver)		–50		500	mV
T_{j_add}	Differential additive jitter	Signal generator source			50	ps
Output Levels for LS/FS						
V_{OL}	Output low voltage		0		0.3	V
V_{OH}	Output high voltage (driven)		2.8		3.6	V
V_{OSE1}	SE1 voltage		0.8			V
V_{CRS}	Output signal crossover voltage		1.3		2.0	V
Output Levels for HS						
V_{HSOI}	HS idle level		–10		10	mV
V_{HSOH}	HS data signal high		360	400	440	mV
V_{HSOL}	HS data signal low		–10		10	mV
V_{CHIRPJ}	Chirp J level (differential)		700		1100	mV
V_{CHIRPK}	Chirp K level (differential)		–900		–500	mV
LS/FS Parameters						
R_{PU}	Bus pull-up resistor on up-stream facing port		1.425	1.5	1.575	kΩ
R_{PD}	Bus pull-down resistor on downstream facing port		14.25	15	15.75	kΩ
Z_{INP}	Input impedance exclusive of pull-up/pull-down		300			kΩ

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Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{TERM}	Termination voltage for up-stream facing port R_{PU}		3.0		3.6	V
HS Parameters						
V_{HSTERM}	Termination voltage in HS		–10		10	mV
T_{HSR}	Rise time for HS (10%-90%)		100			ps
T_{HSF}	Fall time for HS (10%-90%)		100			ps
Z_{HSDRV}	Driver output resistance (also serves as FS termination which with HS capable)		40.5	45	49.5	Ω
eUSB2 (eD+/eD-)						
LS/FS Parameters (VCC = 1.1-1.2V)						
V_{IL}	Input low voltage		–0.1		0.35*VCC	V
V_{IH}	Input high voltage		0.65*VCC		1.05*VCC	V
V_{HYS}	Receive single-end hysteresis voltage		0.04*VCC			V
V_{OL}	Output low voltage				0.15*VCC	V
V_{OH}	Output high voltage		0.85*VCC		VCC	V
R_{SRC_LSFS}	Transmit output impedance		28		60	Ω
HS Parameters						
$V_{TX\_DIF\_TERM}$	Transmit differential voltage (terminated)		165	200	245	mV
V_{TX_CM}	Transmit common mode		170	200	230	mV
R_{SRC_HS}	Transmit source termination impedance		32	40	48	Ω
ΔR_{SRC_HS}	Source impedance mismatch				4	Ω
$V_{TX\_CM\_AC}$	Transmit CM AC (50MHz-480MHz)				30	$+/-mV_{PK}$
$T_{RISE\_FALL\_TRM}$	Transit rise and fall time (20%-80%)		100			PS
$\Delta T_{RISE\_FALL\_TRM}$	Transit rise/fall mismatch				25	%
V_{RX_CM}	Receive common mode range		120	200	280	mV
C_{RX_CM}	Receive center-tapped capacitance		15		50	pF
$V_{RX\_DIF\_SENS}$	Receive sensitivity (peak differential)		60			+/-mV
R_{RCV_DIF}	Differential receiver termination (repeater)		72	80	88	Ω

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Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
$V_{SQUELCH\_DIF}$	Squelch detect threshold voltage (peak differential)		60		110	mV
$V_{CM\_RX\_AC}$	Receiver AC common mode (50MHz-480MHz)				60	+/-mV_{PK}
T_{j_add}	Differential additive jitter	Signal generator source			50	ps

Switching Characteristics

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
D+/D- FS Driver Switching Characteristics						
T_{FR}	Rise Time (10%-90%)	USB 2.0 specification	4		20	ns
T_{FF}	Fall Time (10%-90%)	USB 2.0 specification	4		20	ns
D+/D- LS Driver Switching Characteristics						
T_{LR}	Rise Time (10%-90%)	USB 2.0 specification	75		300	ns
T_{LF}	Fall Time (10%-90%)	USB 2.0 specification	75		300	ns
eD+/eD- LS/FS Driver Switching Characteristics						
T_{FR}/T_{FF}	Rise/Fall time (10%-90%)	eUSB2 specification	2		6	ns
T_{RF_MM}	Transmit rise/fall mismatch	eUSB2 specification			25	%

Timing Requirements

Parameter	Description	Min.	Typ.	Max.	Units
RESET Timing					
$T_{\_VDD18\_RAMP}$	Ramp time for VDD18 to reach min. 1.62V			2	ms
$T_{\_VDD33\_RAMP}$	Ramp time for VDD33 to reach min. 2.7V			2	ms
$T_{\_aRTN\_B}$	Duration for RST_N to be asserted low to complete reset while powered	10			us
$T_{\_READY}$	Time for eUSB2 interface to be ready after RST_N is de-asserted or both power suppliers reach minimum recommended voltages, whichever is later			3	ms

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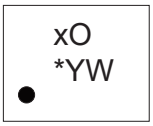
Part Marking



xO: PI3EUSB1100GHE
*: Die Rev
YW: Date Code (Year&Workweek)
● Pin 1 location
Note: If Die Rev is “0”, then there is no Die Rev character.

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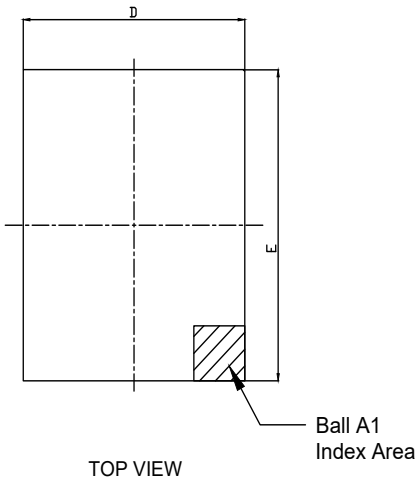
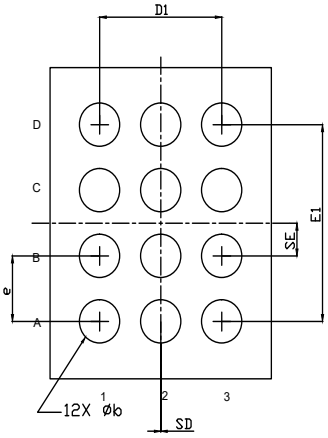
Packaging Mechanical

12-WLCSP (GH)

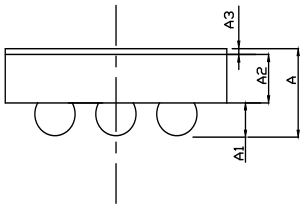


TOP VIEW

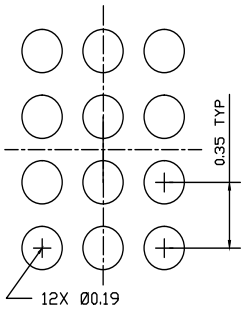


BOTTOM VIEW

PKG.	DIMENSIONS(MM)		
SYMBOL	Min.	Nom.	Max.
A	0.393	0438	0.483
A1	0.135	0.155	0.175
A2	0.238	0.258	0.278
A3	0.020	0.025	0.030
D	1.190	1.220	1.250
E	1.620	1.650	1.680
D1	0.650	0.700	0750
E1	1.000	1.050	1.100
b	0.190	0.210	0.230
e	0.350BSC		
SD	0.000BSC		
SE	0.175BSC		



SIDE VIEW



BOTTOMRECOMMEND LAND PATTERN VIEW

Note:

1. All DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

20-0494

DIODES INCORPORATED | PERICOM ENABLING SERIAL CONNECTIVITY

DATE: 08/31/20

DESCRIPTION: 12-Ball, WLCSP,1.22 x 1.65(X1-WLB1712-12)

PACKAGE CODE: GH (GH12)

DOCUMENT CONTROL #: PD-2261 **REVISION:--**

For latest package info.

Please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Orderable Part Number	Package Code	Package Description
PI3EUSB1100GHEX	GH	12-ball, 1.22 x 1.65mm (WLCSP) X1-WLB1712-12

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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