PERICOM®

PI3HDX621

3.4Gbps HDMI1.4b Active 2:1 Switch with ARC and Fast Switching

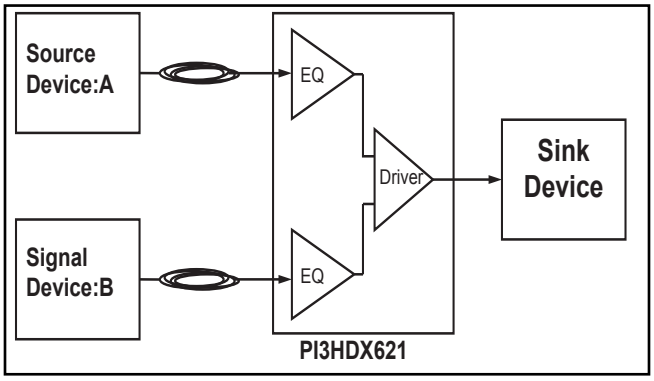
Features

- **HDMI 1.4b compliant for sink side application**
- **Operation up to 3.4 Gbps per lane**
- **Support up to 48-bit per pixel Deep Color**
- **Fast switching between two TMDS input ports**
- **Programmable equalizer, emphasis and amplitude settings to achieve optimized TMDS signal integrity**
- **Each input can be AC coupled or DC coupled, while the output will maintain TMDS compliance DC coupled, current steering signals**
- **Idle clock detection function for output squelch and auto standby**
- **Integrated ARC(Audio Return Channel) and DDC Mux**
- **Integrated ESD protection on I/O pins to connector**
- **3.3V single power supply**
- **8 KV contact per IEC61000-4-2, level 4, 8 KV HBM**
- **Industrial temperature coverage**
- **Packaging (Pb-free & Green): 48-contact LQFP (FB48)**

Application

- **Notebook Computers, Set Top Box**
- **A/V Home Entertainment Systems**
- **Dongle and Switches**

Typical Application Block Diagram



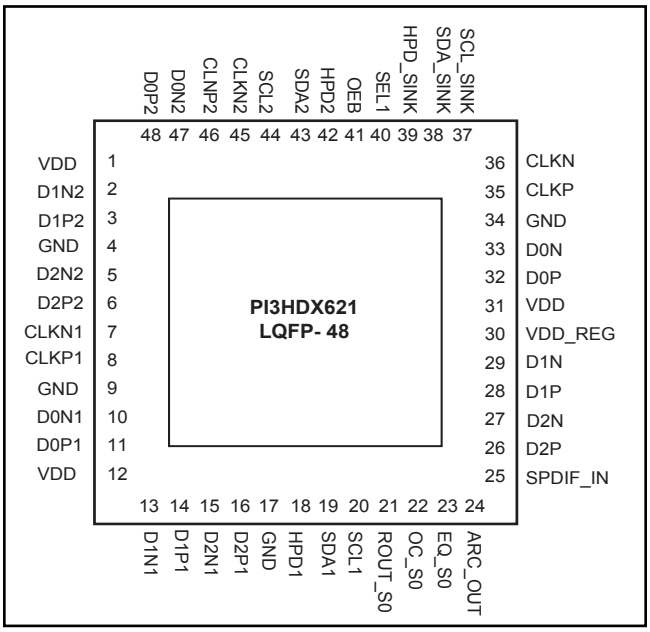
Description

PI3HDX621 is the active-type 2:1 switch compliant to HDMI 1.4b specification, featuring equalized TMDS input and pre-emphasized TMDS outputs, with 3.4 Gbps high speed and long cable application.

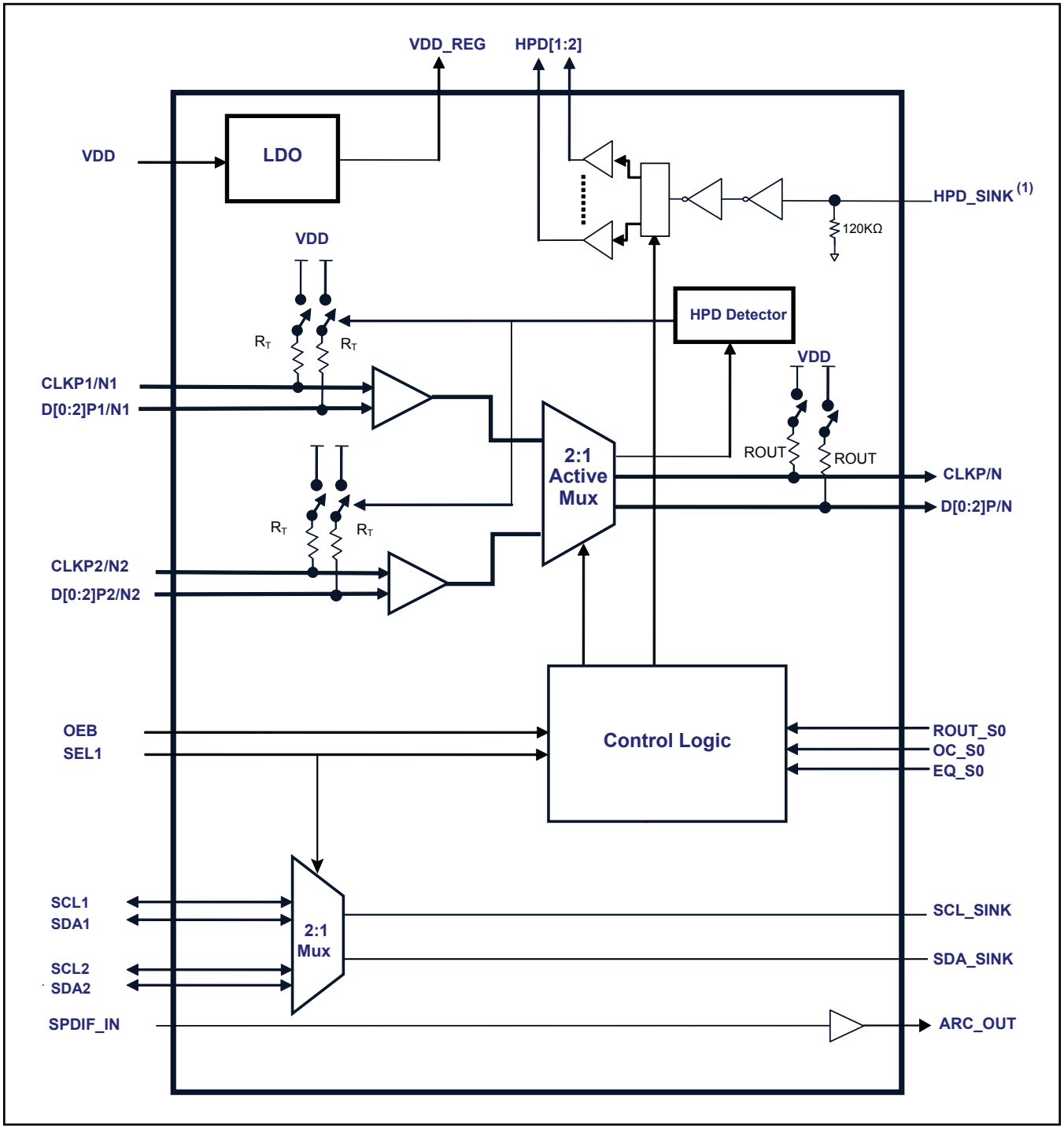
Two TMDS input ports switch fast in the built-in high speed Mux through port selection pins. Redriver boost the input signal quality, adjust known channel losses at the transmitter and restore signal integrity at the receiver. It offers doube termination or open drain output mode by output selection pin.

TMDS output can shut down to reduce power dissipation by sink side HPD detection status. DDC 2:1 Mux and ARC drivers are integrated. PI3HDX621 is specified to operate over -40 to 85 °C temperature range with 8kV ESD protection pins.

Pin Configuration



Functional Block Diagram



Note:

(1) If HPD_SINK input voltage is higher than 5V, serial resister is recommended. The resister value is about 20 -25kΩ.

Pin Description

Pin #	Pin Name	I/O[(1)]	Description
39	HPD_SINK	I	Sink side hot plug detector input; internal pull-down at 120Kohm.
18	HPD1	O	Port 1 HPD output
42	HPD2	O	Port 2 HPD output
7 8 10 11 13 14 15 16	CLKN1 CLKP1 D0N1 D0P1 D1N1 D1P1 D2N1 D2P1	I	Port 1 TMDS inputs. Rt = 50 Ohm
45 46 47 48 2 3 5 6	CLKN2 CLKP2 D0N2 D0P2 D1N2 D1P2 D2N2 D2P2	I	Port 2 TMDS inputs. Rt = 50 Ohm
36 35 33 32 29 28 27 26	CLKN CLKP D0N D0P D1N D1P D2N D2P	O	TMDS outputs. Rout = 50 Ohm when Rout_S0 = "1"
20	SCL1	IO	Port 1 DDC Clock
44	SCL2	IO	Port 2 DDC Clock
19	SDA1	IO	Port 1 DDC Data
43	SDA2	IO	Port 2 DDC Data
37	SCL_SINK	IO	Sink side DDC Clock
38	SDA_SINK	IO	Sink side DDC Data
21	ROUT_S0	I	TMDS output termination selection. Internal 100 Kohm pull-up. See ROUT_S0 truth table for functionality. "1" or "NC": Double termination "0": Open drain output

Pin Description

Pin #	Pin Name	I/O(1)	Description
41	OEB	I	Output Enable control. Active low. Internal 100 Kohm pull-down. See truth table for functionality. "1": TMDS Port1 and Port2 Output disable "0": TMDS Port1 and Port2 Output enable
22	OC_S0	I	TMDS output pre-emphasis selection. This pin has internal 100 Kohm pull-up. See OC_S0 truth table for functionality. "0": Pre-emphasis 0 dB "1": Pre-emphasis 2.5 dB
23	EQ_S0	I	TMDS Data Input Equalization selection. This pin has an internal 100 KOhm pull-low. See EQ_S0 truth table for functionality. "0" or "NC": 9 dB "1": 15 dB TMDS Clock inputs is always set as 3 dB EQ
40	SEL1	I	PORT1 or PORT2 selection. This pin has an internal 100 KOhm pull-up "1": Port 1 select "0": Port 2 select Please see Port Selection truth table.
25	SPDIF_IN	I	Single mode ARC signal input
24	ARC_OUT	O	Single mode ARC signal output
1, 12, 31	VDD	P	3.3V power supply
30	VDD_REG	P	LDO output for internal core power supplier. External capacitor 2.2 to 4.7 µF should be added to GND.
4, 9, 17, 34	GND	G	Ground

Note:
(1) I = Input, O = Output, IO = Bidirectional, P = Power, G = Ground.

Functional Description

Squelch

Automatic output squelch function disables TMDS output when no Input signal presents. Output Disable (Squelch) Mode uses TMDS Clock channel signal detection. When low voltage levels on the TMDS input clock signals are detected, Squelch state enables and TMDS output port signals shall disable; when the TMDS clock input signal levels are above a pre-determined threshold voltage, output ports shall return to the normal voltage swing levels.

Hot Plug Detect Sink HPD_SINK Shut Down

When HPD_SINK pin is floating or tie to GND, TMDS outputs shall shut down to sleep mode; HPD_SINK does not control DDC channel.

Pre-emphasis OC_S0 Truth Table

Configuration Pins		Functional Description		
ROUT_S0	**OC_S0**	**Single-end Vswing**	**Pre-emphasis(1)**	**Output Types**
0	0	500 mV	0 dB	Open Drain
0	1	500 mV	2.5 dB	
1	0	500 mV	0 dB	Double termination
1	1	500 mV	2.5 dB	

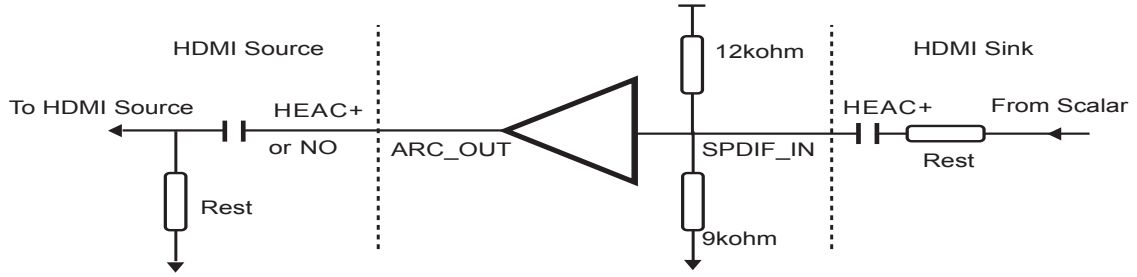
Note:
(1) TMDS Clock Pre-emphasis is fixed 0 dB.

Port Selection SEL1 Truth Table

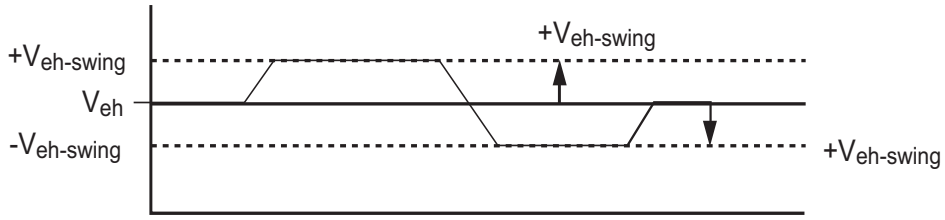
Configuration Pins		Functional Description		
OEB	**SEL1**	**TMDS Port**	**DDC port**	**HPD port**
0	1	CLKN/P1, D0N/P1, D1N/P1,D2N/P1	SCL1/SDA1	HPD1
0	0	CLKN/P2, D0N/P2, D1N/P2,D2N/P2	SCL2/SDA2	HPD2
1	X	OFF	Follow SEL1	Follow SEL1

Audio Return Channel(ARC)

There are two ARC input modes, common mode and single mode input. This device can supports "single mode input" only.

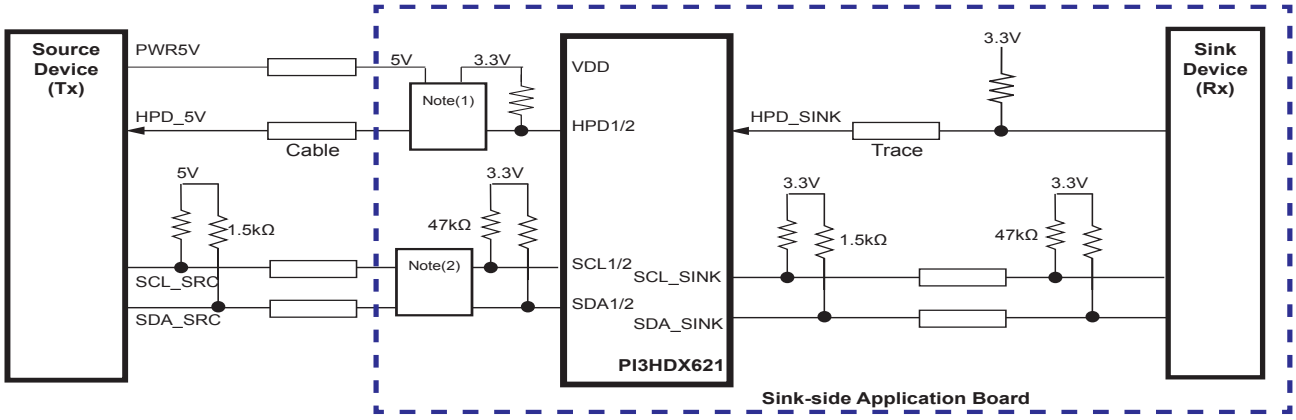


ARC single mode input and output



V_{eh} = 0~5V, $+V_{eh\text{-}swing}$ = 250mV, $-V_{eh\text{-}swing}$ = 250mV

ARC single mode signal output waveform



Typical DDC, HPD application block diagram

Note:

(1) When source device provides 5V power supply, two external BJTs is recommended with 1kΩ pull-up with PWR5V(5V), another pull-up resistor with VDD(3.3V). HPD1/HPD2 outputs are open-drain type with external pull-up resistor requirement.

(2) Also source device DDCs are recommends to use external FETs as a voltage level-shifter for the highly reliable system design.

Absolute Maximum Ratings

Item	Rating
Supply Voltage to Ground Potential	4.5V
All Inputs and Outputs	-0.5V to 4.5V
Storage Temperature	-65 to +150°C
Junction Temperature	150°C
Soldering Temperature	260°C

Note: Stress beyond those lists under "Absolute Maximum Ratings" may cause permanent damage to the device

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Unit
Ambient Operating Temperature	-40	25	85	°C
Power Supply Voltage (measured in respect to GND)	3.0	3.3	3.6	V

Electrical Specification

Parameter	Parameter	Conditions	Min.	Typ.	Max.	Unit
VDD	Operating Voltage		3.0	3.3	3.6	V
IDD	VDD Supply Current	Output Enable (open drain 500 mV single-ended, 0 dB pre-emphasis)		120	150	mA
		Output Enable (double termination, 500 mV single-ended, 0 dB pre-emphasis)		190	230	mA
IDD_SQLH	Supply Current in squelch mode	VDD=3.6V HPD_SINK=3.6V		11	13	mA
ISTB	Standby mode	VDD = 3.6V, HPD_x = 0V, ARC_OUT = 0, OEB = High		4	5	mA
VOL_HPD	Open Drain Output Low Voltage	IOL = 4 mA	0		0.4	V
IOFF_HPD	Off leakage current	VDD = 0V, VIN = 3.6V			20	µA
IOZ_HPD	Output leakage current	VDD = 3.6V, VIN = 3.6V			20	

HPD_SINK

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
IIH	High level digital input current	VIH = VDD	-25		40	µA
IIL	Low level digital input current	VIL = GND	-10		10	µA
VIH	High level digital input voltage	VDD = 3.3V	2.0			V
VIL	Low level digital input voltage		0		0.8	V

Control Pin (OEB)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
IIH	High level digital input current	VIH =VDD	-30		45	µA
IIL	Low level digital input current	VIL = GND	-10		10	µA
VIH	High level digital input voltage		2.0			V
VIL	Low level digital input voltage		0		0.8	V

DDC Channel Block

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
ILK	Input leakage current	DDC switch is OFF	-10		40	µA
CIO	Input/Output capacitance	VIpeak-peak = 1V, 100 KHz		10		pF
RON	On resistance	IO = 3mA, VO = 0.4V		25	50	Ω
VPASS	Switch Output voltage	VI=3.3V, II=100uA VDD=3.3V	1.5	2.0	2.5	V

SPDIF & ARC Pins

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
IIH_SPDIF	High level input current	VDD=3.6V, VIH=3.6V		500		µA
IIL_SPDIF	Low level input current	VDD=3.6V, VIL= GND		-350		µA
VEL	Single mode input/output Vel DC voltage level		0		5.0	V
VEL_SWING_SPDIF	Single mode input swing		0.2		0.6	V
VEL_SWING_ARC_OUT	Single mode ARC output swing		0.4	0.5	0.6	V
RO	Output resistance of ARC output stage			55		Ω
tR	ARC output rise time (10% to 90%)	< 0.4UI (f_{clock} = 6.144MHz)			25	ns
tF	ARC output fall time (10% to 90%)	< 0.4UI (f_{clock} = 6.144MHz)			25	ns
tJPP	ARC signal peak to peak jitter	< 0.4UI (f_{clock} = 6.144MHz)			3	ns

TMDS Differential Pins

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VOH	Single-ended high level output voltage	VDD=3.3V, ROUT=50Ω	VDD-10		VDD+10	mV
VOL	Single-ended low level output voltage		VDD-600		VDD-400	mV
VSWING	Single-ended output swing voltage		400		600	mV
VOD(O)	Overshoot of output differential voltage (1)				180*1	mV
VOD(U)	Undershoot of output differential voltage (2)				200*2	mV
VOC(SS)	Change in steady-state common-mode output voltage between logic				5	mV
IOS	Short Circuit output current		-12		12	mA
	Short Circuit output current at double termination mode		-24		24	mA
$VI_{(open)}$	Single-ended input voltage under high impedance input or open	II=10uA	VDD-10		VDD+10	mV
RT	Input termination resistance	VIN=2.9V	45	50	55	Ω
IOZ	Leakage current with Hi-Z I/O	VDD=3.6V			10	µA

Note:
(1) Overshoot of output differential voltage VOD(O) = (VSWING(MAX) * 2) * 15%
(2) Undershoot of output differential voltage VOD(O) = (VSWING(MIN) * 2) * 25%

TMDS Differential Pins

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
tPD	Propagation delay	V_{DD} = 3.3V, Rout = 50 Ohm			2000	ps
tR	Differential output signal rise time (20% - 80%)				190	
tF	Differential output signal fall time (20% - 80%)				190	
$tSK_{(p)}$	Pulse skew			10	50	
$tSK_{(D)}$	Intra-pair differential skew			23	50	
$tSK_{(O)}$	Inter-pair differential skew				100	
$tJIT_{(pp)}$	Peak-to-peak output jitter CLK residual jitter	CLK Input = 300MHz clock		15	30	
$tJIT_{(pp)}$	Peak-to-peak output jitter DATA Residual Jitter			18	50	
tSX	Select to switch output				10	
tEN	Enable time				1	us
tDIS	Disable time				10	ns

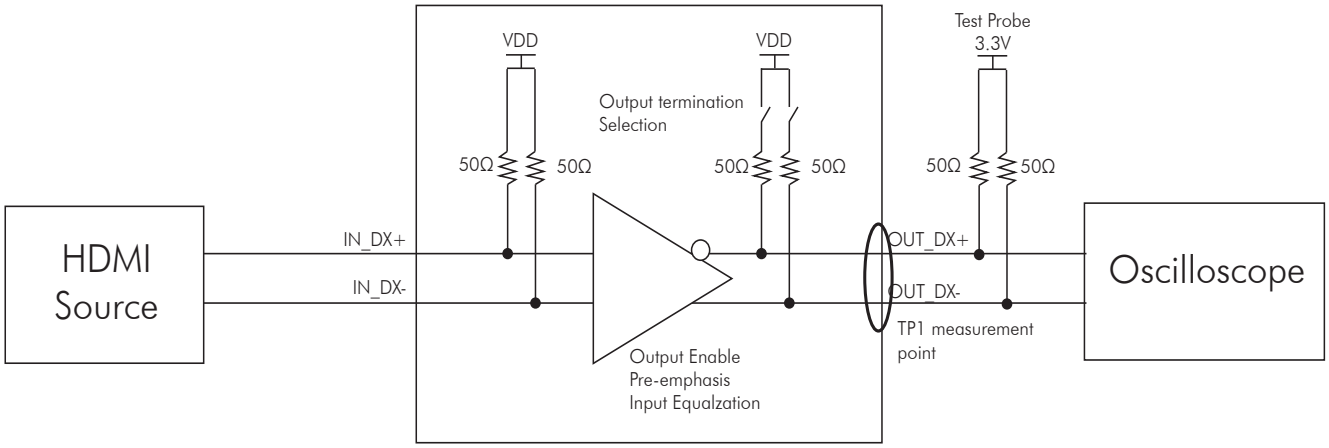
DDC I/O Pins (SCL, SCL_SINK, SDA, SDA_SINK)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$tPD_{(DDC)}$	Propagation Delay	C_L = 10pF		0.4	2.5	ns

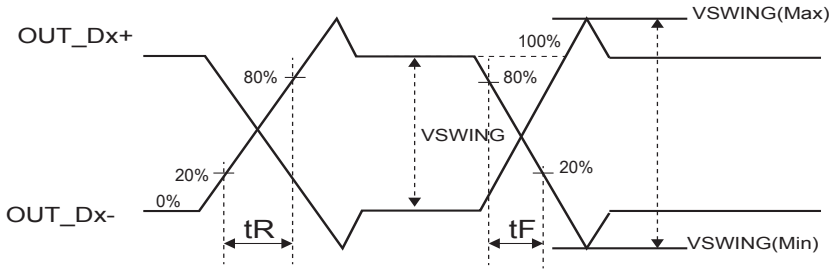
Control and Status Pins (HPD_SINK, HPD)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$tPD_{(HPD)}$	Propagation Delay	C_L = 10pF, Pull-up resistor=1 Kohm Open drain output		10		ns
$tSX_{(HPD)}$	Select to switch output			10		ns

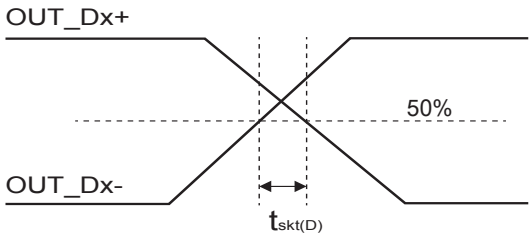
Test Setup of DC-coupled TMDS Input Measurement



Rise/Fall Time and Single-ended Swing Voltage

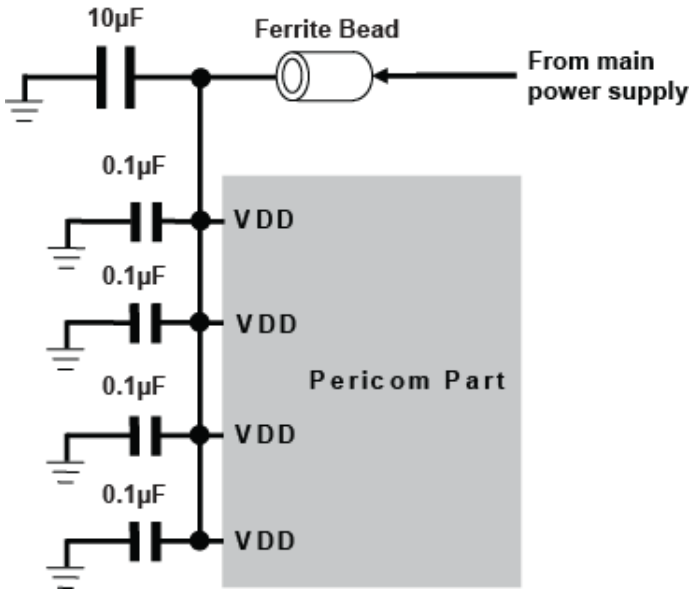


Intra-pair Skew Definition



Power Supply Decoupling Circuit

It is recommended to put 0.1 µF decoupling capacitors on each VDD pins of our part, there are four 0.1 µF decoupling capacitors are put in Figure 1 with an assumption of only four VDD pins on our part, if there is more or less VDD pins on our Pericom parts, the number of 0.1 µF decoupling capacitors should be adjusted according to the actual number of VDD pins. On top of 0.1 µF decoupling capacitors on each VDD pins, it is recommended to put a 10 µF decoupling capacitor near our part's VDD, it is for stabilizing the power supply for our part. Ferrite bead is also recommended for isolating the power supply for our part and other power supplies in other parts of the circuit. But, it is optional and depends on the power supply conditions of other circuits.



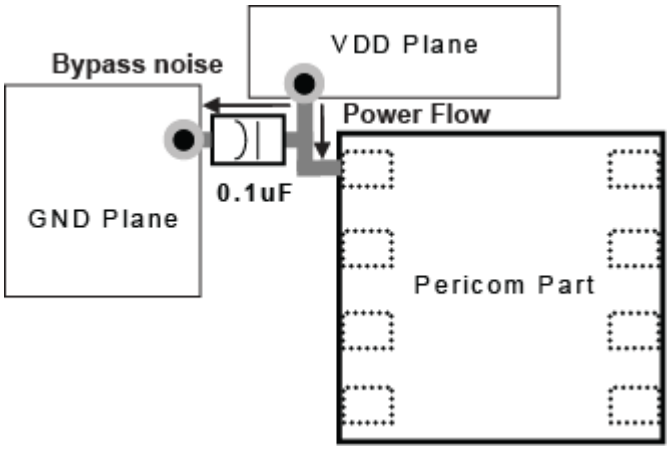
Recommended Power Supply Decoupling Capacitor Diagram

Requirements on the De-coupling Capacitors

There is no special requirement on the material of the capacitors. Ceramic capacitors are generally being used with typically materials of X5R or X7R.

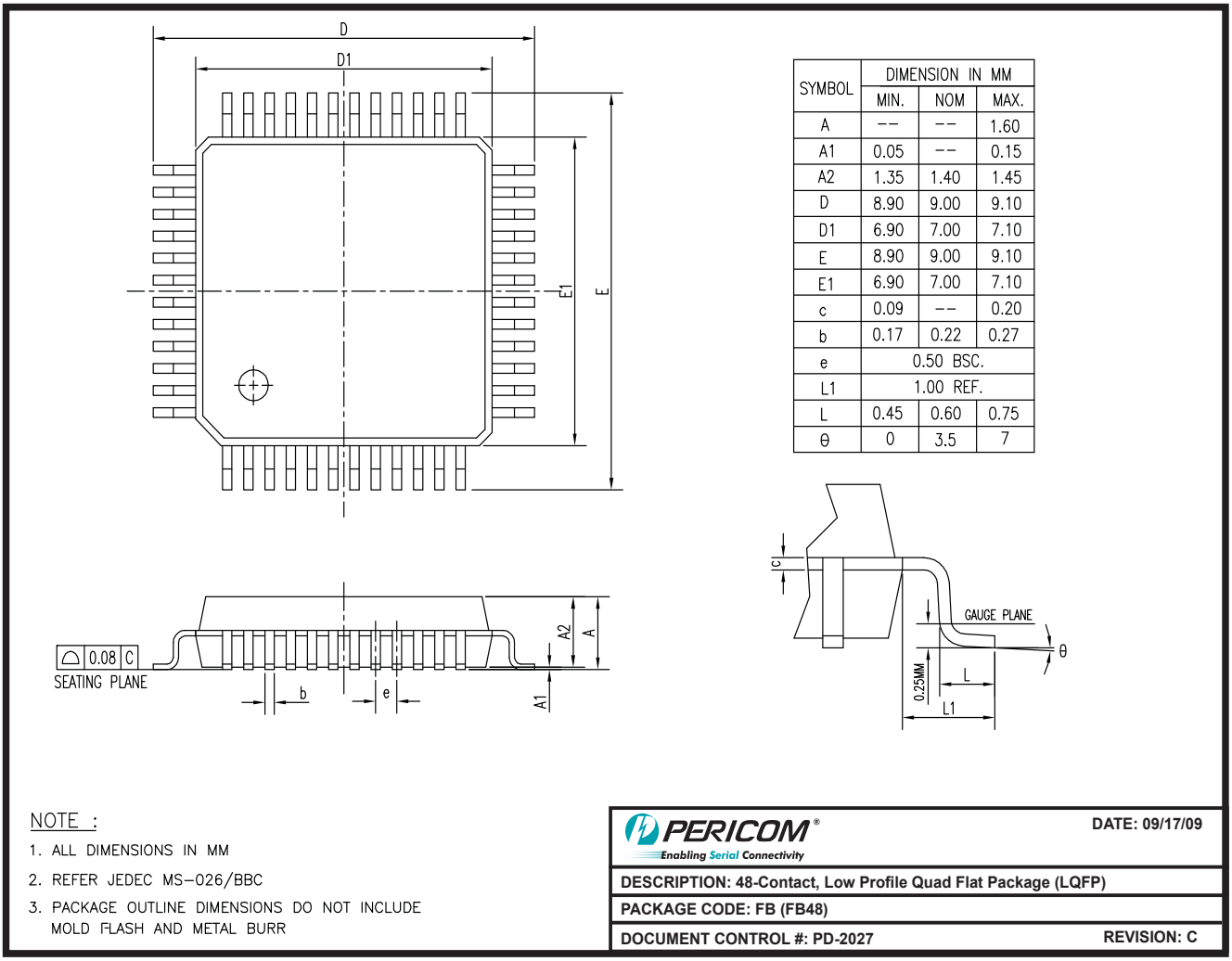
Layout and Decoupling Capacitor Placement Consideration

- Each 0.1 µF decoupling capacitor should be placed as close as possible to each VDD pin.
- VDD and GND planes should be used to provide a low impedance path for power and ground.
- Via holes should be placed to connect to VDD and GND planes directly.
- Trace should be as wide as possible
- Trace should be as short as possible.
- The placement of decoupling capacitor and the way of routing trace should consider the power flowing criteria.
- 10 µF Capacitor should also be placed closed to our part and should be placed in the middle location of 0.1 µF capacitors.
- Avoid the large current circuit placed close to our part; especially when it is shared the same VDD and GND planes. Since large current flowing on our VDD or GND planes will generate a potential variation on the VDD or GND of our part.



Decoupling Capacitor Placement Diagram

Packaging Mechanical: 48-Contact LQFP (FB)



SYMBOL	DIMENSION IN MM		
	MIN.	NOM	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
D	8.90	9.00	9.10
D1	6.90	7.00	7.10
E	8.90	9.00	9.10
E1	6.90	7.00	7.10
c	0.09	--	0.20
b	0.17	0.22	0.27
e	0.50 BSC.		
L1	1.00 REF.		
L	0.45	0.60	0.75
θ	0	3.5	7

NOTE :
1. ALL DIMENSIONS IN MM
2. REFER JEDEC MS-026/BBC
3. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BURR

PERICOM Enabling Serial Connectivity — DATE: 09/17/09

DESCRIPTION: 48-Contact, Low Profile Quad Flat Package (LQFP)

PACKAGE CODE: FB (FB48)

DOCUMENT CONTROL #: PD-2027 — REVISION: C

Please check for the latest package information on the Pericom web site at www.pericom.com/support/packaging/

Ordering Information

Ordering Number	Package Code	Package Description
PI3HDX621FBE	FB	Pb-free & Green 48-Contact LQFP

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- X suffix = Tape/Reel

Related Products

Part Number	Product Description
PI3WVR12612	Wide Voltage Range DisplayPort™ & HDMI Video Switch
PI3HDX1204-B	HDMI2.0 Redriver and Displayport Level Shifter for 6Gbps Application
PI3EQXDP1201	Displayport 1.2 redriver with built-in auto test mode
PI3HDX414	1:4 Active 3.4Gbps HDMI1.4b Splitter/DeMux with Signal Conditioning
PI3HDX412BD	1:2 Active 3.4Gbps HDMI1.4b Splitter/DeMux with Signal Conditioning
PI3HDX511F	Low power HDMI 1.4b 3.4Gbps redriver & Displayport dual mode level shifter
PI3HDMI336	3:1 Active 2.5Gbps HDMI Switch with I2C control and ARC Transmitter

Reference Information

Document	Description
HDMI1.4b	High-Definition Multimedia Interface Specification Version 1.4b, HDMI Licensing, LLC