A product Line of
Diodes Incorporated

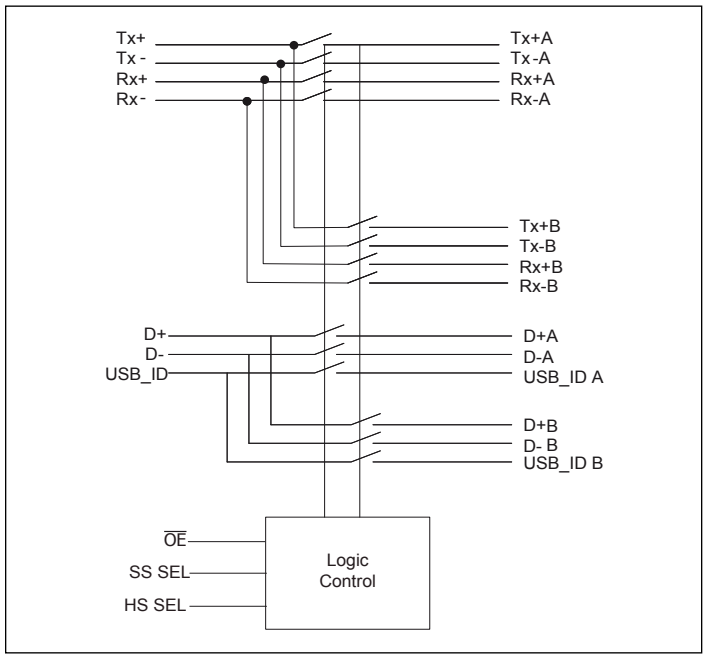
PI3USB3102Q

Automotive USB3.0 and USB2.0 Combo Switch

Features

- AEC-Q 100 Qualified
- 1:2 mux/demux for USB 3.0SS, 2.0HS, and 2.0FS signals
- Switches Tx, Rx, Dx, and USB_ID from USB3.0 connector
- Insertion Loss for superspeed channels @ 2.5 GHz: -1.7dB
- -3dB Bandwidth for superspeed channels: 4.7GHz
- Return loss for superspeed channels @ 2.5GHz: -16dB
- Low Bit-to-Bit Skew, 7ps max (between '+' and '-' bits)
- Low Crosstalk for superspeed channels: -25dB@5.0 Gbps
- Low Off Isolation for superspeed channels: -25dB@5.0 Gbps
- V_{DD} Operating Range: 3.3V +/-10%
- ESD Tolerance: 2kV HBM
- Low channel-to-channel skew, 35ps max
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. “Green” Device (Note 3)
- Packaging (Pb-free & Green):
  - 32 TQFN (ZL)

Block Diagram



Description

Diodes' PI3USB3102Q USB3.0 and USB2.0 Combo Switch is a complete 1:2 switching solution for SuperSpeed USB 3.0 signals. PI3USB3102Q provides differential high-speed lanes for the USB3.0 4.8 Gbps TX and RX lanes as well as a differential lane for 480 Mbps USB 2.0 signals and the USB_ID signal.

PI3USB3102Q can be used to connect two hosts to a single device or a single host to two devices.

PI3USB3102Q offers excellent signal integrity for high-speed signals and low power dissipation. Insertion loss is 1.7 dB and return loss is -16 dB at 2.5 GHz. Power dissipation is 6.6 mW maximum.

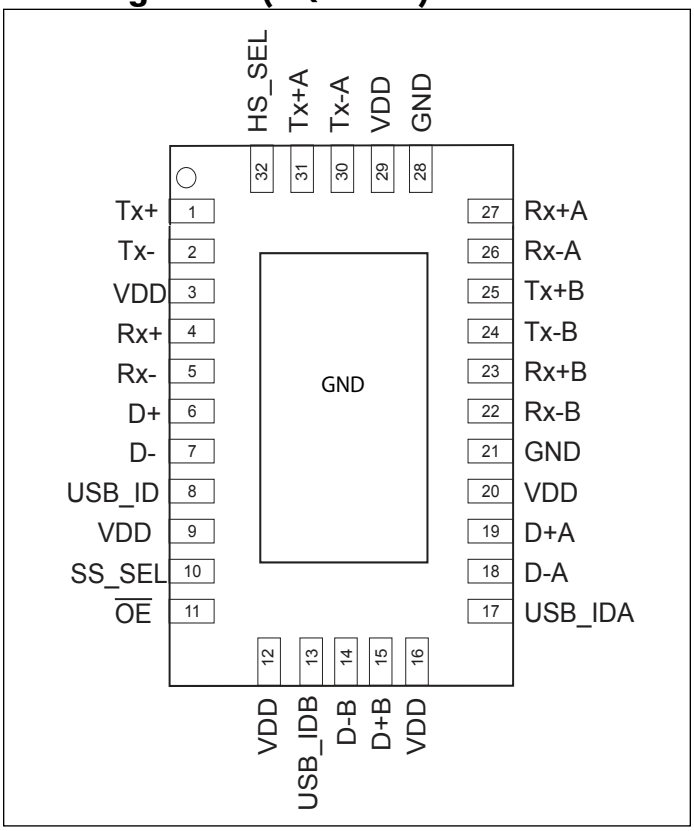
Application

Routing of USB3.0 signals with low signal attenuation between source and sink.

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Assignment (TQFN-32)



Truth Table

$\overline{OE}$	SS_SEL	HS_SEL	Function
Low	Low	Low	Port A active for all channels
Low	Low	High	Port A for SS, port B for HS and ID
Low	High	Low	Port B for SS, port A for HS and ID
Low	High	High	Port B active for all channels
High	x	x	I/O's are hi-z and IC is power down

Pin Description

Pin#	Pin Name	Signal Type	Description
1	Tx+	I/O	positive differential USB3.0 Tx signal for COM port
2	Tx-	I/O	negative differential USB3.0 Tx signal for COM port
3	VDD	Power	3.3V +/-10% power supply
4	Rx+	I/O	positive differential USB3.0 Rx signal for COM port
5	Rx-	I/O	negative differential USB3.0 Rx signal for COM port
6	D+	I/O	positive differential USB2.0 signal for COM port
7	D-	I/O	negative differential USB2.0 signal for COM port
8	USB_ID	I/O	USB_ID for COM port
9	VDD	Power	3.3V +/-10% power supply
10	SS_SEL	I	switch logic control for SuperSpeed Path If HIGH, then path B is selected for SuperSpeed channels only If LOW, then path A is selected for SuperSpeed channels only
11	$\overline{OE}$	I	Output enable. if $\overline{OE}$ is low, IC is enabled. If $\overline{OE}$ is high, then IC is power down and all I/Os are hi-z
12	VDD	Power	3.3V +/-10% power supply
13	USB_IDB	I/O	USB_ID for port B
14	D-B	I/O	negative differential USB2.0 signal for port B
15	D+B	I/O	positive differential USB2.0 signal for port B
16	VDD	Power	3.3V +/-10% power supply
17	USB_IDA	I/O	USB_ID for port A
18	D-A	I/O	negative differential USB2.0 signal for port A
19	D+A	I/O	positive differential USB2.0 signal for port A
20	VDD	Power	3.3V +/-10% power supply
21	GND	Ground	Ground
22	Rx-B	I/O	negative differential USB3.0 Rx signal for port B
23	Rx+B	I/O	positive differential USB3.0 Rx signal for port B
24	Tx-B	I/O	negative differential USB3.0 Tx signal for port B
25	Tx+B	I/O	positive differential USB3.0 Tx signal for port B
26	Rx-A	I/O	negative differential USB3.0 Rx signal for port A
27	Rx+A	I/O	positive differential USB3.0 Rx signal for port A
28	GND	Ground	Ground
29	VDD	Power	3.3V +/-10% power supply
30	Tx-A	I/O	negative differential USB3.0 Tx signal for port A
31	Tx+A	I/O	positive differential USB3.0 Tx signal for port A
32	HS_SEL	I	switch logic control for USB2.0 (D+/-) and USB_ID path If High, path B is selected If LOW, path A is selected

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C
Supply Voltage to Ground Potential ..... –0.5V to +4.2V
DC Input Voltage ..... –0.5V to V_{DD}
DC Output Current 120mA
Power Dissipation 0.5W
ESD:
HBM per AEC-Q 100-002 (All Pins)..... 2000V
CDM per AEC-Q 100-011 (All Pins) 250V

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics for Switching over Operating Range

(TA = –40°C to +85°C, VDD = 3.3V ±10%)

Parameter	Description	Test Conditions(1)	Min.	Typ.(1)	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed HIGH level	1.5			V
V_{IL}	Input LOW Voltage	Guaranteed LOW level			0.75	
V_{IK}	Clamp Diode Voltage, Dx	V_{DD} = Max., I_{IN} = –18mA		–0.8	–1.1	
IIH	Input HIGH Current	V_{DD} = Max., V_{IN} = V_{DD}			±5	µA
I_{IL}	Input LOW Current	V_{DD} = Max., V_{IN} = GND			±5	
$I_{OFF\_HS/ID}$	I/O leakage when part is off for D+, D- and USB_ID signals only	V_{DD} = 0V, V_{INPUT} = 0V to 3.6V			20	
R_{ON_SS}	On resistance between input to output for SuperSpeed signals	V_{DD} = 3.3V, Vinput = 0V to 1V, I_{INPUT} = 20mA		10	13	Ohm
R_{ON_FS}	On resistance between input to output for USB2.0 FS signals (D+/D-)	V_{DD} = 3.3V, Vinput = 0 to 3.3V, I_{INPUT} = 20mA		7	9	Ohm
R_{ON_HS}	On resistance between input to output for USB2.0 HS signals (D+/D-)	V_{DD} = 3.3V, Vinput = -0.4V to +0.4V, I_{INPUT} = 20mA		4	6	Ohm
USB_ID_I	Input voltage tolerance on USB_ID path				5.5	V
USB_ID_O	Output voltage on USB_ID path	USB_ID input from 0V to 5.25V			3.6	V

Power Supply Characteristics (TA = –40°C to +85°C)

Parameter	Description	Test Conditions(1)	Min.	Typ.(1)	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{DD} = Max., V_{IN} = GND or V_{DD}			2	mA

Dynamic Electrical Characteristics over Operating Range (TA = -40° to +85°C, VDD = 3.3V ±10%)

Parameter	Description	Test Conditions		Typ.	Max.	Units
X_{TALK}	Crosstalk on SuperSpeed Channels	See Fig. 1 for Measurement Setup	f= 2.5 GHz	-25dB		dB
O_{IRR}	OFF Isolation on SuperSpeed Channels	See Fig. 2 for Measurement Setup	f= 2.5 GHz	-22dB		
I_{LOSS}	Differential Insertion Loss on SuperSpeed Channels	@5.0Gbps (see figure 3)		-1.7		dB
R_{loss}	Differential Return Loss on SuperSpeed channels	@ 2.5GHz		-16		dB
BW_SS	Bandwidth -3dB for SuperSpeed path (Tx±/ Rx±)	See figure 3		4.7		GHz
BW_HS	-3dB BW for USB high speed path (D+/-)	See figure 3		1.5		GHz
Tsw a-b	time it takes to switch from port A to port B				1	us
Tsw b-a	time it takes to switch from port B to port A				1	us
Tstartup	Vdd valid to channel enable				10	us
Twakeup	Enabling output by changing $\overline{OE}$ from low to High				10	us

Note:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{DD} = 3.3V, T_A = 25°C ambient and maximum loading.

Switching Characteristics (T_A= -40° to +85°C, V_{DD} = 3.3V±10%)

Parameter	Description	Min.	Typ.	Max.	Units
T_{pd}	Propagation delay (input pin to output pin)		80		ps
t_{b-b}	Bit-to-bit skew within the same differential pair		5		ps
t_{ch-ch}	Channel-to-channel skew			35	ps

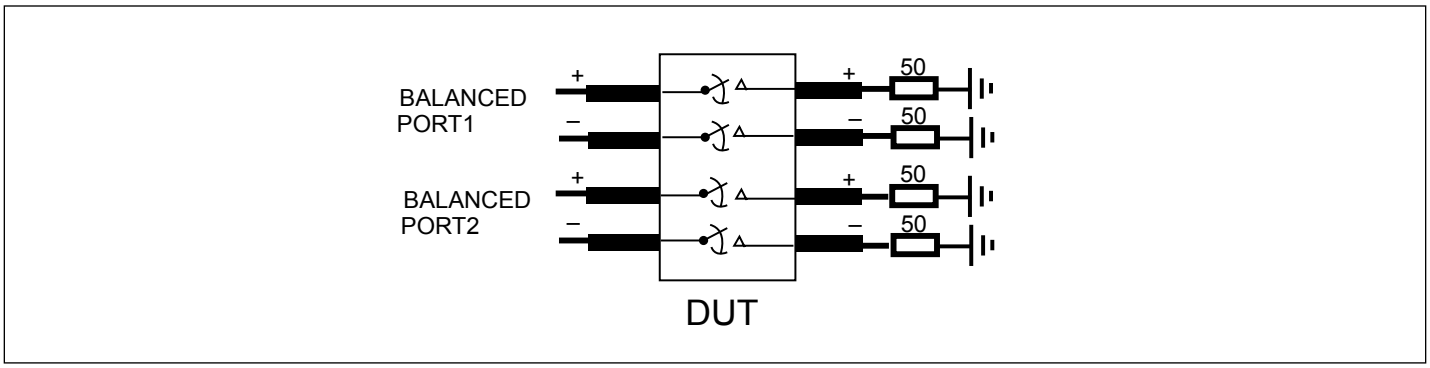


Fig 1. Crosstalk Setup

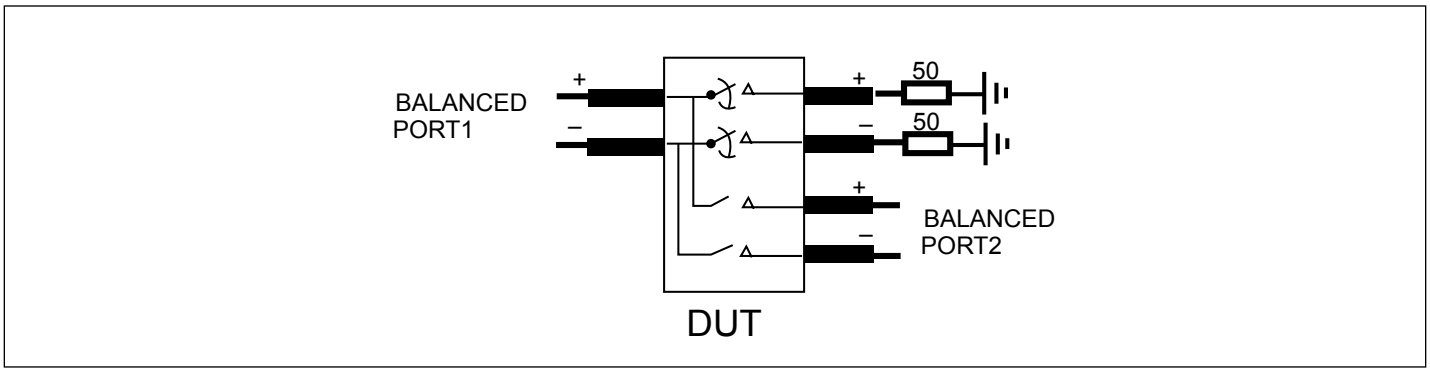


Fig 2. Off-isolation setup

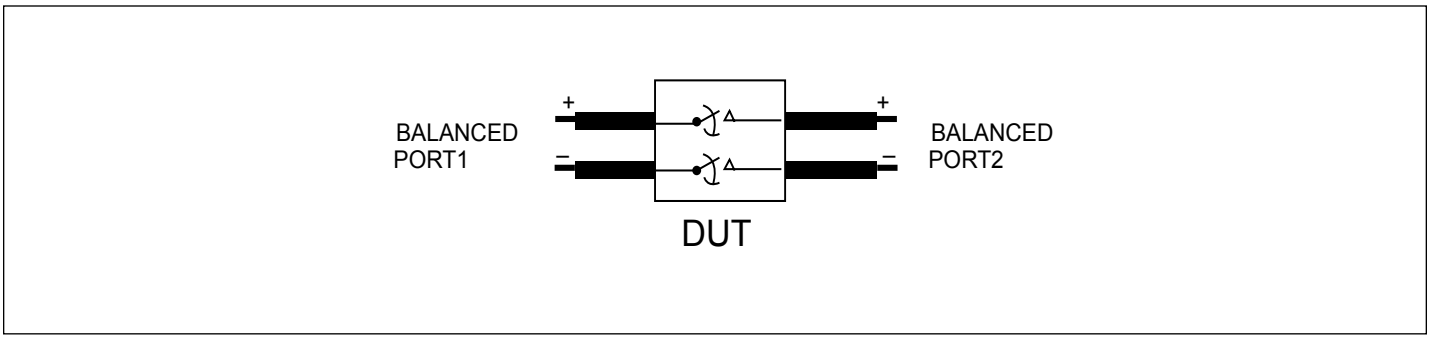


Fig 3. Differential Insertion Loss set up

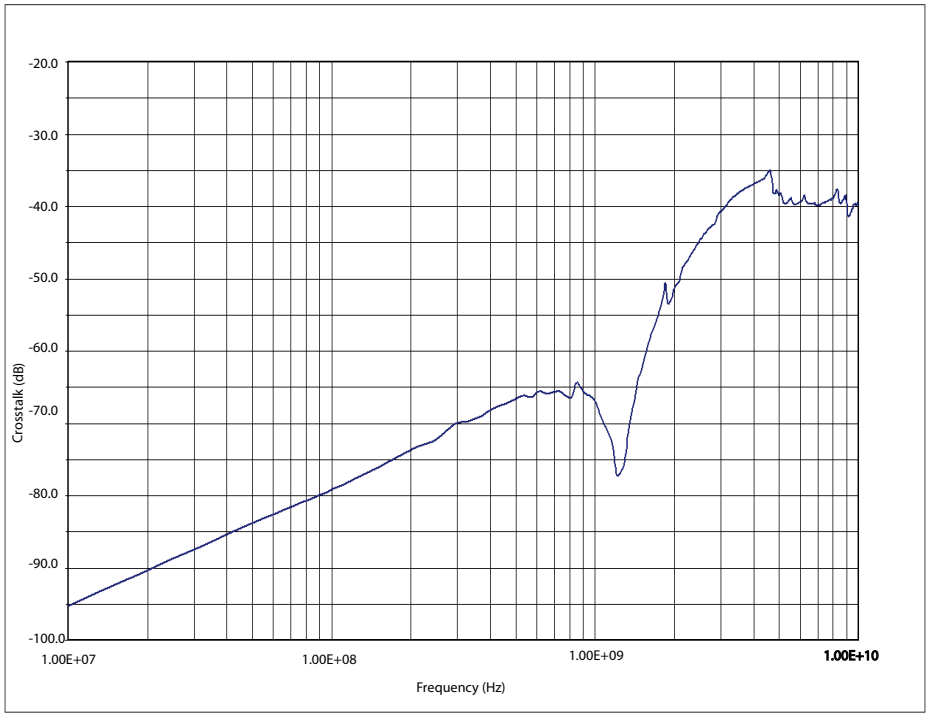


Fig 4. Xtalk for SuperSpeed channels (Tx/Rx)

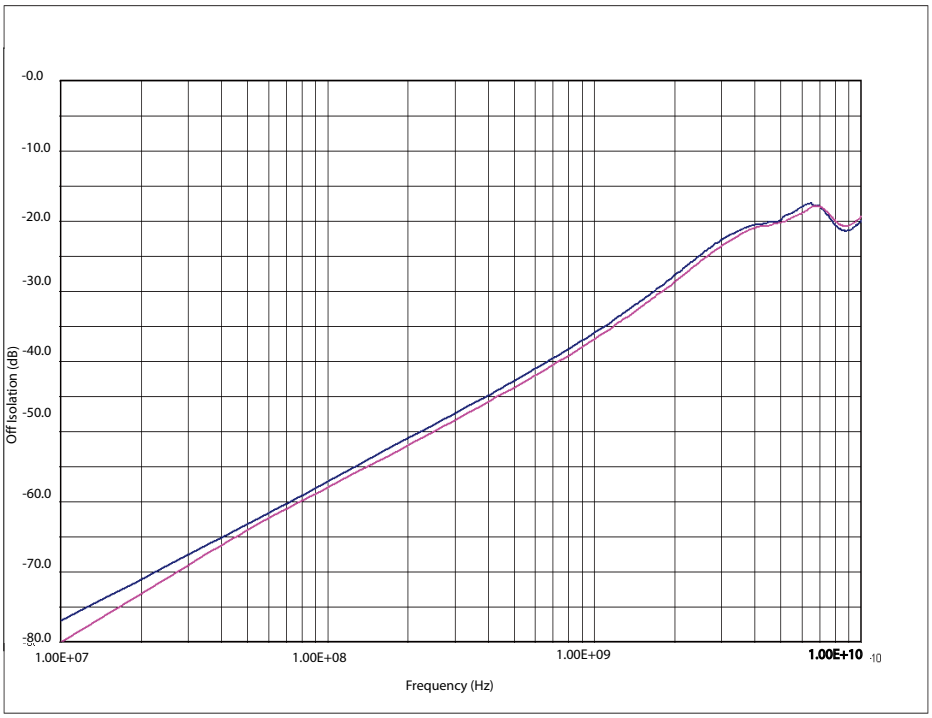


Fig 5. Off Isolation for SuperSpeed channels (Tx/Rx). Red is for path B and Blue is for path A

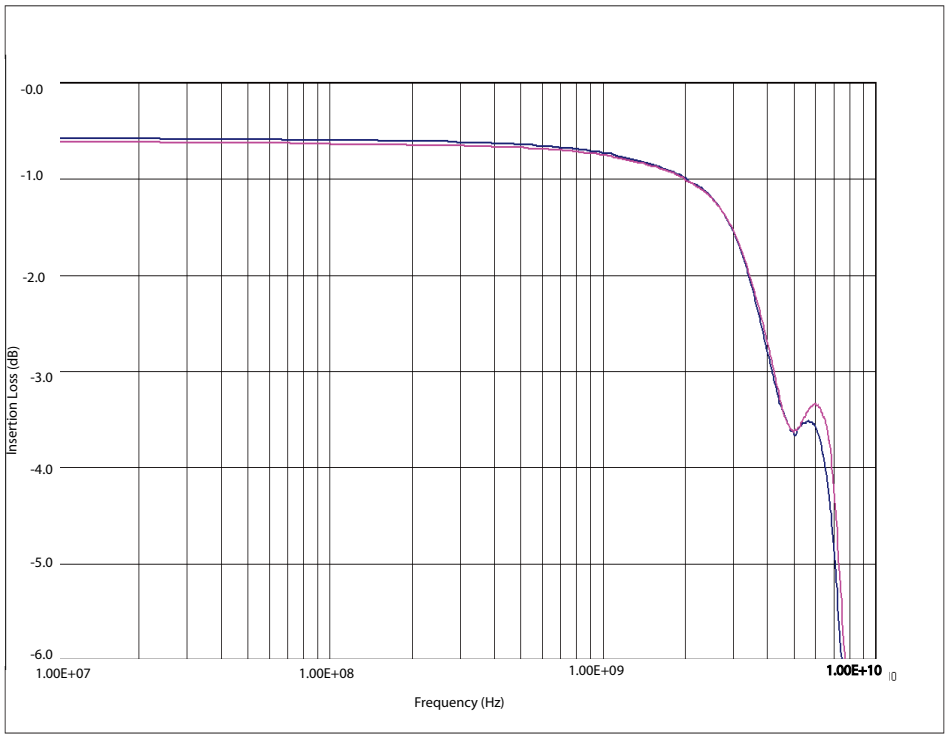
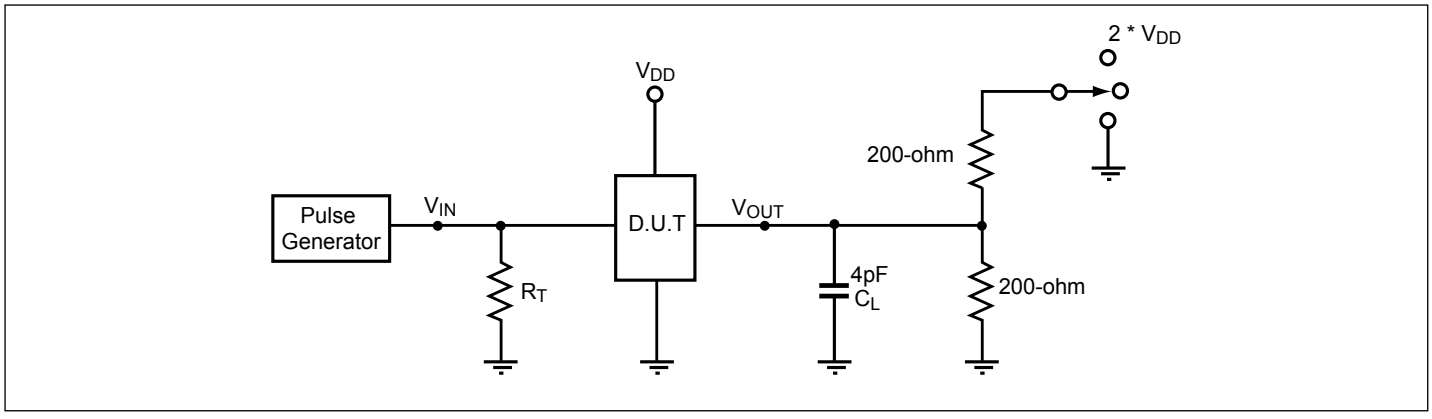


Fig 6. Insertion Loss for SuperSpeed channels (Tx/Rx). Red is for path B and Blue is for path A

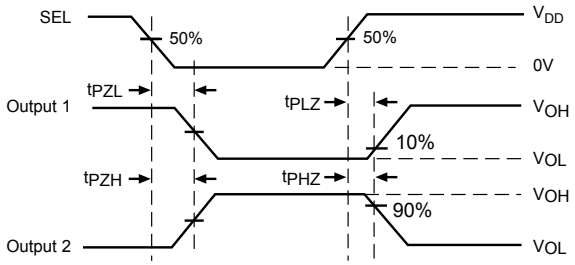
Test Circuit for Electrical Characteristics(1-5)



Notes:

1. C_L = Load capacitance: includes jig and probe capacitance.
2. R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator
3. Output 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
4. Output 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
5. All input impulses are supplied by generators having the following characteristics: PRR ≤ MHz, $Z_O = 50\Omega$, $t_R \leq 2.5$ns, $t_F \leq 2.5$ns.
6. The outputs are measured one at a time with one transition per measurement.

Switching Waveforms

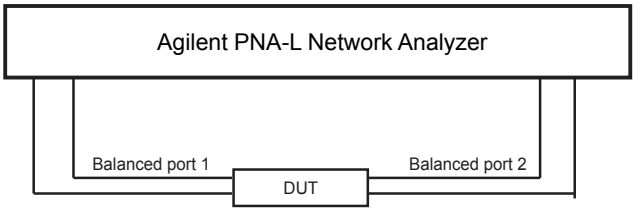


Voltage Waveforms Enable and Disable Times

Switch Positions

Test	Switch
t_{PLZ}, t_{PZL} (output on B-side)	2 * Vdd
t_{PHZ}, t_{PZH} (output on B-side)	GND
Prop Delay	Open

Test Circuit for Dynamic Electrical Characteristics



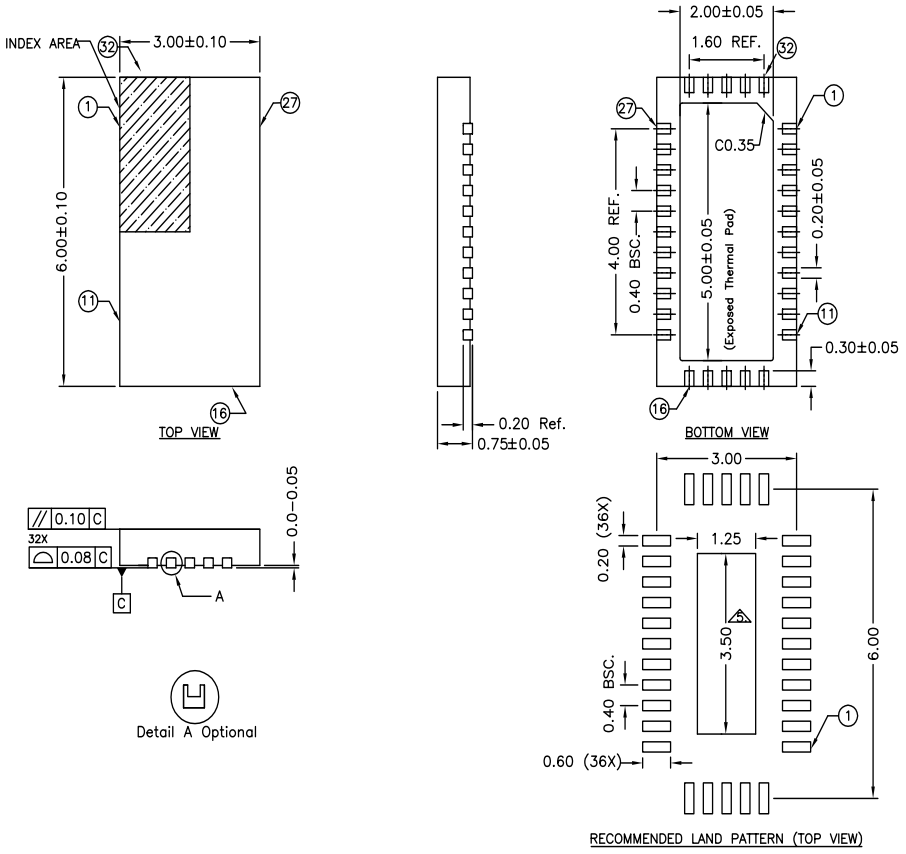
Part Marking

ZL Package

PI3USB
3102QZLE
YYWWXX

YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Site Code

Packaging Mechanical: 32-TQFN (ZL)



NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED).

DIODES INCORPORATED | PERICOM A PRODUCT LINE OF DIODES INCORPORATED — ENABLING SERIAL CONNECTIVITY

DATE: 07/05/16

DESCRIPTION: 32-Contact, Very Thin Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZL (ZL32)

DOCUMENT CONTROL #: PD-2044 REVISION: C

16-0142

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Code	Package Code	Package Description
PI3USB3102QZLEX	ZL	32-Contact, Very Thin Quad Flat No-Lead (TQFN)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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