Not Recommended for New Design - Use PI3WVR648

A Product Line of
Diodes Incorporated

PI3WVR646

2:1 MIPI D-PHY and C-PHY Switch

Description

The DIODES PI3WVR646 is a 4-data lane D-PHY or 3–data lane C–PHY MIPI switch. This 10-channel single-pole, double-throw (SPDT) switch is optimized for switching between high-speed (HS) or low-power (LP) MIPI signal. The PI3WVR646 is designed for the MIPI specification and allows connection to a CSI or DSI module.

Application(s)

- Cellular Phones, Smart Phones
- Tablets
- Laptops
- Displays

Features

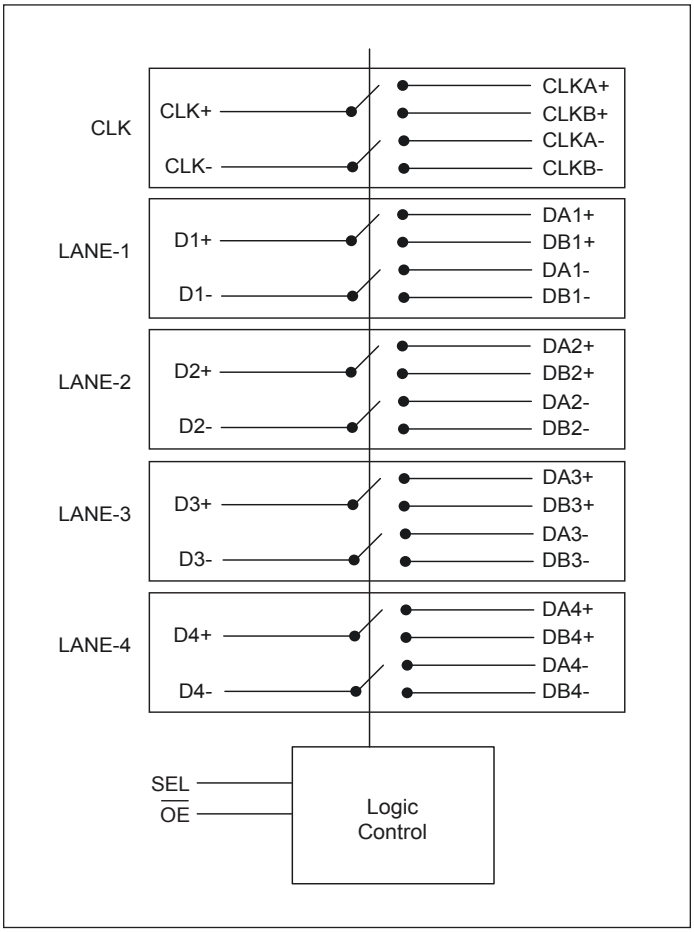
- SPDT (10x) Switch Type and Signal Type Support MIPI D-PHY, C-PHY and Other Low Speed Signal Interfaces
- Data Rate: D-PHY(2.5Gbps) 4-Data Lane and C-PHY (2.5Gsps) 3-Data Lane
- Supports 2:1 Clock Differential Signal
- -3dB Bandwidth: 4.5GHz Typical
- Low Crosstalk: -30dB @ 1.25GHz
- Low Off Isolation: -26dB @ 1.25GHz
- Input Signals:
  - 0 to 1.3V for MIPI Standard Signal Type
  - 0 to 4V for Low Speed Signals<500Mhz
- Low R_{ON}: 6Ω Typical
- Low ΔR_{ON}: 0.1Ω Typical
- Low R_{ON_FLAT}: 0.3Ω
- I_{CCZ}: 1μA Maximum
- I_{CC}: 15μA Typical
- C_{ON}: 1.5pF Typical
- Skew of Opposite Transitions of the Same Output: 2ps Typical
- V_{DD} Operating Range: 1.5V to 5V
- ESD Tolerance: 2kV HBM
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. “Green” Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/
- Packaging (Pb-free & Green):
  - 36-Pin, UWLB (GE) 2.44 × 2.44

Notes:

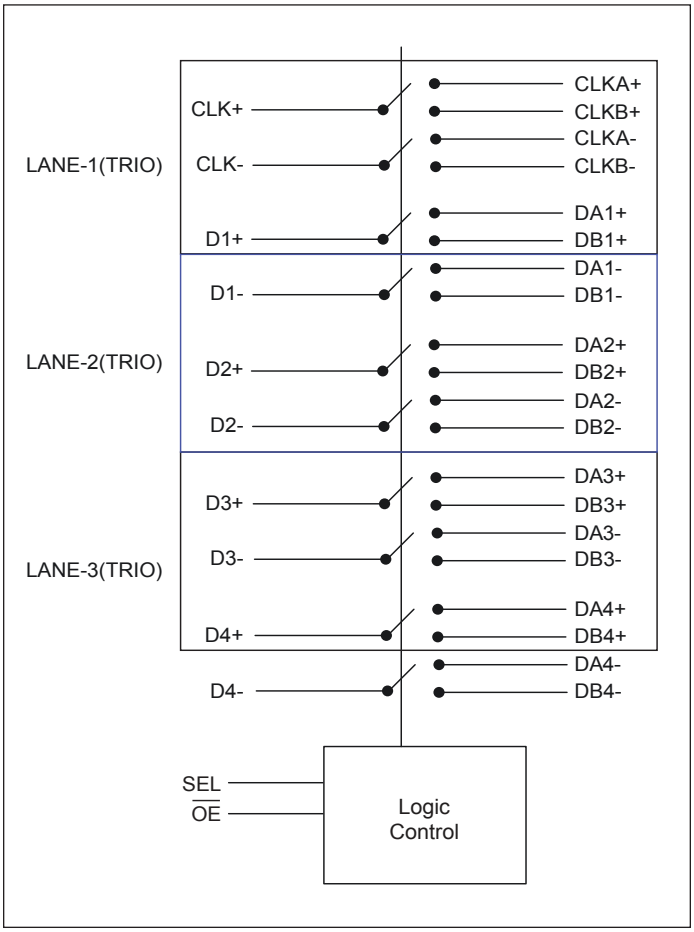
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Block Diagram

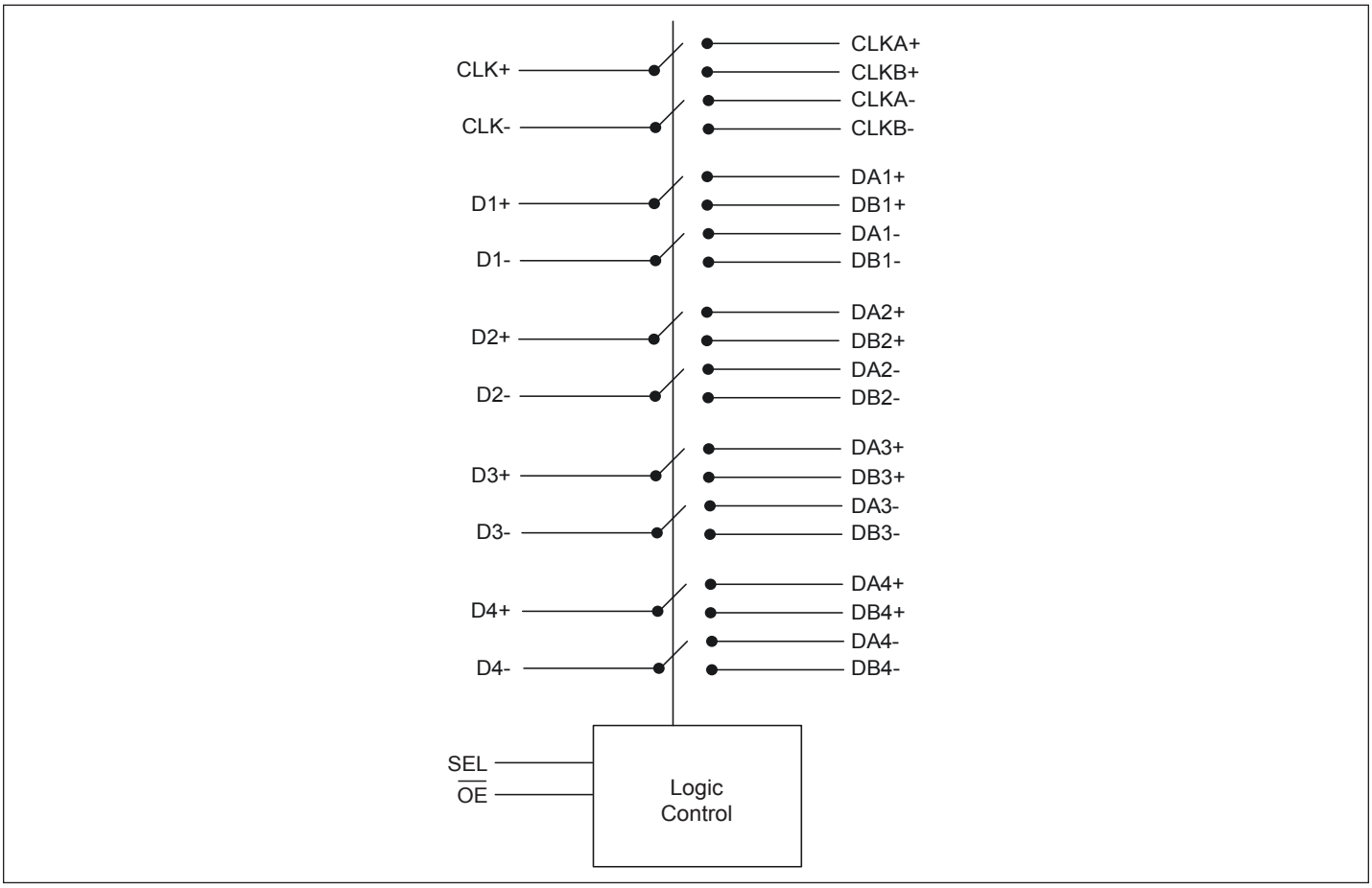
PI3WVR646 D-PHY Application



PI3WVR646 C-PHY Application



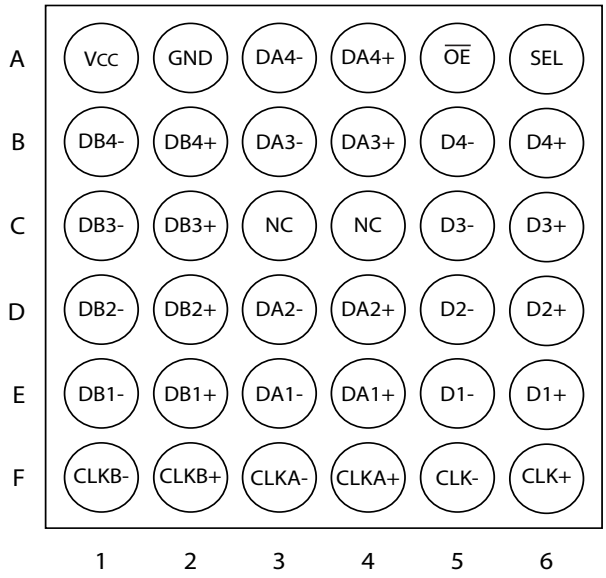
Block Diagram



Truth Table

SEL	$\overline{OE}$	Function
LOW	LOW	CLK+ = CLKA+, CLK- = CLKA-, Dn(±) = DAn(±)
HIGH	LOW	CLK+ = CLKB+, CLK- = CLKB-, Dn(±) = DBn(±)
X	HIGH	Clock and Data Ports High Impedance

Pin Configuration (Top View)



Pin Description

Pin#	Pin Name	Type	Description
A1	V_{CC}	Power	1.5V to 5V power supply
A2	GND	Ground	Ground
A3	DA4-	I/O	Negative differential signal 4 for port A
A4	DA4+	I/O	Positive differential signal 4 for port A
A5	$\overline{OE}$	I	Output enable. If $\overline{OE}$ is low, IC enables. If $\overline{OE}$ is high, IC powers down. All I/Os are Hi-Z.
A6	SEL	I/O	Switch logic control
B1	DB4-	I/O	Negative differential signal 4 for port B
B2	DB4+	I/O	Positive differential signal 4 for port B
B3	DA3-	I/O	Negative differential signal 3 for port A
B4	DA3+	I/O	Positive differential signal 3 for port A
B5	D4-	I/O	Negative differential signal 4 for COM port
B6	D4+	I/O	Positive differential signal 4 for COM port
C1	DB3-	I/O	Negative differential signal 3 for port B
C2	DB3+	I/O	Positive differential signal 3 for port B
C3, C4	NC	—	Not connected
C5	D3-	I/O	Negative differential signal 3 for COM port
C6	D3+	I/O	Positive differential signal 3 for COM port
D1	DB2-	I/O	Negative differential signal 2 for port B

Pin#	Pin Name	Type	Description
D2	DB2+	I/O	Positive differential signal 2 for port B
D3	DA2-	I/O	Negative differential signal 2 for port A
D4	DA2+	I/O	Positive differential signal 2 for port A
D5	D2-	I/O	Negative differential signal 2 for COM port
D6	D2+	I/O	Positive differential signal 2 for COM port
E1	DB1-	I/O	Negative differential signal 1 for port B
E2	DB1+	I/O	Positive differential signal 1 for port B
E3	DA1-	I/O	Negative differential signal 1 for port A
E4	DA1+	I/O	Positive differential signal 1 for port A
E5	D1-	I/O	Negative differential signal 1 for COM port
E6	D1+	I/O	Positive differential signal 1 for COM port
F1	CLKB-	I/O	Clock negative differential signal for port B
F2	CLKB+	I/O	Clock positive differential signal for port B
F3	CLKA-	I/O	Clock negative differential signal for port A
F4	CLKA+	I/O	Clock positive differential signal for port A
F5	CLK-	I/O	Clock negative differential signal for COM port
F6	CLK+	I/O	Clock positive differential signal for COM port

Absolute Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

V_{CC}, Supply Voltage, ... -0.5V to 6.0V
V_{CNTRL}, DC Input Voltage ($\overline{OE}$, SEL)(1) ..... -0.5V to V_{CC}
V_{SW}, DC Switch I/O Voltage(1,2) ..... -0.3V to 4.0V
I_{IK}, DC Input Diodes Current ..... -50mA
I_{OUT}, DC Output Current 25mA
T_{STG}, Storage Temperature ..... -65°C to +150°C
Tj, Junction Temperature ..... 125°C
ESD:
Human Body Model, JEDEC: JESD22-A114, All Pins 2.0kV
Charged Device Model, JEDEC: JESD22-C101 ..... 1.0kV

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Note:
1. The input and output negative ratings can be exceeded if the input and output diode current ratings are observed.
2. V_{SW} refers to analog data switch paths.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation.
Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications.

Symbol	Description	Test Conditions	Min.	Max.	Units
V_{CC}	Supply Voltage	—	1.5	5.0	V
V_{CNTRL}	Control Input Voltage (SEL, $\overline{OE}$)(1)	—	0	V_{CC}	V
V_{SW}	Switch I/O Voltage (CLK-, D-, CLKA-, CLKB-, DA-, DB-)	MIPI HS Mode	0	0.5	V
		MIPI LP Mode	0	1.3	V
		I2C, SPI, SDIO and other low speed signal, Frequency < 500Mhz	0	4(2)	V
T_A	Operating Temperature	—	-40	+85	°C

Note:
1. The control inputs must be held HIGH or LOW; they must not float.
2. The max Vsw is equal to VCC when VCC is smaller than 4V.

DC and Transient Characteristics

All typical values are at T_A = 25°C unless otherwise specified.

Symbol	Description	Test Conditions	V_{CC} (V)	T_A = -40°C to +85°C			Units
				Min.	Typ.	Max.	
V_{IK}	Clamp Diode Voltage ($\overline{OE}$, SEL)	I_{IN} = -18mA	1.5	-1.2	—	-0.6	V
V_{IH}	Input Voltage High	SEL, $\overline{OE}$	1.5 to 5	1.3	—	—	V
V_{IL}	Input Voltage Low	SEL, $\overline{OE}$	1.5 to 5	—	—	0.5	V

Symbol	Description	Test Conditions	V_{CC} (V)	T_A = -40°C to +85°C			Units
				Min.	Typ.	Max.	
I_{IN}	Control Input Leakage ($\overline{OE}$, SEL)	V_{CNTRL} = 0 to V_{CC}	5	-0.5		0.5	µA
$I_{NO(OFF)}$ $I_{NC(OFF)}$	Off Leakage Current of Port CLKA-, DA-, CLKB- and DB-	V_{SW} = 0.0 ≤ DATA ≤ 1.3V	5	-0.5	—	0.5	µA
$I_{A(ON)}$	On Leakage Current of Common Ports (CLK-, D-)	V_{SW} = 0.0 ≤ DATA ≤ 1.3V	5	-0.5	—	0.5	µA
I_{OFF}	Power-Off Leakage Current (All I/O Ports)	V_{SW} = 0.0 or 1.3V	0	-0.5	—	0.5	µA
I_{OZ}	Off-State Leakage	V_{SW} = 0.0 ≤ DATA ≤ 1.3V, $\overline{OE}$ = High	5	-0.5	—	0.5	µA
$R_{ON\_MIPI\_HS}$	Switch On Resistance for HS MIPI	I_{ON} = -8mA, $\overline{OE}$ = 0V, SEL = V_{CC} or 0V, CLKA, CLKB, DB- or DA- = 0.2V	1.5	—	6	9	Ω
			2.5				
			3.3				
			5				
$R_{ON\_MIPI\_LP}$	Switch On Resistance for LP MIPI	I_{ON} = -8mA, $\overline{OE}$ = 0V, SEL = V_{CC} or 0V, CLKA, CLKB, DB- or DA- = 1.2V	1.5	—	6	9	Ω
			2.5				
			3.3				
			5				
$\Delta R_{ON\_MIPI\_HS}$	On Resistance Matching Between HS MIPI Channels(1)	I_{ON} = -8mA, $\overline{OE}$ = 0V, SEL = V_{CC} or 0V, CLKA, CLKB, DB- or DA- = 0.2V	1.5	—	0.1	—	Ω
			2.5				
			3.3				
			5				
$\Delta R_{ON\_MIPI\_LP}$	On Resistance Matching Between LP MIPI Channels(1)	I_{ON} = -8mA, $\overline{OE}$ = 0V, SEL = V_{CC} or 0V, CLKA, CLKB, DB- or DA- = 1.2V	1.5	—	0.1	—	Ω
			2.5				
			3.3				
			5				
$R_{ON\_FLAT\_MIPI\_HS}$	On Resistance Flatness for HS MIPI	I_{ON} = -8mA, $\overline{OE}$ = 0V, SEL = V_{CC} or 0V, CLKA, CLKB, DB- or DA- = 0 to 0.3V	1.5	—	0.3	—	Ω
			2.5				
			3.3				
			5				
$R_{ON\_FLAT\_MIPI\_LP}$	On Resistance Flatness for LP MIPI	I_{ON} = -8mA, $\overline{OE}$ = 0V, SEL = V_{CC} or 0V, CLKA, CLKB, DB- or DA- = 0 to 1.3V	1.5	—	0.3	—	Ω
			2.5				
			3.3				
			5				
I_{CC}	Quiescent Supply Current	V_{SEL} = 0 or V_{CC}, I_{OUT} = 0, $\overline{OE}$ = 0V	5	—	15	30	µA

Symbol	Description	Test Conditions	V_{CC} (V)	T_A = -40°C to +85°C			Units
				Min.	Typ.	Max.	
I_{CCZ}	Quiescent Supply Current (High Impedance)	V_{SEL} = 0 or V_{CC}, I_{OUT} = 0, $\overline{OE}$ = VCC	5	—	—	1	µA
I_{CCT}	Increase in I_{CC} Current Per Control Voltage and V_{CC}	V_{SEL} = 0 or V_{CC}, $\overline{OE}$ = 1.5V	5	—	1	—	µA

AC Electrical Characteristics

All typical values are for V_{CC} = 3.3V and T_A = 25°C unless otherwise specified.

Symbol	Description	Test Conditions	V_{CC} (V)	T_A = -40°C to +85°C			Units
				Min.	Typ.	Max.	
t_{INIT}	Initialization Time V_{CC} to Output[1]	R_L = 50Ω, C_L = 0pF, V_{SW} = 0.6V	1.5 to 5	—	60	—	µs
t_{EN}	Enable Time $\overline{OE}$ to Output	R_L = 50Ω, C_L = 0pF, V_{SW} = 0.6V	1.5 to 5	—	60	150	µs
t_{DIS}	Disable Time $\overline{OE}$ to Output	R_L = 50Ω, C_L = 0pF, V_{SW} = 0.6V	1.5 to 5	—	35	250	ns
t_{ON}	Turn-On Time SEL to Output	R_L = 50Ω, C_L = 0pF, V_{SW} = 0.6V	1.5 to 5	—	350	1100	ns
t_{OFF}	Turn-Off Time SEL to Output	R_L = 50Ω, C_L = 0pF, V_{SW} = 0.6V	1.5 to 5	—	125	800	ns
t_{BBM}	Break-Before-Make Time	R_L = 50Ω, C_L = 0pF, V_{SW} = 0.6V	1.5 to 5	—	—	450	ns
t_{PD}	Propagation Delay[1]	C_L = 0pF, R_L = 50Ω	1.5 to 5	—	—	0.25	ns
O_{IRR}	Off Isolation for MIPI[1]	R_L = 50Ω, f = 1250MHz, $\overline{OE}$ = HIGH, V_{SW} = $0.2V_{PP}$	1.5 to 5	—	-26	—	dB
X_{TALK}	Crosstalk for MIPI[1]	R_L = 50Ω, f = 1250MHz, SEL = HIGH, V_{SW} = $0.2V_{PP}$	1.5 to 5	—	—	-30	dB
		R_L = 50Ω, f = 1250MHz, SEL = LOW, V_{SW} = $0.2V_{PP}$		—	—	-30	
I_{LOSS}	Insertion Loss[1]	R_L = 50Ω, C_L = 0pF, f = 1250MHz, V_{SW} = $0.2V_{PP}$	1.5 to 5	—	-0.9	—	dB
		R_L = 50Ω, C_L = 0pF, f = 750MHz, V_{SW} = $0.2V_{PP}$	1.5 to 5	—	-0.7	—	
BW	-3db Bandwidth[1]	R_L = 50Ω, C_L = 0pF, V_{SW} = $0.2V_{PP}$	1.5 to 5	3.0	4.5	—	GHz

Note:

1. Guaranteed by characterization.

High-Speed-Related AC Electrical Characteristics

Symbol	Description	Test Conditions	V_{CC} (V)	T_A = -40°C to +85°C			Units
				Min.	Typ.	Max.	
$t_{SK(P)}$	HS Mode Skew of Opposite Transitions of the Same Output(1)	R_L = 50Ω, C_L = 0pF, V_{SW} = 0.3V	1.5 to 5	—	2	4	ps
	HS Mode Slew of all Group A or Group B Channels(1)	R_L = 50Ω, C_L = 0pF, V_{SW} = 0.3V	1.5 to 5	—	4	7	

Note:

1. Guaranteed by characterization.

Capacitance

Symbol	Description	Test Conditions	T_A = -40°C to +85°C			Units
			Min.	Typ.	Max.	
C_{IN}	Control Pin Input Capacitance(1)	V_{CC} = 0V, f = 1MHz	—	2.1	—	pF
C_{ON}	On Capacitance(1)	V_{CC} = 3.3V, $\overline{OE}$ = 0V, f = 1250MHz (in HS common value)	—	1.5	—	pF
C_{OFF}	Off Capacitance(1)	V_{CC} or $\overline{OE}$ = 3.3V, f = 1250MHz (both sides in HS common value)	—	0.9	—	pF

Note:

1. Guaranteed by characterization.

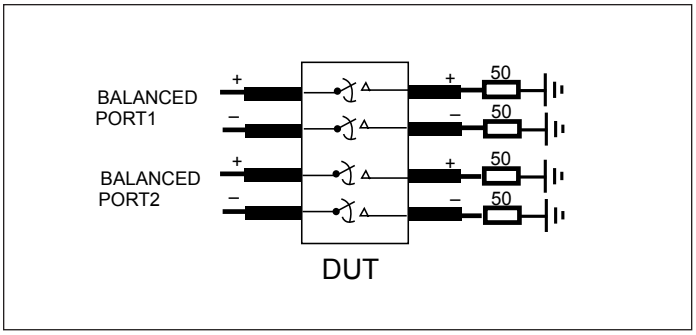


Figure 1. Crosstalk Setup

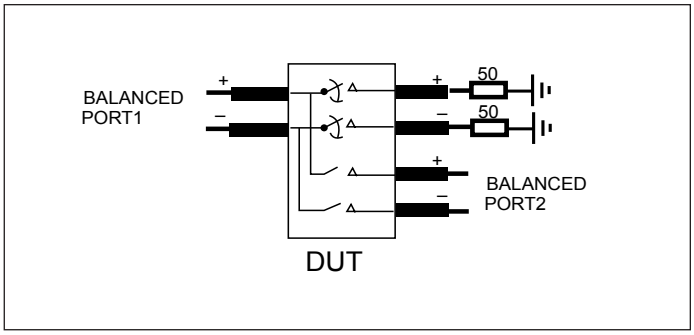


Figure 2. Off-Isolation Setup

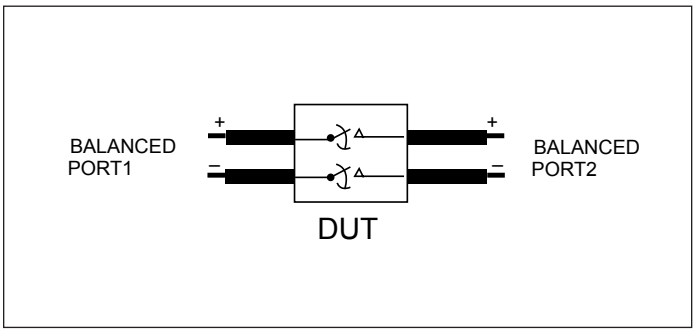
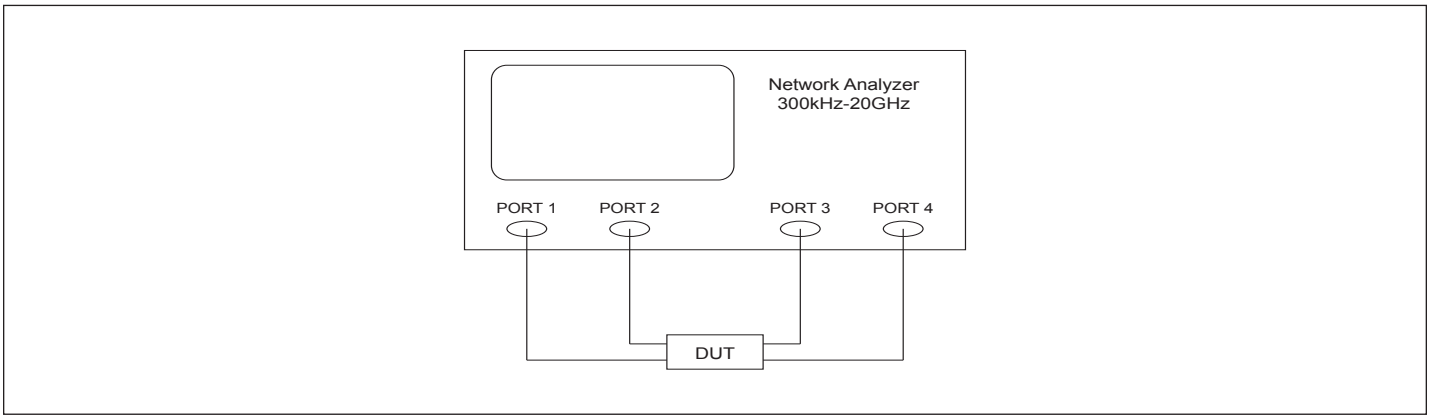
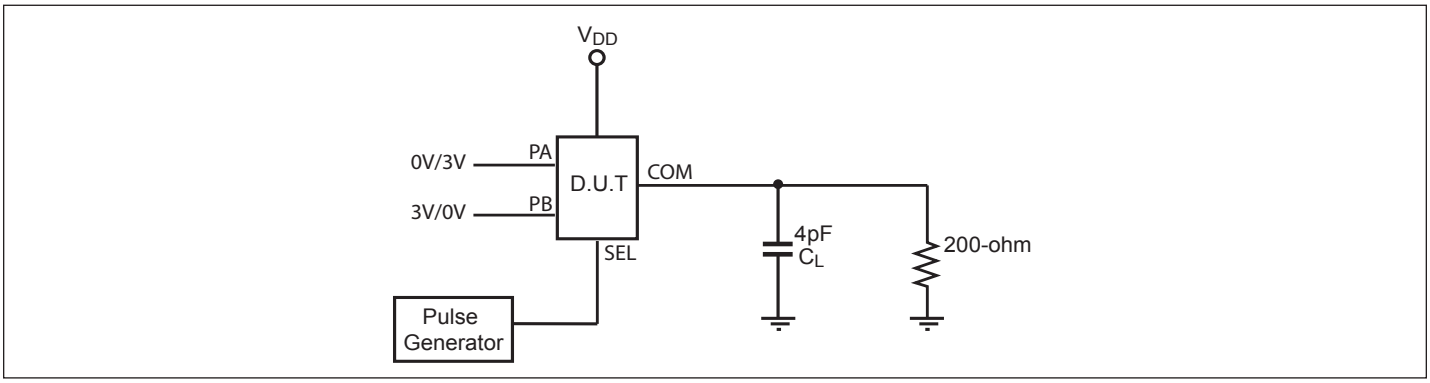


Figure 3. Differential Insertion Loss

Test Circuit for Dynamic Electrical Characteristics



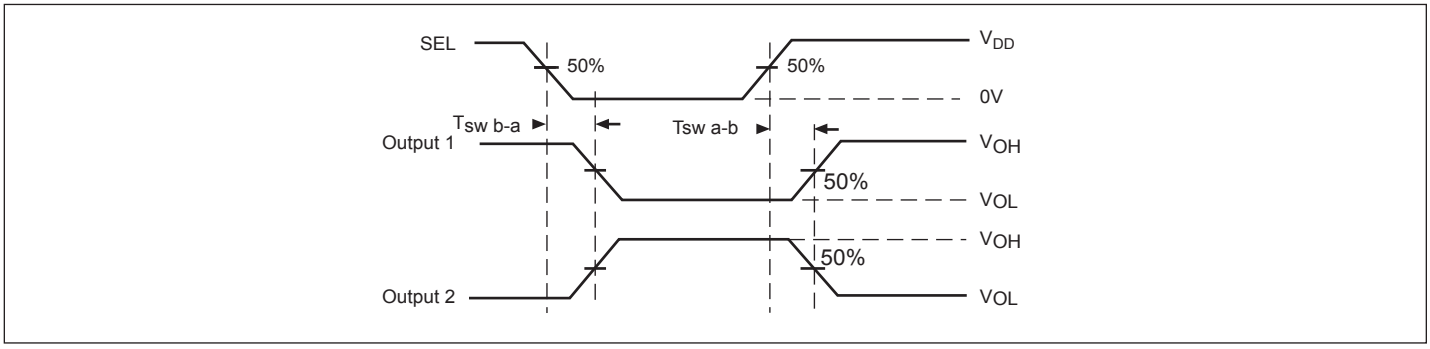
Test Circuit for Electrical Characteristics(1-4)



Notes:

1. C_L = Load capacitance: includes jig and probe capacitance.
2. R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.
3. All input impulses are supplied by generators having the following characteristics: PRR ≤ MHz, Z_O = 50Ω, t_R ≤ 2.5ns, t_F ≤ 2.5ns.
4. The outputs are measured one at a time with one transition per measurement.

Switching Waveforms



Voltage Waveforms for Select Timing

Test Condition

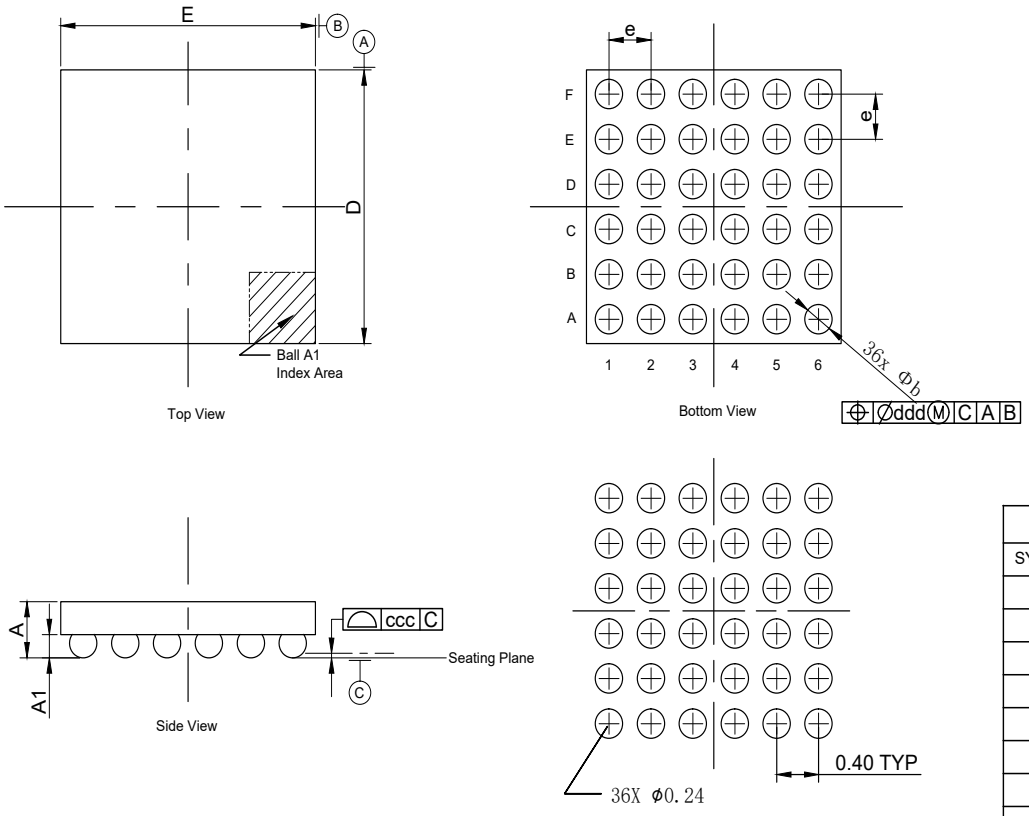
Output 1 Test Condition	Output 2 Test Condition
PA = Low	PA = High
PB = High	PB = Low

Part Marking

Z: Die Rev
YY: Year
WW: Workweek
1st X: Assembly Site Code
2nd X: Fab Site Code

Packaging Mechanical

36-UWLB (GE)



PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.46	0.54
A1	0.19	0.23
D	2.41	2.47
e	0.40 BSC	
E	2.41	2.47
b	0.24	0.28
ccc	0.05 TYP	
ddd	0.015 TYP	

Notes:
1. NO JEDEC SPEC APPLIES

DIODES INCORPORATED / PERICOM ENABLING SERIAL CONNECTIVITY	**DATE: 11/05/21**
DESCRIPTION: U-WLB2424-36, Wafer Level	
PACKAGE CODE: GE (GE36)	
DOCUMENT CONTROL#: PD-2224	**REVISION: A**

21-1505

For latest package information:

See http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/.

Ordering Information

Ordering Code	Package Code	Package Description
PI3WVR646GEEX	GE	U-WLB2424-36, Wafer Level

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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