Obsolete – Part Discontinued

PI4IOE5V9520

Remote 2-bit I²C-bus low power I/O port with interrupt and reset

Features

- Operation power supply voltage from 2.3V to 5.5V
- 2-bit I²C-bus GPIO with interrupt and reset
- 5V tolerant I/Os
- Active Low interrupt output
- Active Low reset input
- Low current consumption
- 0Hz to 1MHz clock frequency
- Noise filter on SCL/SDA inputs
- Power-on reset, software reset
- ESD protection (4KV HBM and 1KV CDM)
- Package offered: UQFN 1.6x1.6-8

Description

The PI4IOE5V9520 provides 2 bits of General Purpose parallel Input/Output (GPIO) expansion for I²C-bus applications. It includes the features such as higher driving capability, 5V tolerance, lower power supply, individual I/O configuration, and smaller packaging. It provides a simple solution when additional I/O is needed for ACPI power switches, sensors, push buttons, LEDs, fans, etc.

The PI4IOE5V9520 consists of a 2-bit quasi-bidirectional port and an I²C-bus interface.

The PI4IOE5V9520 open-drain interrupt output ($\overline{INT}$) is activated by any updated of the port inputs and is used to indicate the system master that the port inputs has changed.

The power-on reset sets the registers to their default values and initializes the device state machine. The Reset pin ($\overline{Reset}$) causes the same reset/initialization to occur without de-powering the device.

Pin Configuration

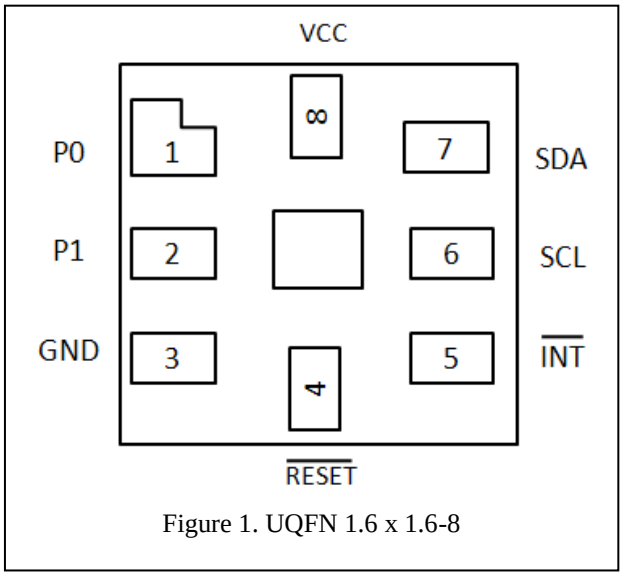


Figure 1. UQFN 1.6 x 1.6-8

Pin Description

Table 1. Pin description

Pin	Name	Type	Description
1	P0	I/O	Input/Output 0
2	P1	I/O	Input/Output1
3	GND	G	Supply ground
4	$\overline{\text{RESET}}$	I	Reset pin
5	$\overline{\text{INT}}$	O	Interrupt output (open-drain)
6	SCL	I	Serial clock line
7	SDA	I/O	Serial data line
8	VCC	P	Power supply

* I = Input; O = Output; P = Power; G = Ground

Maximum Ratings

Power supply.....-0.5V to +6.0V
Voltage on an I/O pin.....GND-0.5V to +6.0V
Input current.....±20mA
Output current on an I/O pin.....±50mA
Supply current.....40mA
Ground supply current.....50mA
Total power dissipation.....200mW
Operation temperature.....-40~85℃
Storage temperature.....-65~150℃
Maximum Junction temperature ,T j(max).....125℃

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Static characteristics

VCC = 2.3 V to 5.5 V; GND = 0 V; Tamb = -40 ℃ to +85 ℃; unless otherwise specified.

Table 2: Static characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power supply						
VCC	Supply voltage		2.3	-	5.5	V
I_{CC}	Supply current	Operating mode; VCC = 5.5 V; no load; f_{SCL}= 100 kHz	-	104	175	μA
I_{stb}	Standby current	Standby mode; VCC = 5.5 V; no load; V_I = VCC; f_{SCL}= 0 kHz; I/O = inputs		0.25	1	μA
V_{POR}	Power-on reset voltage[1]		-	1.16	1.41	V
Input SCL, input/output SDA						
V_{IL}	Low level input voltage		-0.5	-	+0.3VCC	V
V_{IH}	High level input voltage		0.7VCC	-	5.5	V
I_{OL}	Low level output current	V_{OL} = 0.4V	20	-	-	mA
I_L	Leakage current	V_I = VCC = GND	-1	-	1	μA
C_i	Input capacitance	V_I = GND	-	5	10	pF

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I/Os						
V_{IL}	Low level input voltage		-0.5	-	+0.81	V
V_{IH}	High level input voltage		+1.8	-	5.5	V
I_{OL}	Low level output voltage current	VCC = 2.3 V; V_{OL} = 0.5 V[2]	12	28	-	mA
		VCC = 3.0V; V_{OL} = 0.5 V[2]	17	35	-	mA
		VCC = 4.5 V; V_{OL} = 0.5 V[2]	25	42	-	mA
I_{OL}(tot)	Total LOW-level output current	V_{OL} = 0.5V; VCC = 4.5V			50	mA
I_{OH}	HIGH-level output current	V_{OH} = GND	-30	-359	-480	uA
Itrt(pu)	Transient boosted pull-up current	V_{OH} = GND	-0.5	-1.0		mA
C_i	Off-state Input capacitance		-	9	10	pF
C_o	Off-state Output capacitance		-	9	10	pF
Interrupt $\overline{\text{INT}}$						
I_{OL}	Low level input voltage	V_{OL} = 0.4V	3	13	-	mA
I_{OH}	High level input voltage	V_{OL} = 0.4V	-1		+1	uA
Reset $\overline{\text{RESET}}$						
V_{IL}	Low level input voltage		-0.5	-	+0.81	V
V_{IH}	High level input voltage		+1.8	-	5.5	V
I_L	Input leakage current	V_I = VCC = GND	-1		1	µA

Note:
[1]: VCC must be lowered to 0.2 V for at least 5 us in order to reset part.
[2]: Each I/O must be externally limited to a maximum of 25 mA and the total package must be limited to a maximum current of 50 mA.

Dynamic characteristics

Table 3: Dynamic characteristics

Symbol	Parameter	Conditions	Standard mode I²C		Fast mode I²C		Fast mode Plus I²C		Unit
			Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	0	1000	kHz
t_{BUF}	Bus free time between a STOP and START condition		4.7	-	1.3	-	0.5	-	µs
$t_{HD;STA}$	Hold time (repeated) START condition		4.0	-	0.6	-	0.26	-	µs
$t_{SU;STA}$	Set-up time for a repeated START condition		4.7	-	0.6	-	0.26	-	µs
$t_{SU;STO}$	Set-up time for STOP condition		4.0	-	0.6	-	0.26	-	µs
$t_{VD;ACK}$[1]	Data valid acknowledge time		-	3.45	-	0.9	-	0.45	µs
$t_{HD;DAT}$[2]	Data hold time		0	-	0	-	0	-	ns
$t_{VD;DAT}$	Data valid time		-	3.45	-	0.9	-	0.45	us
$t_{SU;DAT}$	Data set-up time		250	-	100	-	50	-	ns
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	0.26	-	µs
t_f	Fall time of both SDA and SCL signals		-	300	-	300	-	120	ns
t_r	Rise time of both SDA and SCL signals		-	1000	-	300	-	120	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter		-	50	-	50		50	ns
Port timing									
$t_{v(Q)}$	Data output valid time[3]		-	200	-	200	-	200	ns
$t_{su(D)}$	Data input set-up time		100	-	100	-	100	-	ns
$t_{h(D)}$	Data input hold time		1	-	1	-	1	-	µs
Interrupt timing									
$t_{v(INT)}$	Valid time on pin $\overline{INT}$		-	4	-	4	-	4	µs
$t_{rst(INT)}$	Reset time on pin $\overline{INT}$		-	4	-	4	-	4	µs

Symbol	Parameter	Conditions	Standard mode I²C		Fast mode I²C		Fast mode Plus I²C		Unit
			Min	Max	Min	Max	Min	Max	
Reset timing									
$t_{w(rst)}$	Reset pulse width		25	-	25	-	25	-	ns
$t_{rec(rst)}$	Reset recovery time[4]		0	-	0	-	0	-	ns
t_{rst}	Reset time		1	-	1	-	1	-	us

Note:
[1]: $t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA (out) LOW.
[2]: $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.
[3]: $t_{v(Q)}$measured from 0.7VCC on SCL to 50% I/O output.
[4]: To reset the device while actively communicating on the bus may cause glitches or errant STOP conditions. Upon reset, the full delay will be the sum of t_{rst} and RC time constant of SDA bus.

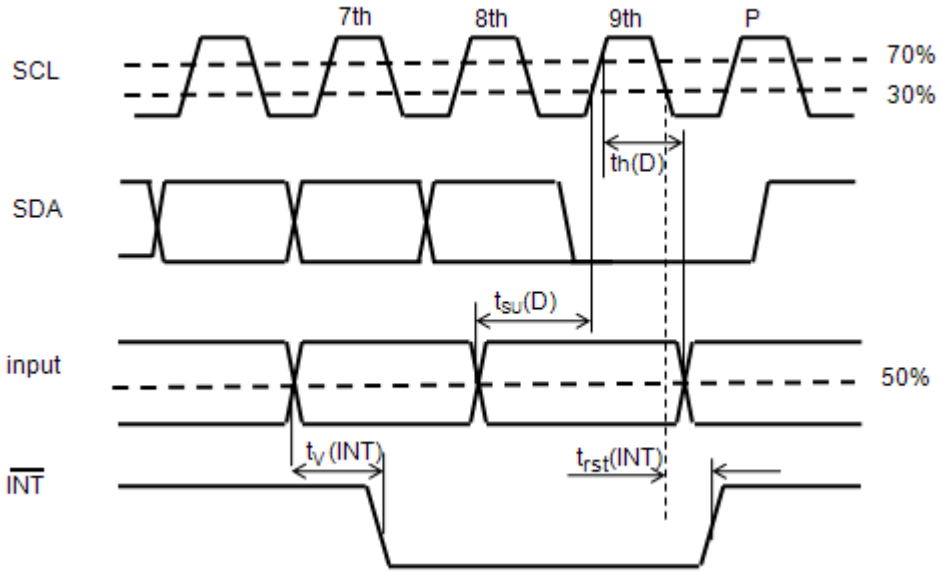
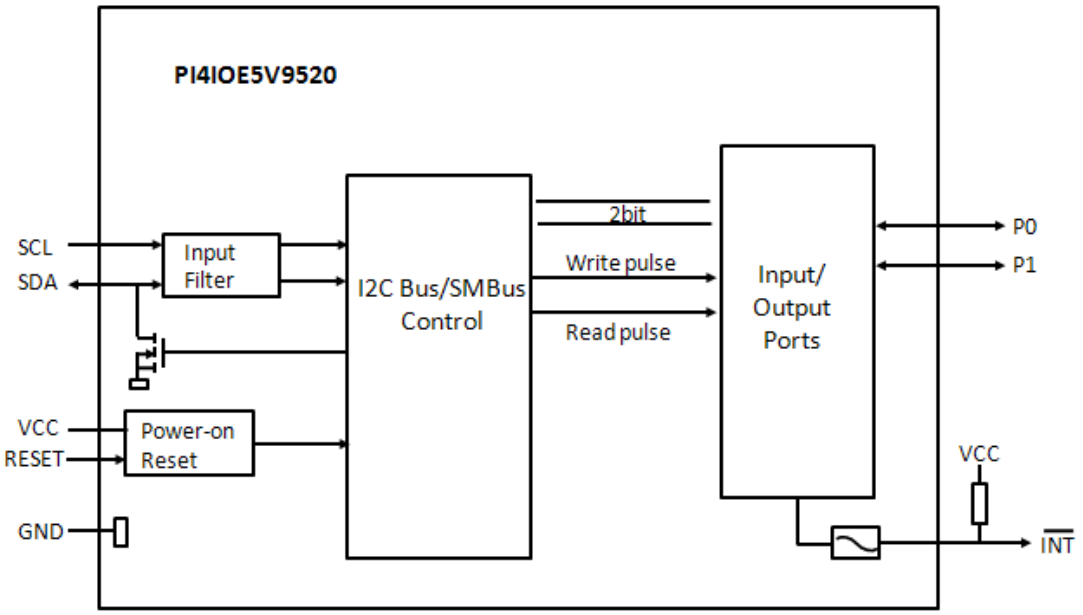


Figure 2: Timing diagram for INT timing and Port timing

PI4IOE5V9520 Block Diagram

Figure 3: Block diagram of PI4IOE5V9520



Note: All I/Os are set to inputs at reset.

Details Description

a. Device address

Table 4: Device address

	b7(MSB)	b6	b5	b4	b3	b2	b1	b0
Address Byte	0	1	0	0	1	0	0	R/W

Note: Read "1", Write "0"

b. Software Reset Call

General Call address: allows resetting the device through the I²C-bus upon reception of the right I²C-bus sequence.

	b7(MSB)	b6	b5	b4	b3	b2	b1	b0
General Call Address	0	0	0	0	0	0	0	0

c. Software Reset

The Software Reset Call allows all the devices in the I²C-bus to be reset to the power-up state value through a specific formatted I²C-bus command. To be performed correctly, it implies that the I²C-bus is functional and that there is no device hanging the bus.
The Software Reset sequence is defined as following:

1. A START command is sent by the I²C-bus master.
2. The reserved General Call I²C-bus address '0000 000' with the R/W bit set to 0 (write) is sent by the I²C-bus master.
3. The device acknowledges after seeing the General Call address '0000 0000' (00h) only. If the R/W bit is set to 1 (read), no acknowledge is returned to the I²C-bus master.
4. Once the General Call address has been sent and acknowledged, the master sends 1 byte. The value of the byte must be equal to 06h.
   a. The device acknowledges this value only. If the byte is not equal to 06h, the device does not acknowledge it.
   b. If more than 1 byte of data is sent, the device does not acknowledge any more.
5. Once the right byte has been sent and correctly acknowledged, the master sends a STOP command to end the Software Reset sequence: the device then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time. If the master sends a Repeated START instead, no reset is performed.

The I²C-bus master must interpret a non-acknowledge from the device (at any time) as a 'Software Reset Abort'. The device does not initiate a reset of its registers.
The unique sequence that initiates a Software Reset is described in Figure 4.

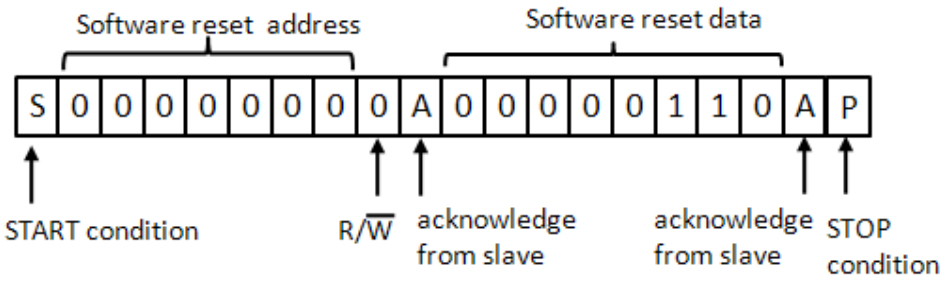


Figure 4: Software reset

d. Quasi-bidirectional I/O architecture

The device ports are entirely independent and are output ports. The state of the ports at the pin is transferred from the ports to the microcontroller in the Read mode (see Figure 7). Output data is transmitted to the ports in the Write mode (see Figure 6).At power-on all ports are HIGH. A bit set to 1 in the data byte drives the line HIGH at the corresponding port. A bit set to 0 in the data byte drives the line LOW at the corresponding port.
If an external voltage is applied to an output, care should be exercised because of the low-impedance path that exists between the pin and either VCC or GND.

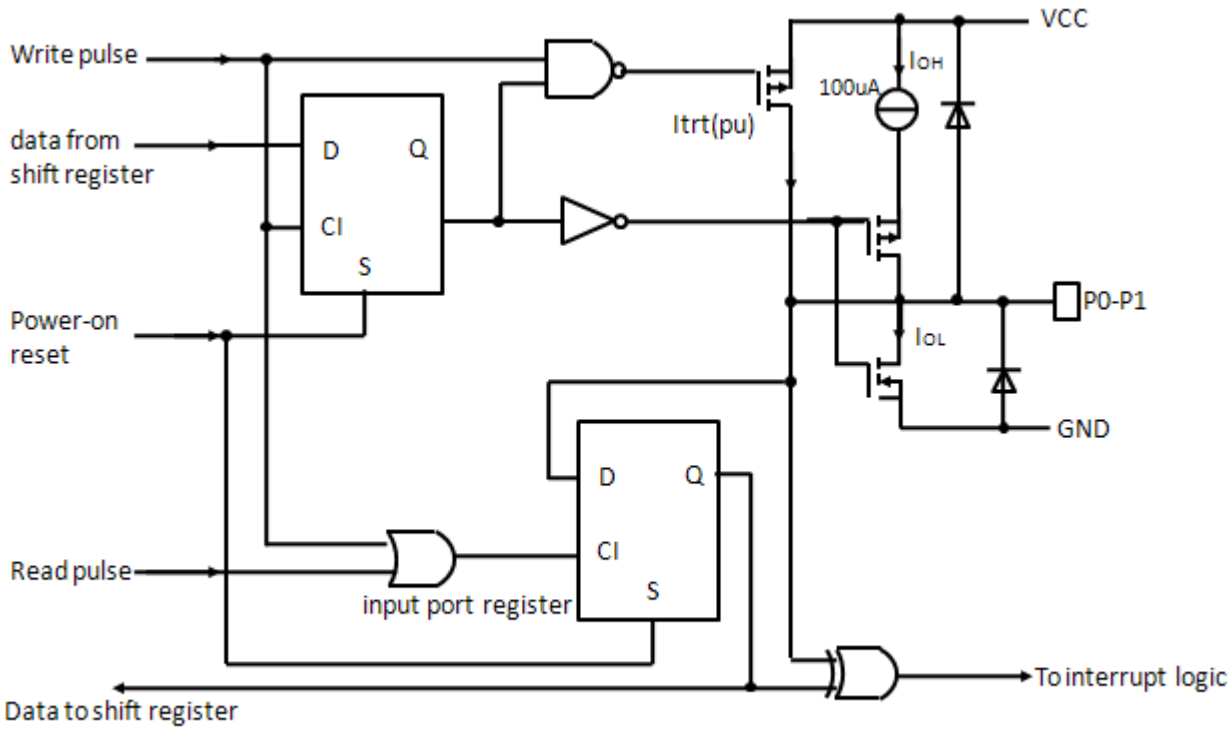


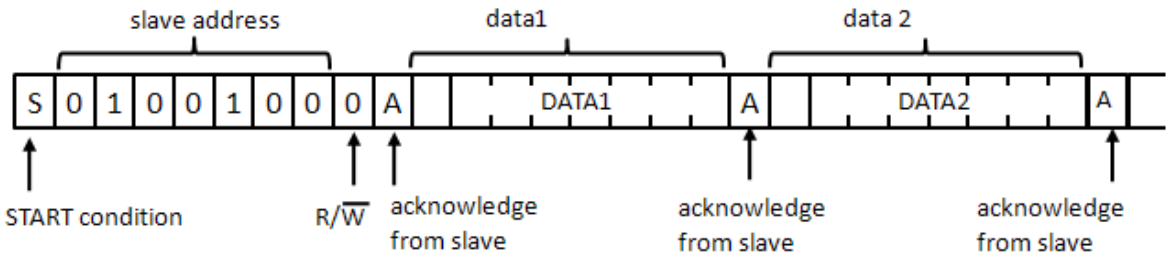
Figure 5:I/O architecture

e. Bus Transaction

Writing to the port (output mode)

To write, the master (microcontroller) first addresses the slave device. By setting the last bit of the byte containing the slave address to logic 0, the Write mode is entered. The device acknowledges and the master sends the data byte for P7 to P0 and is acknowledged by the device. Writes to P7 to P2 are ignored in the PI4IOE5V9520 as only P1 through P0 are available. The 2-bit data is presented on the port lines after it has been acknowledged by the device. The number of data bytes that can be sent successively is not limited. The previous data is overwritten every time a data byte has been sent.

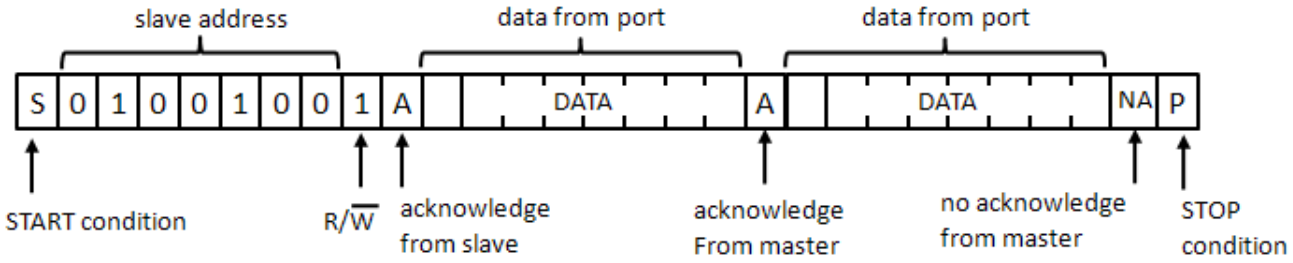
Figure 6: Write to the register



Reading from a port (input mode)

All ports are outputs and cannot be used as inputs. When reading the device, the data returned is the port state at the pin. To read, the master (microcontroller) first addresses the slave device by setting the last bit of the byte containing the slave address to logic 1. The data byte that follows on the SDA is the value of the ports pins. There is no limit to the number of bytes read, and the state of the output port pins is updated at each acknowledge cycle. Logic 1 means that the port is HIGH. Logic 0 means that the port is LOW. When the PI4IOE5V9520 is read, P7 through P2 return logic '1'.

Figure 7: Read from the register



Note: Transfer can be stopped at any time by a STOP condition.

f. Power-on reset

When power is applied to VCC, an internal Power-On Reset (POR) holds the device in a reset condition until VCC has reached VPOR. At that point, the reset condition is released and the device registers and I²C-bus state machine initialize to their default states.

g. Interrupt output ($\overline{INT}$)

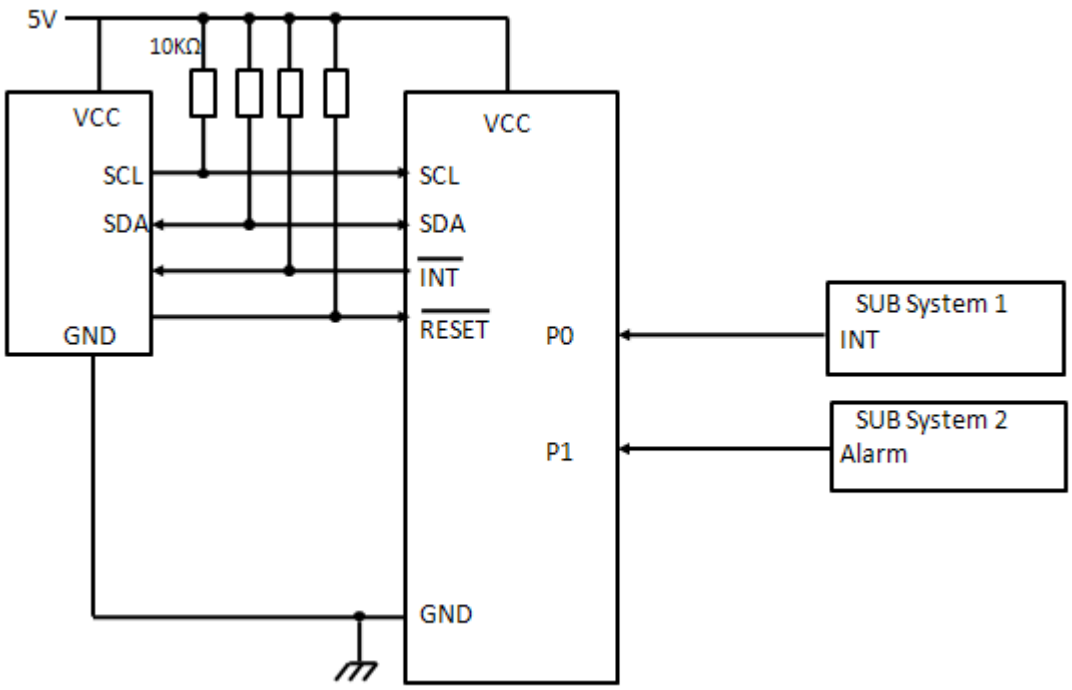
The open-drain interrupt output ($\overline{INT}$) is activated when one of the port pins changes state and the pin is configured as an input. The interrupt is de-activated when the input returns to its previous state or data is read from the device.

h. $\overline{\text{RESET}}$ input

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin LOW for a minimum of $t_{w(rst)}$. The PI4IOE5V9520 registers and I²C-bus state machine will be held in their default state until the $\overline{\text{RESET}}$ input is once again HIGH.

Application design-in information

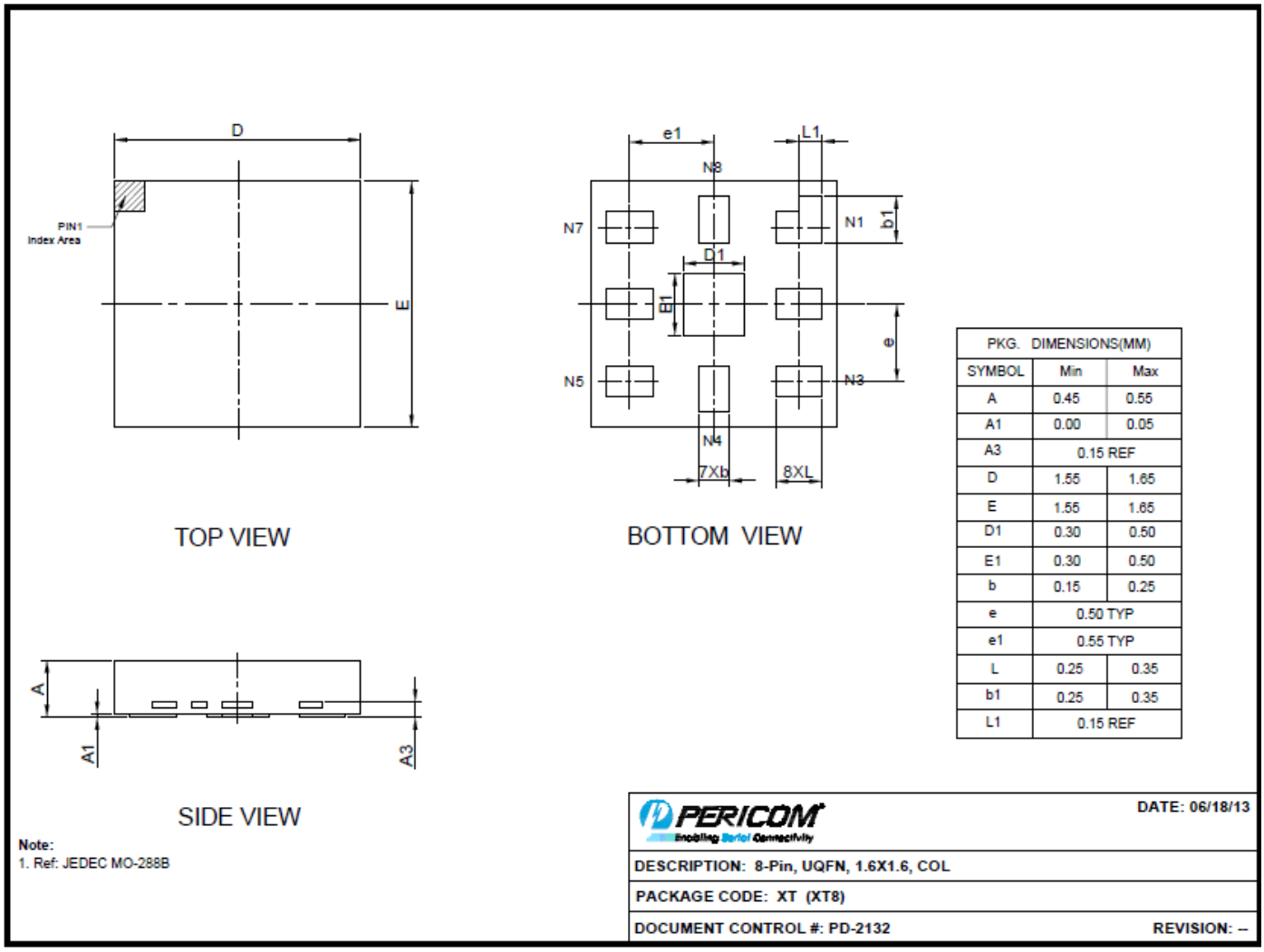
Figure 8: Typical application



Mechanical Information

UQFN-8 (XT)

Figure 9. Package outline UQFN-8 (XT)



PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.45	0.55
A1	0.00	0.05
A3	0.15 REF	
D	1.55	1.65
E	1.55	1.65
D1	0.30	0.50
E1	0.30	0.50
b	0.15	0.25
e	0.50 TYP	
e1	0.55 TYP	
L	0.25	0.35
b1	0.25	0.35
L1	0.15 REF	

Ordering Information

Part No.	Package Code	Package
PI4IOE5V9520XTEX	XT	8-pin UQFN 1.6x1.6, Tape & Reel

Note:
- E = Pb-free and Green
- Adding X Suffix= Tape/Reel