

**Remote 16-bit I/O expander for Fm+ I<sup>2</sup>C-bus with interrupt**
**Features**

- Operation power supply voltage from 2.3V to 5.5V
- 16-bit remote I/O pins that default to inputs at power-up
- 1 MHz I<sup>2</sup>C-bus interface
- Compliant with the I<sup>2</sup>C-bus Fast and Standard modes
- 5.5V tolerant I/Os
- SDA with 30 mA sink capability for 4000 pF buses
- Latched outputs with 25 mA sink capability for directly driving LEDs
- Total package sink capability of 400 mA
- Active LOW open-drain interrupt output
- Low standby current
- 64 programmable slave addresses using 3 address pins
- ESD protection (4KV HBM and 1KV CDM)
- Latch-up tested (exceeds 100mA)
- Offered in two different packages: TSSOP-24 and TQFN 4x4-24

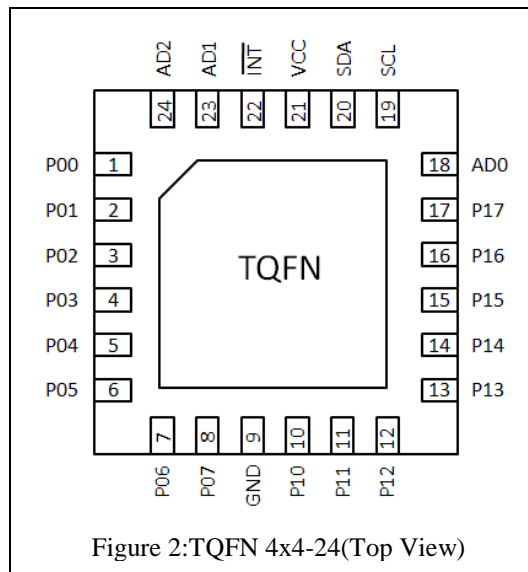
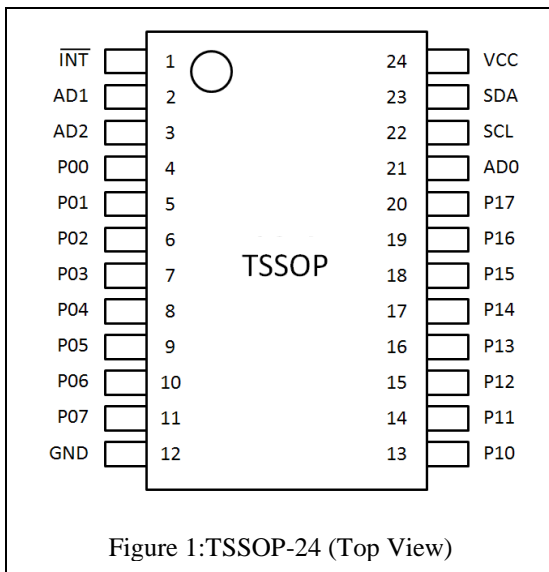
**Description**

The PI4IOE5V9675 provides general purpose remote I/O expansion for most microcontroller families via the two-line bidirectional bus (I<sup>2</sup>C-bus) and is a part of the Fast-mode Plus family.

The PI4IOE5V9675 provides higher Fast-mode Plus (Fm+) I<sup>2</sup>C-bus speeds (1 MHz versus 400 kHz) so that the output can support PWM dimming of LEDs, high I<sup>2</sup>C-bus drive (30 mA) so that many more devices can be on the bus without the need for bus buffers, high total package sink capacity (400 mA) that supports having all 25 mA LEDs on at the same time and more device addresses (64) are available to allow many more devices on the bus without address conflicts.

The device consists of a 16-bit quasi-bidirectional port and an I<sup>2</sup>C-bus interface. The PI4IOE5V9675 has a low current consumption and includes latched outputs with high current drive capability for directly driving LEDs.

It also possesses an interrupt line ( $\overline{\text{INT}}$ ) which can be connected to the interrupt logic of the microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I<sup>2</sup>C-bus. The internal Power-On Reset (POR) or software reset sequence initializes the I/Os as inputs.

**Pin Configuration**




## Pin Description

Table 1: Pin Description

| Pin     |        | Name                    | Type | Description                  |
|---------|--------|-------------------------|------|------------------------------|
| TSSOP24 | TQFN24 |                         |      |                              |
| 1       | 22     | $\overline{\text{INT}}$ | O    | Interrupt input (open-drain) |
| 2       | 23     | AD1                     | I    | Address input 1              |
| 3       | 24     | AD2                     | I    | Address input 2              |
| 4       | 1      | P00                     | I/O  | Port 0 input/output 0        |
| 5       | 2      | P01                     | I/O  | Port 0 input/output 1        |
| 6       | 3      | P02                     | I/O  | Port 0 input/output 2        |
| 7       | 4      | P03                     | I/O  | Port 0 input/output 3        |
| 8       | 5      | P04                     | I/O  | Port 0 input/output 4        |
| 9       | 6      | P05                     | I/O  | Port 0 input/output 5        |
| 10      | 7      | P06                     | I/O  | Port 0 input/output 6        |
| 11      | 8      | P07                     | I/O  | Port 0 input/output 7        |
| 12      | 9      | GND                     | G    | Ground                       |
| 13      | 10     | P10                     | I/O  | Port 1 input/output 0        |
| 14      | 11     | P11                     | I/O  | Port 1 input/output 1        |
| 15      | 12     | P12                     | I/O  | Port 1 input/output 2        |
| 16      | 13     | P13                     | I/O  | Port 1 input/output 3        |
| 17      | 14     | P14                     | I/O  | Port 1 input/output 4        |
| 18      | 15     | P15                     | I/O  | Port 1 input/output 5        |
| 19      | 16     | P16                     | I/O  | Port 1 input/output 6        |
| 20      | 17     | P17                     | I/O  | Port 1 input/output 7        |
| 21      | 18     | AD0                     | I    | Address input 0              |
| 22      | 19     | SCL                     | I    | Serial clock line input      |
| 23      | 20     | SDA                     | I    | Serial data line open-drain  |
| 24      | 21     | VCC                     | P    | Supply voltage               |

\* I = Input; O = Output; P = Power; G = Ground



**Maximum Ratings**

|  |                   |
|--|-------------------|
| Power supply.....  | -0.5V to +6.0V    |
| Voltage on an I/O pin .....                              | GND-0.5V to +6.0V |
| Input current.....                                       | ±20mA             |
| Output current on an I/O pin .....                       | ±50mA             |
| Supply current.....                                      | ±160mA            |
| Ground supply current.....                               | 600mA             |
| Total power dissipation.....                             | 600mW             |
| Operation temperature.....                               | -40~85°C          |
| Storage temperature .....                                | -65~150°C         |
| Maximum Junction temperature ,T <sub>j</sub> (max) ..... | 125°C             |

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Static characteristics**

VCC = 2.3 V to 5.5 V; GND = 0 V; Tamb= -40 °C to +85 °C; unless otherwise specified.

Table 2: Static characteristics

| Symbol                             | Parameter                             | Conditions   | Min.   | Typ. | Max.    | Unit |
|------------------------------------|---------------------------------------|--|--------|------|---------|------|
| <b>Power supply</b>                |                                       |  |        |      |         |      |
| VCC                                | Supply voltage                        |  | 2.3    | -    | 5.5     | V    |
| I <sub>CC</sub>                    | Supply current                        | Operating mode; VCC= 5.5 V; no load; f <sub>SCL</sub> = 1MHz                                     | -      | 250  | 500     | μA   |
| I <sub>sb</sub>                    | Standby current                       | Standby mode; VCC= 5.5 V; no load; V <sub>I</sub> = VCC;; f <sub>SCL</sub> = 0 kHz; I/O = inputs | -      | 2.5  | 10      | uA   |
| V <sub>POR</sub>                   | Power-on reset voltage <sup>[1]</sup> |  | -      | 1.16 | 1.41    | V    |
| <b>Input SCL, input/output SDA</b> |                                       |  |        |      |         |      |
| V <sub>IL</sub>                    | Low level input voltage               |  | -0.5   | -    | +0.3VCC | V    |
| V <sub>IH</sub>                    | High level input voltage              |  | 0.7VCC | -    | 5.5     | V    |
| I <sub>OL</sub>                    | Low level output current              | V <sub>OL</sub> =0.4V  | 20     | -    | -       | mA   |
| I <sub>L</sub>                     | Leakage current                       | V <sub>I</sub> =VCC=GND  | -1     | -    | 1       | μA   |
| C <sub>i</sub>                     | Input capacitance                     | V <sub>I</sub> =GND  | -      | 5    | 10      | pF   |



**PI4IOE5V9675**  
**Preliminary Datasheet**  
**16-bit I<sup>2</sup>C-bus and SMBus I/O port with interrupt**

| Symbol  | Parameter                         | Conditions  | Min.   | Typ. | Max.    | Unit |
|---|-----------------------------------|---|--------|------|---------|------|
| <b>I/Os</b>   |                                   |   |        |      |         |      |
| I <sub>OL</sub>                                     | Low level output current          | VCC = 2.3 V; V <sub>OL</sub> = 0.5 V <sup>[2]</sup> | 12     | 28   |         | mA   |
|   |                                   | VCC=3.0V; V <sub>OL</sub> = 0.5 V <sup>[2]</sup>    | 17     | 35   |         | mA   |
|   |                                   | VCC=4.5V; V <sub>OL</sub> = 0.5 V <sup>[2]</sup>    | 25     | 42   |         | mA   |
| I <sub>OL(tot)</sub>                                | total LOW-level output current    | V <sub>OL</sub> =0.5V;VCC=4.5V                      |        |      | 400     | mA   |
| I <sub>OH</sub>                                     | HIGH-level output current         | V <sub>OH</sub> = GND                               | -30    | -359 | -480    | uA   |
| I <sub>trt(pu)</sub>                                | transient boosted pull-up current | V <sub>OH</sub> = GND                               | -0.5   | -1.0 |         | mA   |
| C <sub>i</sub>                                      | Off-state Input capacitance       | <sup>[3]</sup>                                      | -      | 9    | 10      | pF   |
| C <sub>o</sub>                                      | Off-state Output capacitance      | <sup>[3]</sup>                                      | -      | 9    | 10      | pF   |
| <b>Interrupt <math>\overline{\text{INT}}</math></b> |                                   |   |        |      |         |      |
| I <sub>OL</sub>                                     | Low level output current          | V <sub>OL</sub> =0.4V                               | 6      | -    | -       | mA   |
| C <sub>o</sub>                                      | Output capacitance                |   |        | 2.1  | 10      | pF   |
| <b>Select inputs AD0,AD1,AD2</b>                    |                                   |   |        |      |         |      |
| V <sub>IL</sub>                                     | Low level input voltage           |   | -0.5   | -    | +0.3VCC | V    |
| V <sub>IH</sub>                                     | High level input voltage          |   | 0.7VCC | -    | 5.5     | V    |
| I <sub>L</sub>                                      | Input leakage current             |   | -1     |      | 1       | μA   |
| C <sub>i</sub>                                      | input capacitance                 |   |        | 2.4  | 10      | pF   |

Note:

[1]:VCC must be lowered to 0.2 V for at least 20us in order to reset part.

[2]:Each I/O must be externally limited to a maximum of 25 mA and the total package limited to 400 mA due to internal busing limits.

[3]: The value is not tested, but verified on sampling basis.

## Dynamic Characteristics

Table 3: Dynamic characteristics

| Symbol                                      | Parameter   | Standard mode I <sup>2</sup> C |      | Fast mode I <sup>2</sup> C |     | Fast mode Plus I <sup>2</sup> C |      | Unit |
|---|---|--------------------------------|------|----------------------------|-----|---------------------------------|------|------|
|   |   | Min                            | Max  | Min                        | Max | Min                             | Max  |      |
| f <sub>SCL</sub>                            | SCL clock frequency   | 0                              | 100  | 0                          | 400 | 0                               | 1000 | kHz  |
| t <sub>BUF</sub>                            | bus free time between a STOP and START condition                  | 4.7                            | -    | 1.3                        | -   | 0.5                             |      | μs   |
| t <sub>HD;STA</sub>                         | hold time (repeated) START condition                              | 4.0                            | -    | 0.6                        | -   | 0.26                            |      | μs   |
| t <sub>SU;STA</sub>                         | set-up time for a repeated START condition                        | 4.7                            | -    | 0.6                        | -   | 0.26                            |      | μs   |
| t <sub>SU;STO</sub>                         | set-up time for STOP condition                                    | 4.0                            | -    | 0.6                        | -   | 0.26                            |      | μs   |
| t <sub>VD;ACK</sub> <sup>[1]</sup>          | data valid acknowledge time                                       | -                              | 3.45 | -                          | 0.9 | -                               | 0.45 | μs   |
| t <sub>HD;DAT</sub> <sup>[2]</sup>          | data hold time  | 0                              | -    | 0                          | -   | 0                               |      | ns   |
| t <sub>VD;DAT</sub>                         | data valid time   | -                              | 3.45 | -                          | 0.9 | -                               | 0.45 | ns   |
| t <sub>SU;DAT</sub>                         | data set-up time  | 250                            | -    | 100                        | -   | 50                              |      | ns   |
| t <sub>LOW</sub>                            | LOW period of the SCL clock                                       | 4.7                            | -    | 1.3                        | -   | 0.5                             |      | μs   |
| t <sub>HIGH</sub>                           | HIGH period of the SCL clock                                      | 4.0                            | -    | 0.6                        | -   | 0.26                            |      | μs   |
| t <sub>f</sub>                              | fall time of both SDA and SCL signals                             | -                              | 300  |                            | 300 |                                 | 120  | ns   |
| t <sub>r</sub>                              | rise time of both SDA and SCL signals                             | -                              | 1000 |                            | 300 |                                 | 120  | ns   |
| t <sub>SP</sub>                             | pulse width of spikes that must be suppressed by the input filter | -                              | 50   | -                          | 50  |                                 | 50   | ns   |
| <b>Port timing C<sub>L</sub>≤100pF</b>      |   |                                |      |                            |     |                                 |      |      |
| t <sub>v(Q)</sub>                           | Data output valid time <sup>[3]</sup>                             |                                | 4    |                            | 4   |                                 | 4    | ns   |
| t <sub>su(D)</sub>                          | Data input set-up time  | 0                              |      | 0                          |     | 0                               |      | ns   |
| t <sub>h(D)</sub>                           | Data input hold time  | 4                              |      | 4                          |     | 4                               |      | μs   |
| <b>Interrupt timing C<sub>L</sub>≤100pF</b> |   |                                |      |                            |     |                                 |      |      |
| t <sub>v(INT)</sub>                         | Valid time on pin $\overline{\text{INT}}$                         | -                              | 4    | -                          | 4   |                                 | 4    | μs   |
| t <sub>rst(INT)</sub>                       | Reset time on pin $\overline{\text{INT}}$                         | -                              | 4    | -                          | 4   |                                 | 4    | μs   |

**Note:**

[1]: t<sub>VD;ACK</sub> = time for acknowledgement signal from SCL LOW to SDA (out) LOW.

[2]: t<sub>VD;DAT</sub> = minimum time for SDA data out to be valid following SCL LOW.

[3]: t<sub>v(Q)</sub> measured from 0.7VCC on SCL to 50% I/O output.

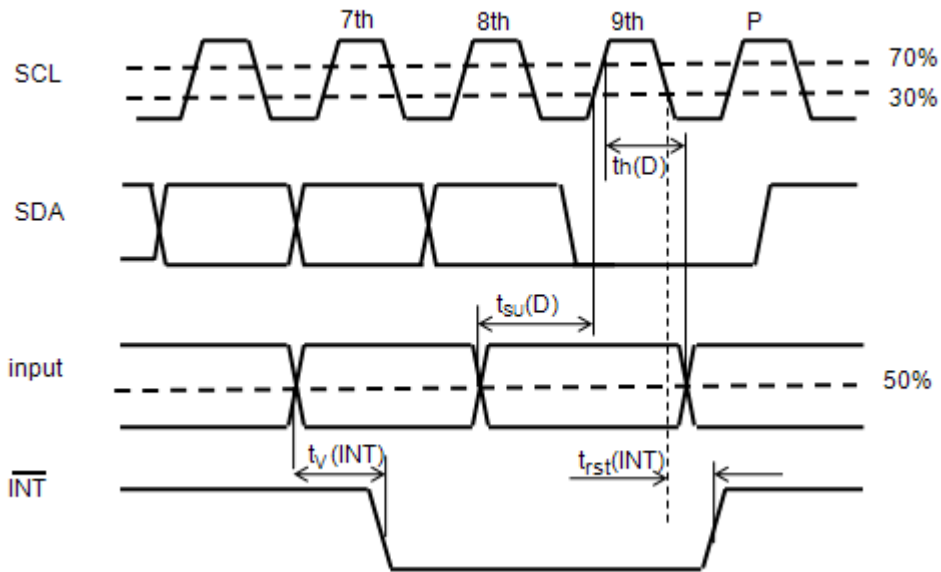
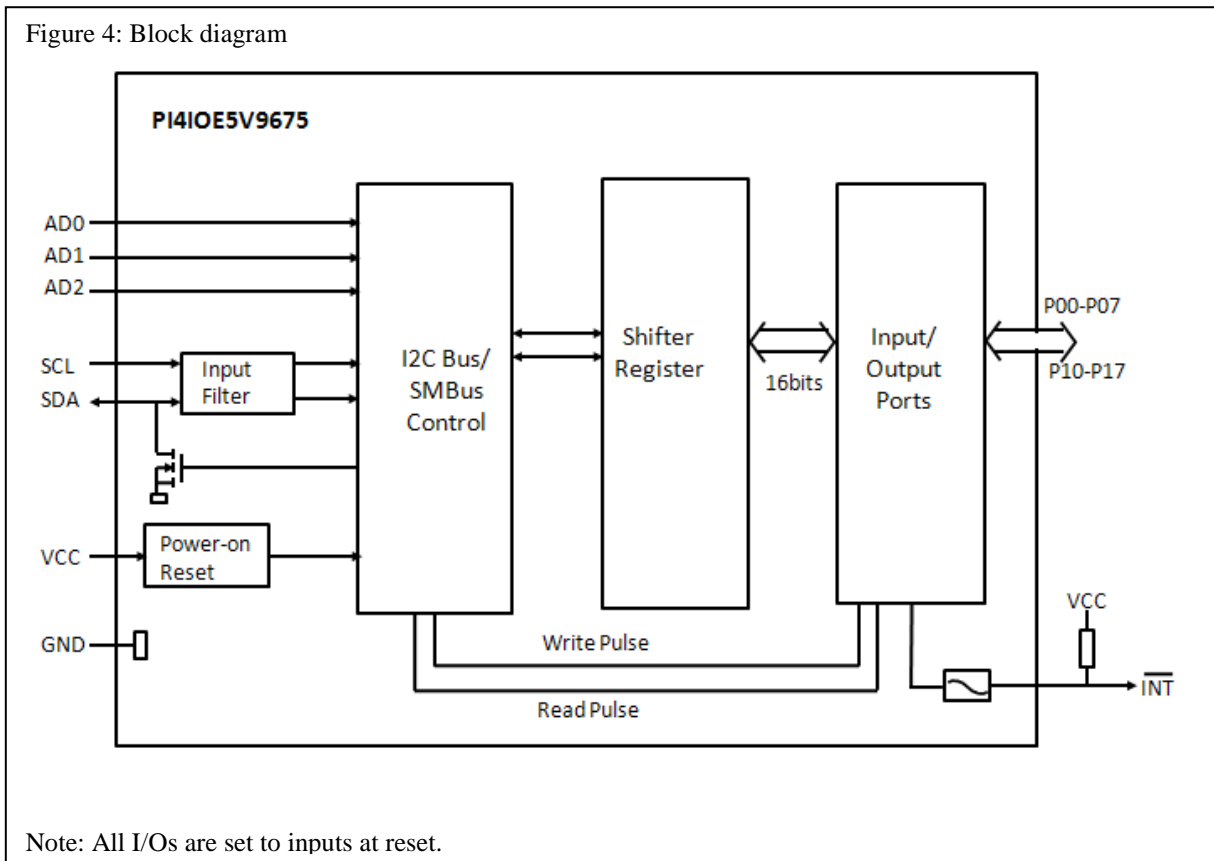


Figure 3: timing parameters for INT signal

**PI4IOE5V9675 Block Diagram**



## Details Description

### a. Device address

Following a START condition, the bus master must send the address of the slave it is accessing and the operation it wants to perform (read or write). The address of the PI4IOE5V9675 is shown in bellow. Slave address pins AD2, AD1, and AD0 choose 1 of 64 slave addresses. To conserve power, no internal pull-up resistors are incorporated on AD2, AD1, and AD0. Address values depending on AD2, AD1, and AD0 can be found in Table “PI4IOE5V9675 address map”.

Remark: The General Call address (0000 0000b) and the Device ID address (1111 100Xb) are reserved and cannot be used as device address. Failure to follow this requirement will cause the PI4IOE5V9675 not to acknowledge.

Remark: Reserved I<sup>2</sup>C-bus addresses must be used with caution since they can interfere with:

- “reserved for future use” I<sup>2</sup>C-bus addresses (0000 011, 1111 101, 1111 110, 1111 111)
- slave devices that use the 10-bit addressing scheme (1111 0xx)
- High speed mode (Hs-mode) master code (0000 1xx)

PI4IOE5V9675 address

|              | b7(MSB) | b6 | b5 | b4 | b3 | b2 | b1 | b0  |
|--------------|---------|----|----|----|----|----|----|-----|
| Address Byte | A6      | A5 | A4 | A3 | A2 | A1 | A0 | R/W |

The last bit of the first byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.



**PI4IOE5V9675**  
**Preliminary Datasheet**  
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**PI4IOE5V9675 Address maps**

| AD2 | AD1 | AD0 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | Address (Write) | Address (Read) |
|-----|-----|-----|----|----|----|----|----|----|----|-----------------|----------------|
| GND | SCL | GND | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 20h             | 21h            |
| GND | SCL | VCC | 0  | 0  | 1  | 0  | 0  | 0  | 1  | 22h             | 23h            |
| GND | SDA | GND | 0  | 0  | 1  | 0  | 0  | 1  | 0  | 24h             | 25h            |
| GND | SDA | VCC | 0  | 0  | 1  | 0  | 0  | 1  | 1  | 26h             | 27h            |
| VCC | SCL | GND | 0  | 0  | 1  | 0  | 1  | 0  | 0  | 28h             | 29h            |
| VCC | SCL | VCC | 0  | 0  | 1  | 0  | 1  | 0  | 1  | 2Ah             | 2Bh            |
| VCC | SDA | GND | 0  | 0  | 1  | 0  | 1  | 1  | 0  | 2Ch             | 2Dh            |
| VCC | SDA | VCC | 0  | 0  | 1  | 0  | 1  | 1  | 1  | 2Eh             | 2Fh            |
| GND | SCL | SCL | 0  | 0  | 1  | 1  | 0  | 0  | 0  | 30h             | 31h            |
| GND | SCL | SDA | 0  | 0  | 1  | 1  | 0  | 0  | 1  | 32h             | 33h            |
| GND | SDA | SCL | 0  | 0  | 1  | 1  | 0  | 1  | 0  | 34h             | 35h            |
| GND | SDA | SDA | 0  | 0  | 1  | 1  | 0  | 1  | 1  | 36h             | 37h            |
| VCC | SCL | SCL | 0  | 0  | 1  | 1  | 1  | 0  | 0  | 38h             | 39h            |
| VCC | SCL | SDA | 0  | 0  | 1  | 1  | 1  | 0  | 1  | 3Ah             | 3Bh            |
| VCC | SDA | SCL | 0  | 0  | 1  | 1  | 1  | 1  | 0  | 3Ch             | 3Dh            |
| VCC | SDA | SDA | 0  | 0  | 1  | 1  | 1  | 1  | 1  | 3Eh             | 3Fh            |
| GND | GND | GND | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 40h             | 41h            |
| GND | GND | VCC | 0  | 1  | 0  | 0  | 0  | 0  | 1  | 42h             | 43h            |
| GND | VCC | GND | 0  | 1  | 0  | 0  | 0  | 1  | 0  | 44h             | 45h            |
| GND | VCC | VCC | 0  | 1  | 0  | 0  | 0  | 1  | 1  | 46h             | 47h            |
| VCC | GND | GND | 0  | 1  | 0  | 0  | 1  | 0  | 0  | 48h             | 49h            |
| VCC | GND | VCC | 0  | 1  | 0  | 0  | 1  | 0  | 1  | 4Ah             | 4Bh            |
| VCC | VCC | GND | 0  | 1  | 0  | 0  | 1  | 1  | 0  | 4Ch             | 4Dh            |
| VCC | VCC | VCC | 0  | 1  | 0  | 0  | 1  | 1  | 1  | 4Eh             | 4Fh            |
| GND | GND | SCL | 0  | 1  | 0  | 1  | 0  | 0  | 0  | 50h             | 51h            |
| GND | GND | SDA | 0  | 1  | 0  | 1  | 0  | 0  | 1  | 52h             | 53h            |
| GND | VCC | SCL | 0  | 1  | 0  | 1  | 0  | 1  | 0  | 54h             | 55h            |
| GND | VCC | SDA | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 56h             | 57h            |
| VCC | GND | SCL | 0  | 1  | 0  | 1  | 1  | 0  | 0  | 58h             | 59h            |
| VCC | GND | SDA | 0  | 1  | 0  | 1  | 1  | 0  | 1  | 5Ah             | 5Bh            |
| VCC | VCC | SCL | 0  | 1  | 0  | 1  | 1  | 1  | 0  | 5Ch             | 5Dh            |
| VCC | VCC | SDA | 0  | 1  | 0  | 1  | 1  | 1  | 1  | 5Eh             | 5Fh            |





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**PI4IOE5V9675 Address maps**

| AD2 | AD1 | AD0 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | Address (Write) | Address (Read) |
|-----|-----|-----|----|----|----|----|----|----|----|-----------------|----------------|
| SCL | SCL | GND | 1  | 0  | 1  | 0  | 0  | 0  | 0  | A0h             | A1h            |
| SCL | SCL | VCC | 1  | 0  | 1  | 0  | 0  | 0  | 1  | A2h             | A3h            |
| SCL | SDA | GND | 1  | 0  | 1  | 0  | 0  | 1  | 0  | A4h             | A5h            |
| SCL | SDA | VCC | 1  | 0  | 1  | 0  | 0  | 1  | 1  | A6h             | A7h            |
| SDA | SCL | GND | 1  | 0  | 1  | 0  | 1  | 0  | 0  | A8h             | A9h            |
| SDA | SCL | VCC | 1  | 0  | 1  | 0  | 1  | 0  | 1  | AAh             | ABh            |
| SDA | SDA | GND | 1  | 0  | 1  | 0  | 1  | 1  | 0  | ACH             | ADh            |
| SDA | SDA | VCC | 1  | 0  | 1  | 0  | 1  | 1  | 1  | A Eh            | A Fh           |
| SCL | SCL | SCL | 1  | 0  | 1  | 1  | 0  | 0  | 0  | B0h             | B1h            |
| SCL | SCL | SDA | 1  | 0  | 1  | 1  | 0  | 0  | 1  | B2h             | B3h            |
| SCL | SDA | SCL | 1  | 0  | 1  | 1  | 0  | 1  | 0  | B4h             | B5h            |
| SCL | SDA | SDA | 1  | 0  | 1  | 1  | 0  | 1  | 1  | B6h             | B7h            |
| SDA | SCL | SCL | 1  | 0  | 1  | 1  | 1  | 0  | 0  | B8h             | B9h            |
| SDA | SCL | SDA | 1  | 0  | 1  | 1  | 1  | 0  | 1  | BAh             | BBh            |
| SDA | SDA | SCL | 1  | 0  | 1  | 1  | 1  | 1  | 0  | BCh             | BDh            |
| SDA | SDA | SDA | 1  | 0  | 1  | 1  | 1  | 1  | 1  | BEh             | BFh            |
| SCL | GND | GND | 1  | 1  | 0  | 0  | 0  | 0  | 0  | C0h             | C1h            |
| SCL | GND | VCC | 1  | 1  | 0  | 0  | 0  | 0  | 1  | C2h             | C3h            |
| SCL | VCC | GND | 1  | 1  | 0  | 0  | 0  | 1  | 0  | C4h             | C5h            |
| SCL | VCC | VCC | 1  | 1  | 0  | 0  | 0  | 1  | 1  | C6h             | C7h            |
| SDA | GND | GND | 1  | 1  | 0  | 0  | 1  | 0  | 0  | C8h             | C9h            |
| SDA | GND | VCC | 1  | 1  | 0  | 0  | 1  | 0  | 1  | CAh             | CBh            |
| SDA | VCC | GND | 1  | 1  | 0  | 0  | 1  | 1  | 0  | CCh             | CDh            |
| SDA | VCC | VCC | 1  | 1  | 0  | 0  | 1  | 1  | 1  | CEh             | CFh            |
| SCL | GND | SCL | 1  | 1  | 1  | 0  | 0  | 0  | 0  | E0h             | E1h            |
| SCL | GND | SDA | 1  | 1  | 1  | 0  | 0  | 0  | 1  | E2h             | E3h            |
| SCL | VCC | SCL | 1  | 1  | 1  | 0  | 0  | 1  | 0  | E4h             | E5h            |
| SCL | VCC | SDA | 1  | 1  | 1  | 0  | 0  | 1  | 1  | E6h             | E7h            |
| SDA | GND | SCL | 1  | 1  | 1  | 0  | 1  | 0  | 0  | E8h             | E9h            |
| SDA | GND | SDA | 1  | 1  | 1  | 0  | 1  | 0  | 1  | E Ah            | E Bh           |
| SDA | VCC | SCL | 1  | 1  | 1  | 0  | 1  | 1  | 0  | E Ch            | E Dh           |
| SDA | VCC | SDA | 1  | 1  | 1  | 0  | 1  | 1  | 1  | E Eh            | E Fh           |

### Software Reset call addresses

- General Call address: allows to reset the PI4IOE5V9675 through the I2C-bus upon reception of the right I2C-bus sequence.

|                      | b7(MSB) | b6 | b5 | b4 | b3 | b2 | b1 | b0  |
|----------------------|---------|----|----|----|----|----|----|-----|
| General Call Address | 0       | 1  | 0  | 0  | 1  | 0  | 0  | R/W |

### Software Reset

The Software Reset Call allows all the devices in the I<sup>2</sup>C-bus to be reset to the power-up state value through a specific formatted I<sup>2</sup>C-bus command. To be performed correctly, it implies that the I<sup>2</sup>C-bus is functional and that there is no device hanging the bus.

The Software Reset sequence is defined as following:

1. A START command is sent by the I<sup>2</sup>C-bus master.
2. The reserved General Call I<sup>2</sup>C-bus address ‘0000 000’ with the R/W bit set to 0 (write) is sent by the I<sup>2</sup>C-bus master.
3. The device acknowledges after seeing the General Call address ‘0000 0000’ (00h) only. If the R/W bit is set to 1 (read), no acknowledge is returned to the I<sup>2</sup>C-bus master.
4. Once the General Call address has been sent and acknowledged, the master sends 1 byte. The value of the byte must be equal to 06h.
  - a. The device acknowledges this value only. If the byte is not equal to 06h, the device does not acknowledge it.
  - b. If more than 1 byte of data is sent, the device does not acknowledge any more.
5. Once the right byte has been sent and correctly acknowledged, the master sends a STOP command to end the Software Reset sequence: the device then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time. If the master sends a Repeated START instead, no reset is performed.

The I<sup>2</sup>C-bus master must interpret a non-acknowledge from the device (at any time) as a ‘Software Reset Abort’. The device does not initiate a reset of its registers.

The unique sequence that initiates a Software Reset is described in Figure 5.

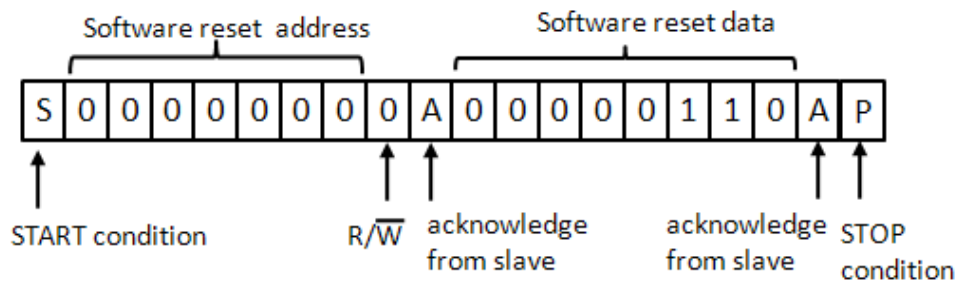


Figure 5 :Software Reset sequence

### Quasi-bidirectional I/O architecture

The PI4IOE5V9675's 16 ports (see Figure 6) are entirely independent and can be used either as input or output ports. Input data is transferred from the ports to the microcontroller in the Read mode. Output data is transmitted to the ports in the Write mode.

Every data transmission from the PI4IOE5V9675 must consist of an even number of bytes, the first byte will be referred to as P07 to P00, and the second byte as P17 to P10. The third will be referred to as P07 to P00, and so on.

This quasi-bidirectional I/O can be used as an input or output without the use of a control signal for data directions. At power-on the I/Os are HIGH. In this mode only a current source ( $I_{OH}$ ) to VCC is active. An additional strong pull-up to VCC ( $I_{trt}(pu)$ ) allows fast rising edges into heavily loaded outputs. These devices turn on when an output is written HIGH, and are switched off by the negative edge of SCL. The I/Os should be HIGH before being used as inputs. After power-on, as all the I/Os are set HIGH, all of them can be used as inputs. Any change in setting of the I/Os as either inputs or outputs can be done with the write mode.

Remark: If a HIGH is applied to an I/O which has been written earlier to LOW, a large current ( $I_{OL}$ ) will flow to GND.

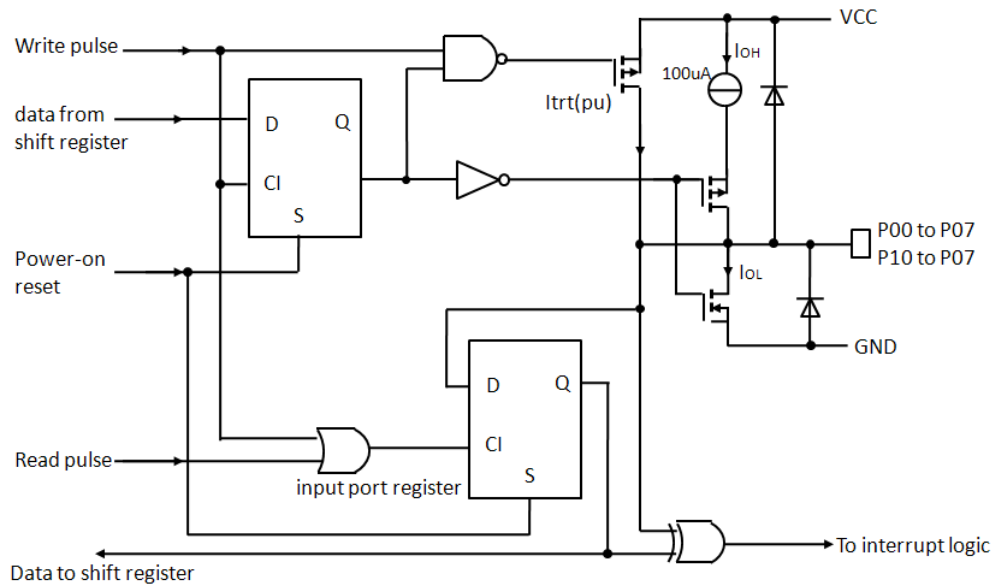


Figure 6. Simplified schematic diagram of P00 to P17

### Writing to the port (Output mode)

To write, the master (microcontroller) first addresses the slave device. By setting the last bit of the byte containing the slave address to logic 0 the Write mode is entered. The PI4IOE5V9675 acknowledges and the master sends the first data byte for P07 to P00. After the first data byte is acknowledged by the PI4IOE5V9675, the second data byte P17 to P10 is sent by the master. Once again, the PI4IOE5V9675 acknowledges the receipt of the data. Each 8-bit data is presented on the port lines after it has been acknowledged by the PI4IOE5V9675.

The number of data bytes that can be sent successively is not limited. After every two bytes, the previous data is overwritten.

The first data byte in every pair refers to Port 0 (P07 to P00), whereas the second data byte in every pair refers to Port 1 (P17 to P10).

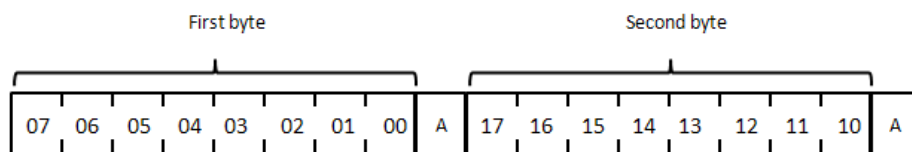


Figure 7. Correlation between bits and ports

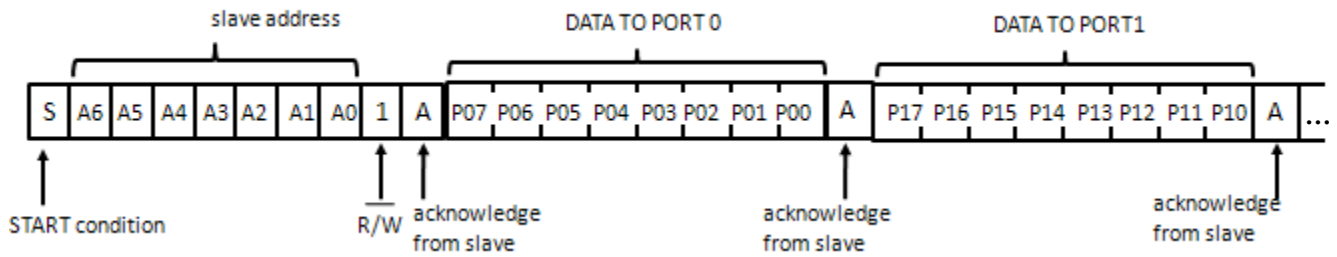


Figure 8. Write Mode

### Reading from a port (Input mode)

All ports programmed as input should be set to logic 1. To read, the master (microcontroller) first addresses the slave device after it receives the interrupt. By setting the last bit of the byte containing the slave address to logic 1 the Read mode is entered.

The data bytes that follow on the SDA are the values on the ports.

If the data on the input port changes faster than the master can read, this data may be lost. Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid.

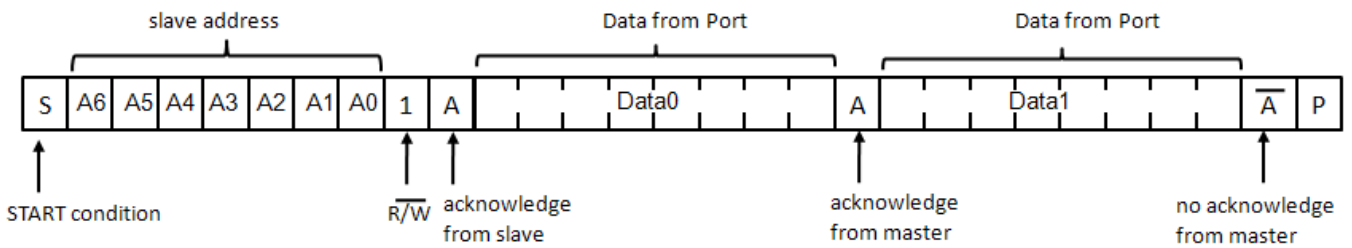


Figure 9. Read input port register

## Power-on reset

When power is applied to VCC, an internal Power-On Reset (POR) holds the PI4IOE5V9675 in a reset condition until VCC has reached VPOR. At that point, the reset condition is released and the PI4IOE5V9675 registers and I<sup>2</sup>C-bus/SMBus state machine will initialize to their default states. Thereafter VCC must be lowered below 0.2 V to reset the device.

## Interrupt output (INT)

The PI4IOE5V9675 provides an open-drain interrupt (INT) which can be fed to a corresponding input of the microcontroller. This gives these chips a kind of master function which can initiate an action elsewhere in the system.

An interrupt is generated by any rising or falling edge of the port inputs. After time  $t_{(V)D}$  the signal INT is valid.

The interrupt disappears when data on the port is changed to the original setting or data is read from or written to the device which has generated the interrupt.

In the write mode, the interrupt may become deactivated (HIGH) on the rising edge of the write to port pulse. On the falling edge of the write to port pulse the interrupt is definitely deactivated (HIGH).

The interrupt is reset in the read mode on the rising edge of the read from port pulse.

During the resetting of the interrupt itself, any changes on the I/Os may not generate an interrupt. After the interrupt is reset any change in I/Os will be detected and transmitted as an INT.

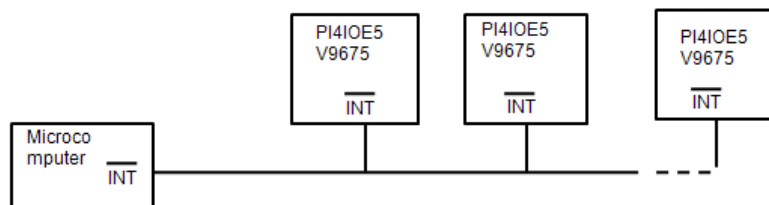


Figure 10. Bidirectional I/O expander application

## Bidirectional I/O expander applications

In the 8-bit I/O expander application shown in Figure 11, P00 and P01 are inputs, and P02 to P07 are outputs. When used in this configuration, during a write, the input (P00 and P01) must be written as HIGH so the external devices fully control the input ports. The desired HIGH or LOW logic levels may be written to the I/Os used as outputs (P02 to P07). During a read, the logic levels of the external devices driving the input ports (P00 and P01) and the previous written logic level to the output ports (P02 to P07) will be read. The GPIO also has an interrupt line (INT) that can be connected to the interrupt logic of the microprocessor. By sending an interrupt signal on this line, the remote I/O informs the microprocessor that there is incoming data or a change of data on its ports without having to communicate via the I<sup>2</sup>C-bus.

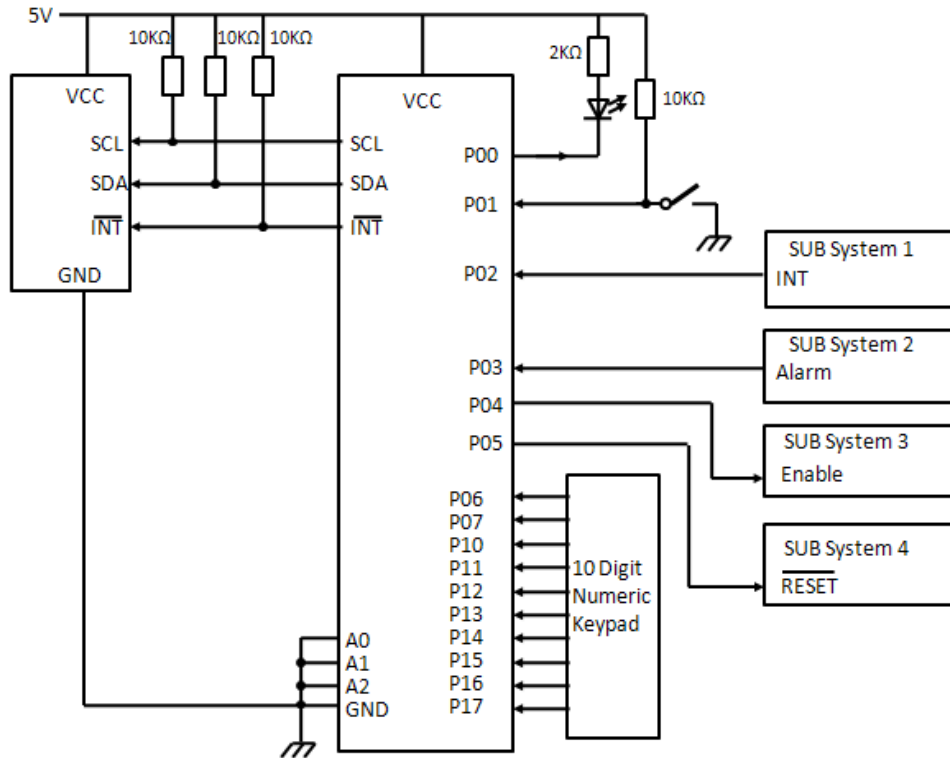


Figure 11. Bidirectional I/O expander application

### High current-drive load applications

The GPIO has a maximum sinking current of 25 mA per bit. In applications requiring additional drive, two port pins in the same octal may be connected together to sink up to 50 mA current. Both bits must then always be turned on or off together. Up to 8 pins (one octal) can be connected together to drive 200 mA.

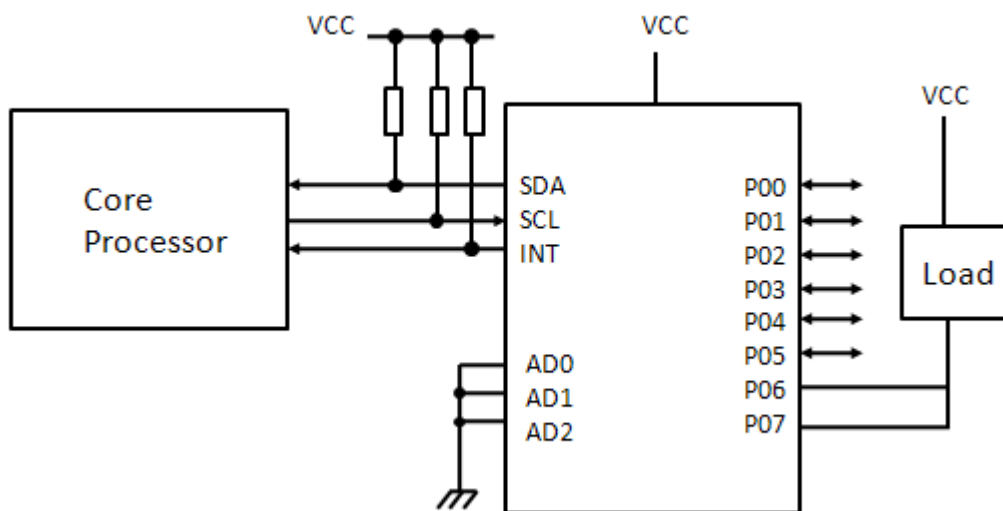
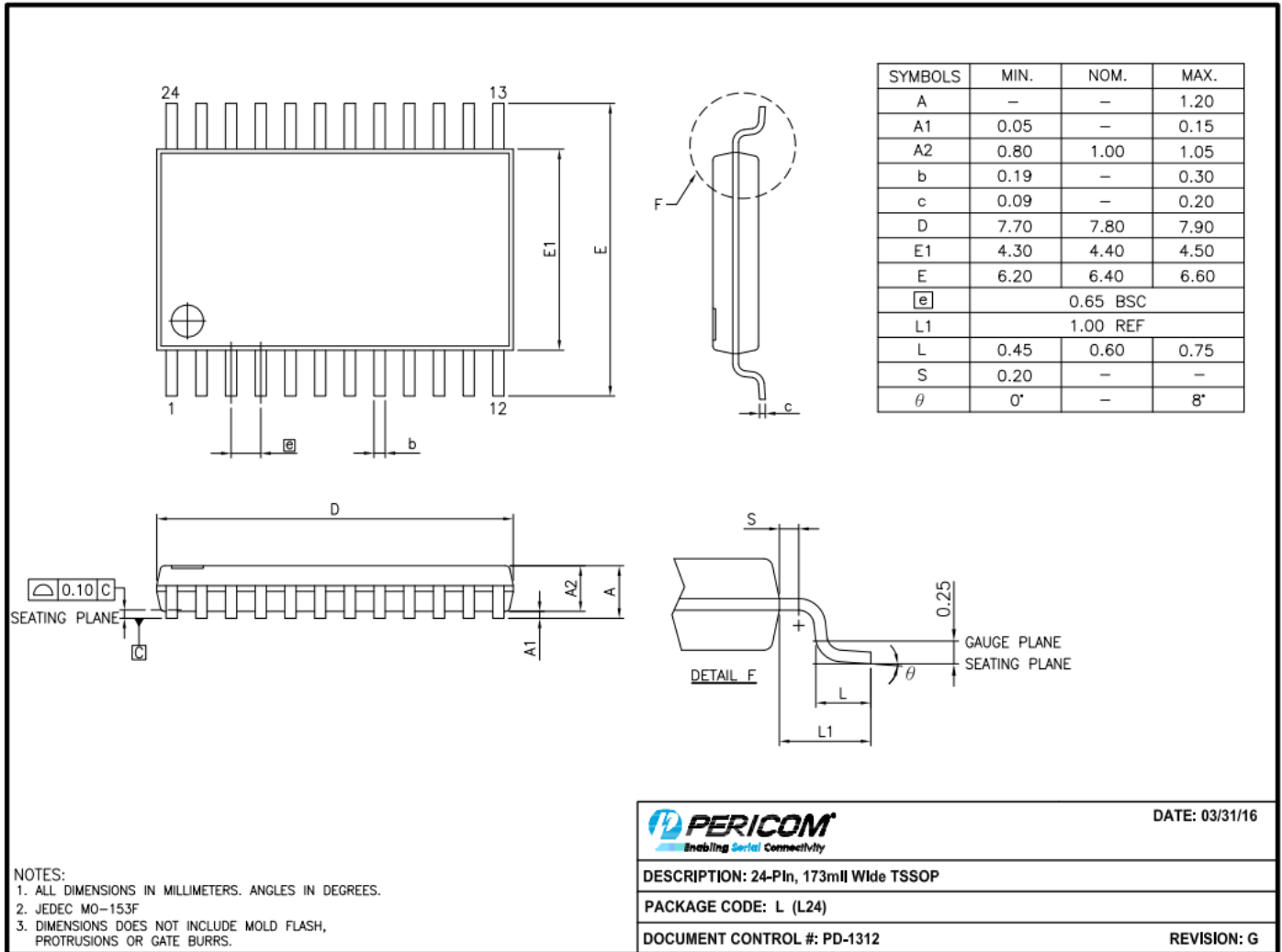
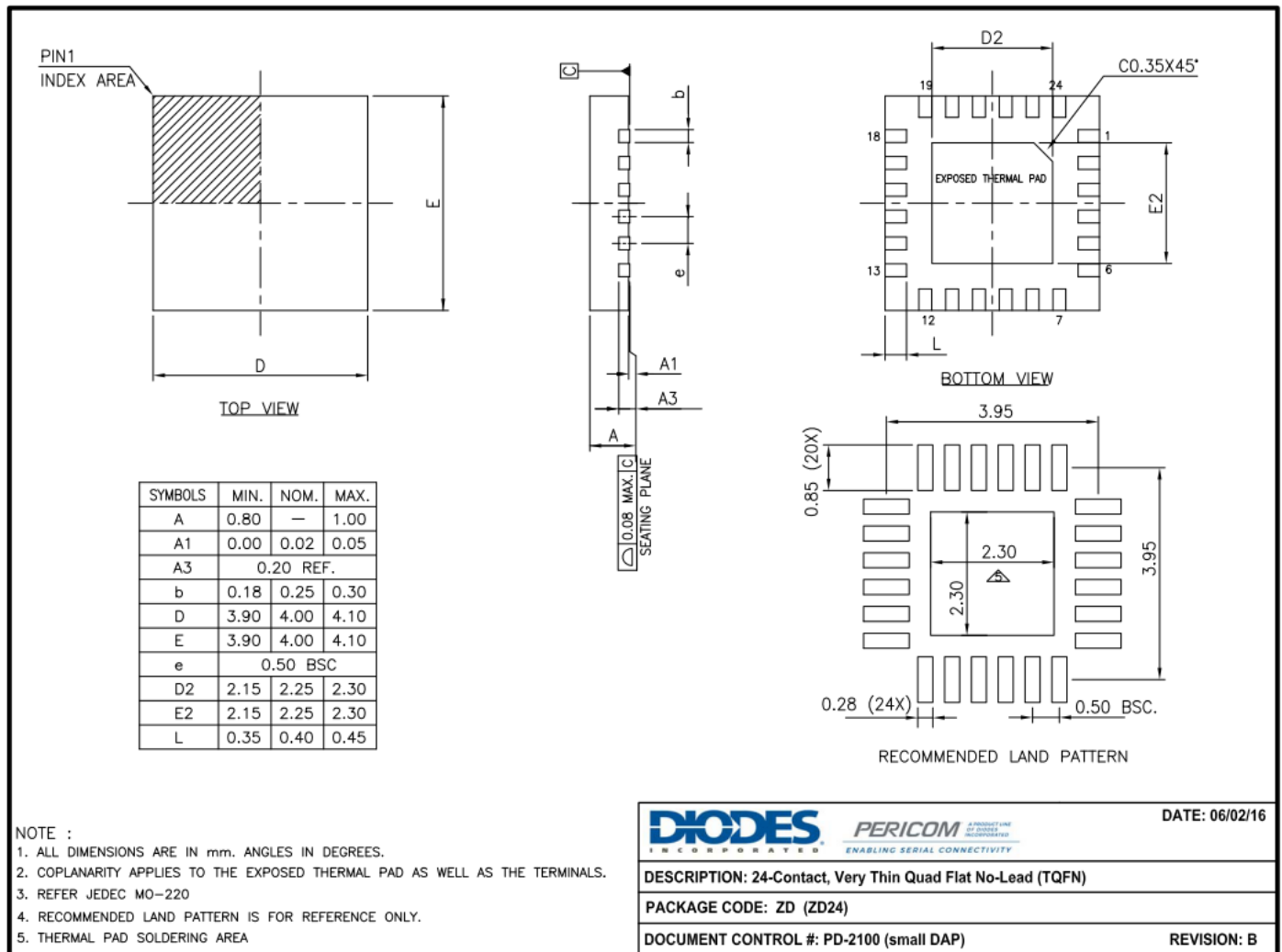


Figure 12. High current-drive load application

**Mechanical Information**  
TSSOP-24(L)



TQFN 4x4-24(ZD)



## Ordering Information

| Part No.         | Package Code | Package  |
|------------------|--------------|--|
| PI4IOE5V9675LE   | L            | Lead free and Green 24-pin TSSOP24(173mil wide)              |
| PI4IOE5V9675LEX  | L            | Lead free and Green 24-pin TSSOP24(173mil wide), Tape & Reel |
| PI4IOE5V9675ZDEX | ZD           | Lead free and Green 24-pin TQFN4.0x4.0, Tape & Reel          |

**Note:**

- E = Pb-free and Green
- Adding X Suffix= Tape/Reel

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