A Product Line of
Diodes Incorporated

PI6CB332000

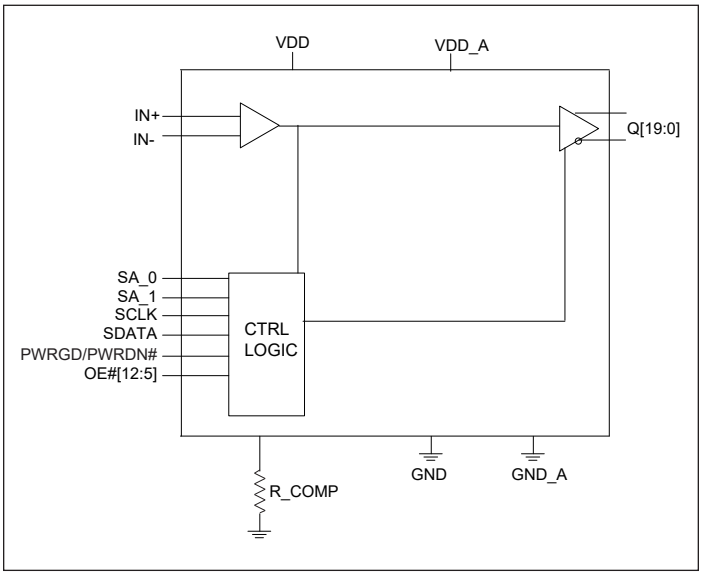
20-Output PCIe 4.0/5.0/6.0 Clock Buffer With On-Chip Termination

Description

The DIODES PI6CB332000 is an 20-output very low-power PCIe clock buffer. It is capable of distributing the reference clocks for UPI, SAS, SATA, and other applications as well. It takes an reference input to fanout 20 100MHz low-power differential HCSL outputs with on-chip terminations. The on-chip termination can save 80 external resistors and make layout easier. 8 OE pins combined with SMBus register pins for controlling each output provides easier power management.

It uses Diodes' proprietary design to achieve very-low jitter that meets PCIe Gen 1/Gen 2/Gen 3/Gen 4/Gen 5/Gen 6 requirement.

Block Diagram



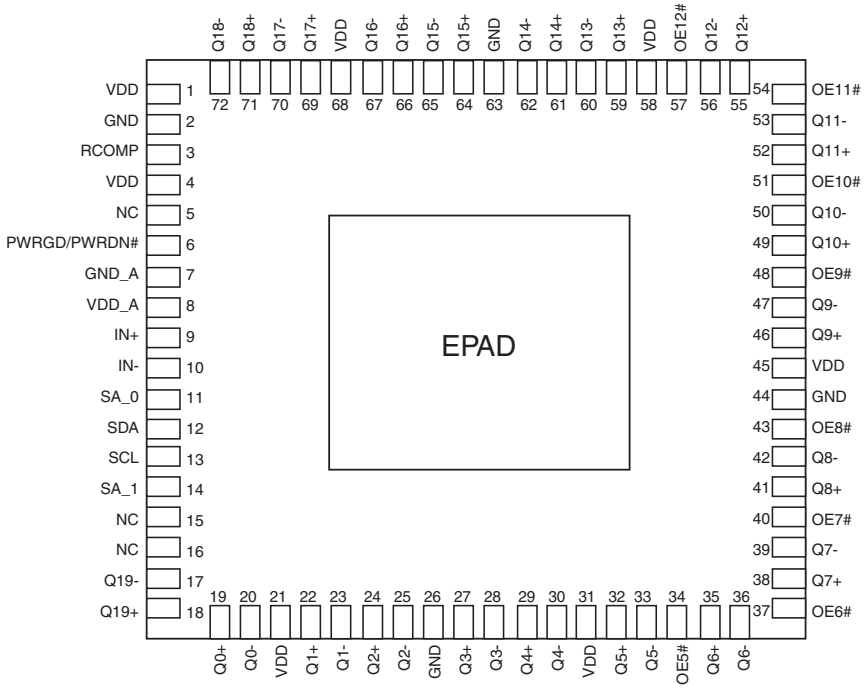
Features

- Supports Intel's DB2000Q Pinout
- 3.3V Supply Voltage
- HCSL Input: 100MHz (Typical), Up to 200MHz
- 20 Differential Low-Power HCSL Outputs with On-Chip Termination
- Strapping Pins or SMBus for Configuration
- Very-Low Jitter Outputs
  - Differential Additive Phase Jitter: DB2000Q <30fs RMS
  - Differential Additive Phase Jitter: PCIe Gen 4 <30fs RMS
  - Differential Additive Phase Jitter: PCIe Gen 5 <20fs RMS
  - Differential Additive Phase Jitter: PCIe Gen 6 <16fs RMS
  - PCIe® Gen 1/Gen 2/Gen 3/Gen 4/Gen 5/Gen 6 Compliant
- Differential Output-to-Output Skew <50ps
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/
- Packaging (Pb-free & Green):
  - 72-lead 10mm × 10mm TQFN

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration



Pin Description

Pin Number	Pin Name	Type		Description
1	VDD	Power	—	Power Supply, Nominal 3.3V
2	GND	Power	—	Connect to Ground
3	RCOMP	Input	—	Connect 412Ω resistor to this pin. Device functions even if this pin is not connected.
4	VDD	Power	—	Power Supply, Nominal 3.3V(1)
5	NC	—	—	No Connect
6	PWRGD/PWRDN#	Input	—	Power Good Enable or Power Down Pin. When powered down, outputs are LOW.
7	GND_A	Power	—	Connect to Ground
8	VDD_A	Power	—	Power Supply, Nominal 3.3V
9	IN+	Input	—	Differential True Clock Input
10	IN-	Input	—	Differential Complementary Clock Input
11	SA_0	Input	—	Address Selection pin, Pulled High
12	SDA	Input/ Output	—	Open Collector for SMBUS Data
13	SCL	Input	—	SMBUS Slave Clock Input
14	SA_1	Input	—	Address Selection Pin, Pulled High

Pin Number	Pin Name	Type		Description
15	NC	—	—	No Connect
16	NC	—	—	No Connect
17	Q19-	Output	HCSL	Differential Complementary Clock Output
18	Q19+	Output	HCSL	Differential True Clock Output
19	Q0+	Output	HCSL	Differential True Clock Output
20	Q0-	Output	HCSL	Differential Complementary Clock Output
21	V_{DD}	Power	—	Power Supply, Nominal 3.3V
22	Q1+	Output	HCSL	Differential True Clock Output
23	Q1-	Output	HCSL	Differential Complementary Clock Output
24	Q2+	Output	HCSL	Differential True Clock Output
25	Q2-	Output	HCSL	Differential Complementary Clock Output
26	GND	Power	—	Ground
27	Q3+	Output	HCSL	Differential True Clock Output
28	Q3-	Output	HCSL	Differential Complementary Clock Output
29	Q4+	Output	HCSL	Differential True Clock Output
30	Q4-	Output	HCSL	Differential Complementary Clock Output
31	VDD	Power	—	Power Supply, Nominal 3.3V
32	Q5+	Output	HCSL	Differential True Clock Output
33	Q5-	Output	HCSL	Differential Complementary Clock Output
34	OE5#	Input	CMOS	Active Low Input for Enabling Q5 Pair. 1 = disable outputs, 0 = enable outputs
35	Q6+	Output	HCSL	Differential True Clock Output
36	Q6-	Output	HCSL	Differential Complementary Clock Output
37	OE6#	Input	CMOS	Active Low Input for Enabling Q6 Pair. 1 = disable outputs, 0 = enable outputs
38	Q7+	Output	HCSL	Differential True Clock Output
39	Q7-	Output	HCSL	Differential Complementary Clock Output
40	OE7#	Input	CMOS	Active Low Input for Enabling Q7 Pair. 1 = disable outputs, 0 = enable outputs
41	Q8+	Output	HCSL	Differential True Clock Output
42	Q8-	Output	HCSL	Differential Complementary Clock Output
43	OE8#	Input	CMOS	Active Low Input for Enabling Q8 Pair. 1 = disable outputs, 0 = enable outputs
44	GND	Power	—	Ground
45	V_{DD}	Power	—	Power Supply, Nominal 3.3V
46	Q9+	Output	HCSL	Differential True Clock Output
47	Q9-	Output	HCSL	Differential Complementary Clock Output

Pin Number	Pin Name	Type		Description
48	OE9#	Input	CMOS	Active Low Input for Enabling Q9 Pair. 1 = disable outputs, 0 = enable outputs
49	Q10+	Output	HCSL	Differential True Clock Output
50	Q10-	Output	HCSL	Differential Complementary Clock Output
51	OE10#	Input	CMOS	Active Low Input for Enabling Q10 Pair. 1 = disable outputs, 0 = enable outputs
52	Q11+	Output	HCSL	Differential True Clock Output
53	Q11-	Output	HCSL	Differential Complementary Clock Output
54	OE11#	Input	CMOS	Active Low Input for Enabling Q11 Pair. 1 = disable outputs, 0 = enable outputs
55	Q12+	Output	HCSL	Differential True Clock Output
56	Q12-	Output	HCSL	Differential Complementary Clock Output
57	OE12#	Input	CMOS	Active Low Input for Enabling Q12 Pair. 1 = disable outputs, 0 = enable outputs
58	VDD	Power	—	Power Supply, Nominal 3.3V
59	Q13+	Output	HCSL	Differential True Clock Output
60	Q13-	Output	HCSL	Differential Complementary Clock Output
61	Q14+	Output	HCSL	Differential True Clock Output
62	Q14-	Output	HCSL	Differential Complementary Clock Output
63	GND	Power	—	Ground
64	Q15+	Output	HCSL	Differential True Clock Output
65	Q15-	Output	HCSL	Differential Complementary Clock Output
66	Q16+	Output	HCSL	Differential True Clock Output
67	Q16-	Output	HCSL	Differential Complementary Clock Output
68	VDD	Power	—	Power Supply, Nominal 3.3V
69	Q17+	Output	HCSL	Differential True Clock Output
70	Q17-	Output	HCSL	Differential Complementary Clock Output
71	Q18+	Output	HCSL	Differential True Clock Output
72	Q18-	Output	HCSL	Differential Complementary Clock Output
—	EPAD	Power	—	Connect to Ground

Note:
1. This pin can be left as NC.

Table 1. SMBus Address Selection

SA_1	SA_0	Address
L	L	D8
L	M	DA
L	H	DE
M	L	C2
M	M	C4
M	H	C6
H	L	CA
H	M	CC
H	H	CE

Table 2. Power Management

PWRGD/PWRDN#	Q+	Q-
0	Low	Low
1	Normal	Normal

Table 3. OE Functionality

Inputs		OE# Hardware Pins and Control Register Bits			
PWRGD/PWRDN#	IN+/IN-	SMBUS Enable Bit	OE# Pin	Q+/Q- [12:5]	Q+/Q- [18:13], [4:0]
0	X	X	X	Low/Low	Low/Low
1	Running	0	X	Low/Low	Low/Low
		1	0	Running	Running
		1	1	Low/Low	Running

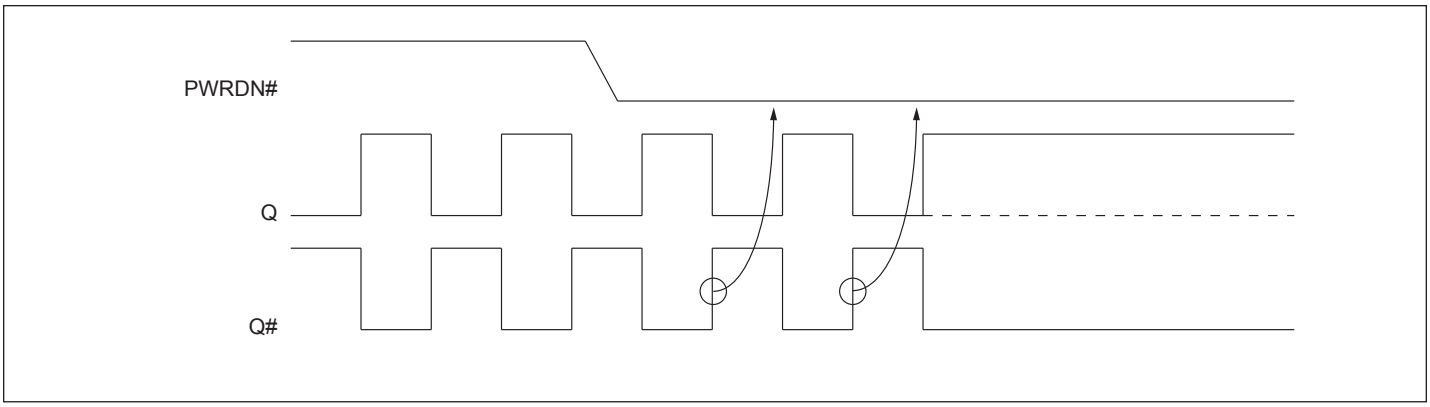


Figure 1. PWRDN# Assertion

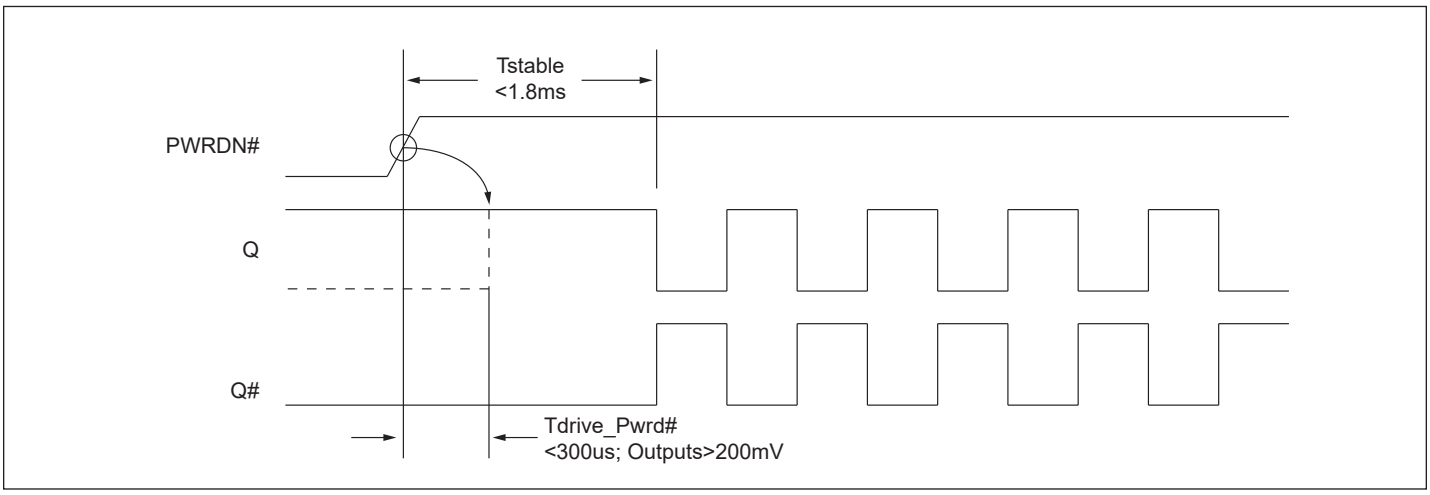


Figure 2. PWRGD Assertion

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature..... –65°C to +150°C
Supply Voltage to Ground Potential, V_{DDxx} .....–0.5V to +4.0V
Input Control Pins Voltage ..... –0.5V to V_{DD}+0.5V
CLK+/- Pins .....-0.5V to 2.5V
SMBus, Input High Voltage 3.6V
ESD Protection (HBM) 2000V
Junction Temperature ....125 °C Max.

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Conditions

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{DD}, V_{DD_A}	Power Supply Voltage	—	3.135	3.3	3.465	V
I_{DD}	Power Supply Current	V_{DD} + V_{DDA}, All outputs active @ 100MHz	—	210	250	mA
I_{DD_PD}	Power Supply Power Down[1] Current	V_{DD} + V_{DDA}, All outputs LOW/ LOW	—	1.8	3.0	mA
T_A	Ambient Temperature	Industrial grade	–40	—	85	°C

Note:
1. Input clock is not running.

Input Electrical Characteristics

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
R_{pu}	Internal Pull-Up Resistance	—	—	120	—	KΩ
R_{dn}	Internal Pull-Down Resistance	—	—	120	—	KΩ
L_{PIN}	Pin Inductance	—	—	—	7	nH

SMBus Electrical Characteristics

Temperature = T_A. Supply voltages per normal operation conditions. See test circuits for load conditions.

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{DDSMB}	Nominal Bus Voltage	—	2.7	—	3.6	V
V_{IHSMB}	SMBus Input High Voltage	SMBus, V_{DDSMB} = 3.3V	2.1	—	3.6	V
		SMBus, V_{DDSMB} < 3.3V	0.65 V_{DDSMB}	—	—	
V_{ILSMB}	SMBus Input Low Voltage	SMBus, V_{DDSMB} = 3.3V	—	—	0.6	V
		SMBus, V_{DDSMB} < 3.3V	—	—	0.6	

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
$I_{SMBSINK}$	SMBus Sink Current	SMBus, at V_{OLSMB}	4	—	—	mA
V_{OLSMB}	SMBus Output Low Voltage	SMBus, at $I_{SMBSINK}$	—	—	0.4	V
f_{MAXSMB}	SMBus Operating Frequency	Maximum frequency	—	—	400	kHz
t_{RMSB}	SMBus Rise Time	(Max V_{IL} - 0.15) to (Min V_{IH} + 0.15)	—	—	1000	ns
t_{FMSB}	SMBus Fall Time	(Min V_{IH} + 0.15) to (Max V_{IL} - 0.15)	—	—	300	ns

LVCMOS DC Electrical Characteristics

Temperature = T_A. Supply voltages per normal operation conditions. See test circuits for the load conditions.

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	Single-ended inputs except trilevel pins	2	—	V_{DD} +0.3	V
V_{IL}	Input Low Voltage	Single-ended inputs except trilevel pins	-0.3	—	0.8	V
V_{IH}	Input High Voltage	Single-ended trilevel inputs	2.4	—	V_{DD} +0.3	V
V_{IM}	Input Mid Voltage	Single-ended trilevel inputs	1.2	$0.5V_{DD}$	1.8	V
V_{IL}	Input Low Voltage	Single-ended trilevel inputs	-0.3	—	0.9	V
I_{IH}	Input High Current	Single-ended inputs, $V_{IN} = V_{DD}$		—	5	mA
I_{IL}	Input Low Current	Single-ended inputs, $V_{IN} = 0V$	-5	—	—	µA
I_{IH}	Input High Current	Single-ended inputs with pull-up resistor, $V_{IN} = V_{DD}$	—	—	5	mA
I_{IL}	Input Low Current	Single-ended inputs with pull-up resistor, $V_{IN} = 0V$	-50	—	—	µA
C_{IN}	Input Capacitance	—	1.5	—	5	pF
t_{RF}	Rise/Fall Time of Input	—	—	—	5	ns

LVCMOS AC Electrical Characteristics

Temperature = T_A. Supply voltages per normal operation conditions. See test circuits for the load conditions.

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
t_{OELAT}	Output Enable Latency	Q start after OE# assertion Q stop after OE# deassertion	1	6	10	clocks
t_{PDLAT}	PD# Deassertion	Differential outputs enable after PD# deassertion	—	200	300	µs

HCSL Input Characteristics(1)

Temperature = T_A. Supply voltages per normal operation conditions. See test circuits for the load conditions.

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Frequency	—	1	100	200	MHz
V_{IHDIF}	Differential Input High Voltage(3)	IN+, IN-, single-ended measurement	330	—	1150	mV
V_{ILDIF}	Differential Input Low Voltage(3)	IN+, IN-, single-ended measurement	-300	0	300	mV
V_{SWING}	Differential Input Swing Voltage	Peak-to-peak value (V_{IHDIF} - V_{ILDIF})	200	—	—	mV
V_{COM}	Common Mode Voltage	—	0	—	900	mV
t_{RF}	Differential Input Slew Rate(2)	—	0.7	—	—	V/ns
I_{IN}	Differential Input Leakage Current	$V_{IN} = V_{DD}$, V_{IN} = GND	-5	—	5	µA
t_{DC}	Differential Input Duty Cycle	Measured differentially	45	—	55	%
tj_{c-c}	Differential Input Cycle-to-Cycle Jitter	Measured differentially	—	—	125	ps

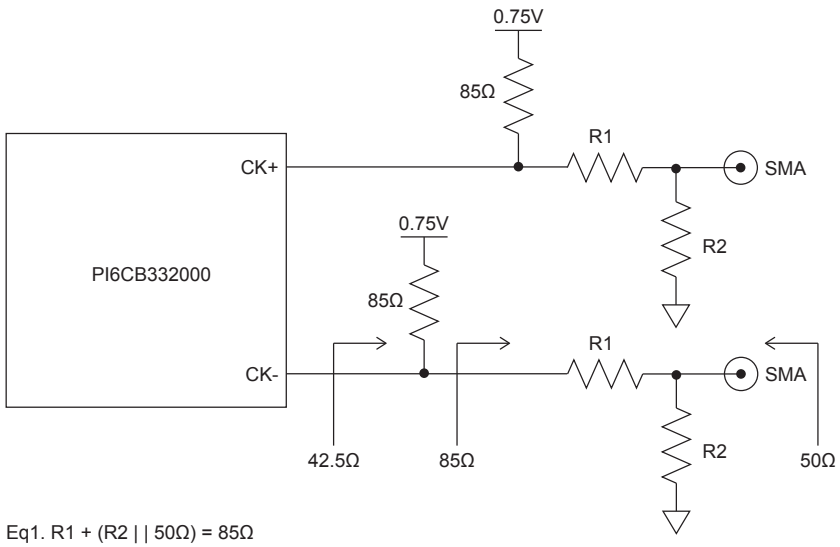
Note:
1. Guaranteed by design and characterization—not 100% tested in production.
2. Slew rate measured through ±75mV window centered around differential zero.
3. The device can be driven by a single-ended clock by driving the true clock and biasing the complement clock input to the Vbias, where Vbias is (V_{IH}-V_{IL})/2.

HCSL Output DC Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output Voltage High(1)	—	225	—	270	mV
V_{OL}	Output Voltage Low(1)		10	0	150	mV
V_{OMAX}	Output Voltage Maximum (Overshoot)(1)	—	—	—	V_{OH} + 75mV	mV
V_{OMIN}	Output Voltage Minimum (Undershoot)(1)		V_{OL} + 75mV	—	—	mV
Vcross absolute	Absolute Crossing Point Voltage(1,2)	—	130	—	200	mV
Vcross relative	Relative Crossing Point Voltage(1,2)	—	—	—	35	mV
DC Distortion	Duty Cycle Distortion(3,4)	—	-1	—	1	%

Note:
1. At default SMBUS amplitude settings.
2. Guaranteed by design and characterization—not 100% tested in production.
3. Measured from differential waveform.
4. Duty cycle distortion is the difference in duty cycle between the out and input clock when the device is operated in the PLL bypass mode.



Eq1. R1 + (R2 | | 50Ω) = 85Ω

Eq2. ((42.5Ω | | 85Ω) + R1) | | R2 = 50Ω

R1 = 47.8Ω, standard 1% value R1 = 47Ω
R2 = 145.8Ω, standard 1% value R2 = 147Ω

Figure 3. HCSL Output DC Test Load

HCSL Output AC Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
f_{OUT}	Output Frequency	—	—	100	200	MHz
t_{RF}	Slew Rate[1,2,3]	Scope averaging on, 10in trace	1.5	3.0	4	V/ns
Dt_{RF}	Slew Rate Matching[1,2,4]	Scope averaging on, 10in trace	—	—	20	%
t_{SKEW}	Output Skew[1,2]	Averaging on, V_T = 50%	—	—	50	ps
V_{MAX}	Maximum Output Voltage	Measurement on single ended signal using absolute value	660	780	850	mV
V_{MIN}	Minimum Output Voltage		-150	20	150	mV
tj_{c-c}	Additive Cycle-to-Cycle Jitter[1,2]	—	—	0	0.05	ps
T_{pd}	Propagation Delay	—	—	1.5	2	ns

PCIe Common Clock (CC) Architecture Jitter

Symbol	Parameters	Condition	Min.	Typ.	Max.	Spec Limit	Units
t_{jPHASE}	Additive Integrated Phase Jitter (RMS)(1,2,7,8)	PCIe Gen 1(6)	—	0	0.03	86	ps (pkpk)
		PCIe Gen 2 Low Band, 10kHz < f < 1.5MHz (PLL BW 5-16MHz or 8-5MHz, CDR = 10MHz)	—	0	0.03	3	ps
		PCIe Gen 2 High Band, 1.5MHz < f < Nyquist (50MHz); (PLL BW 5-16MHz or 8-5MHz, CDR = 10MHz)	—	0	0.03	3.1	ps
		PCIe Gen 3 (PLL BW 2-4MHz or 2-5MHz, CDR = 10MHz)	—	0	0.03	1	ps
		PCIe Gen 4 (PLL BW 2-4MHz or 2-5MHz, CDR = 10MHz)	—	0	0.03	0.5	ps
		PCIe Gen 5 (PLL BW of 500K to 1.8MHz, CDR = 20MHz) (9)	—	0.015	0.03	0.15	ps
		PCIe Gen 6 (PLL BW 500K to 1MHz, CDR = 10MHz)	—	0.008	0.016	0.1	ps
		100MHz (12kHz to 20MHz), input jitter ~156fs	—	87	120	NA(10)	fs
		156.25MHz (12kHz to 20MHz), input jitter ~110fs	—	47	100	NA(10)	fs
		100MHz, apply DB2000Q filter, see figure 5	—	—	25	80	fs

Note:
1. Guaranteed by design and characterization—not 100% tested in production.
2. Measured from differential waveform.
3. Slew rate is measured through the Vswing voltage range centered around differential 0V within ±150mV window.
4. Slew rate matching is measured through ±75mV window centered around differential zero.
5. See http://www.pcisig.com for complete specifications.
6. Sample size of at least 100k cycles. This can be extrapolated to 108ps pk-pk @ 1M cycles for a BER of 10^{-12}.
7. Applies to all differential outputs.
8. For additive jitter RMS value is calculated by the following equation = SQRT [(total jitter)*^{2} - (input jitter)*^{2}].
9. PCIe Gen 5 v0.9 specification
10. Not available.

PCIe Independent Reference Clock Architecture Jitter

Symbol	Parameters	Condition	Min.	Typ.	Max.	Spec Limit	Units
t_{jPHASE}	Additive Integrated Phase Jitter (RMS)	PCIe Gen 3 SRIS (PLL BW 2-4MHz or 2-5MHz, CDR = 10MHz)	—	0	0.03	0.7	ps
		PCIe Gen 4 SRIS (PLL BW 2-4MHz or 2-5MHz, CDR = 10MHz)	—	0	0.03	0.7	ps
		PCIe Gen 4 SRNS (PLL BW 2-4MHz or 2-5MHz, CDR = 10MHz)	—	0	0.03	0.7	ps
		PCIe 5.0 SRIS (PLL BW 500K-1.8MHz, CDR = 20MHz)	—	0.01	0.02	0.177	ps
		PCIe 6.0 SRIS(PLL BW 500K-1MHz, CDR = 10MHz)	—	0.008	0.016	0.106	ps

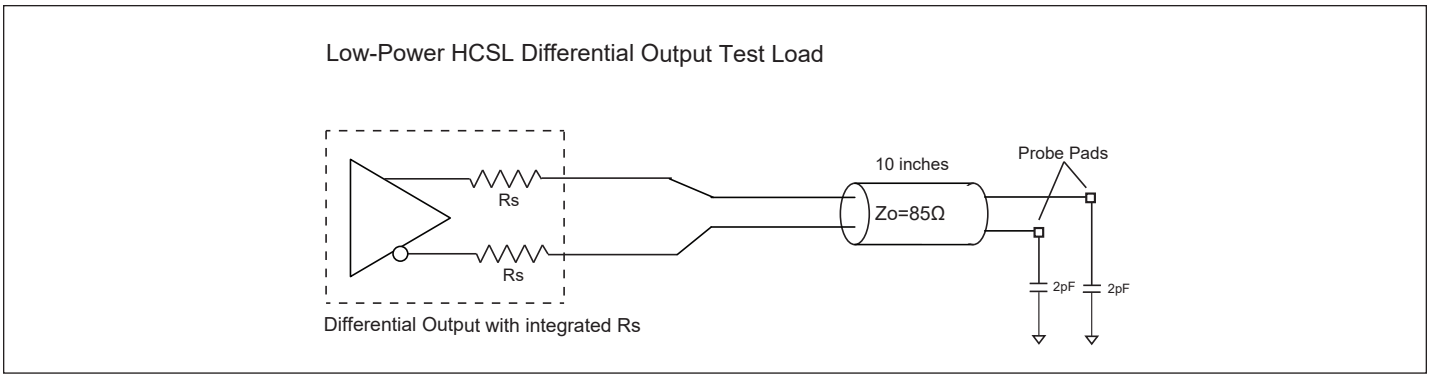


Figure 4. Low Power HCSL AC Test Circuit

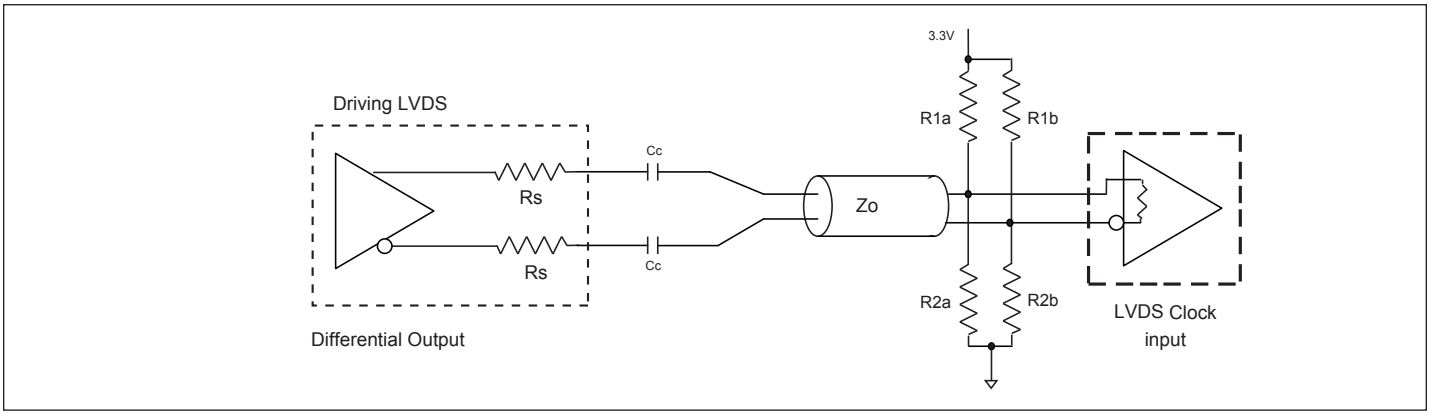


Figure 5. Differential Output Driving LVDS

Table 4. Differential Output Terminations Driving LVDS (Z_0 =100Ω)

Component	Receiver with Termination	Receiver without Termination	Unit
R_{1a}, R_{1b}	10,000	140	Ω
R_{2a}, R_{2b}	5600	75	Ω
C_C	0.1	0.1	µF
V_{CM}	1.2	1.2	V

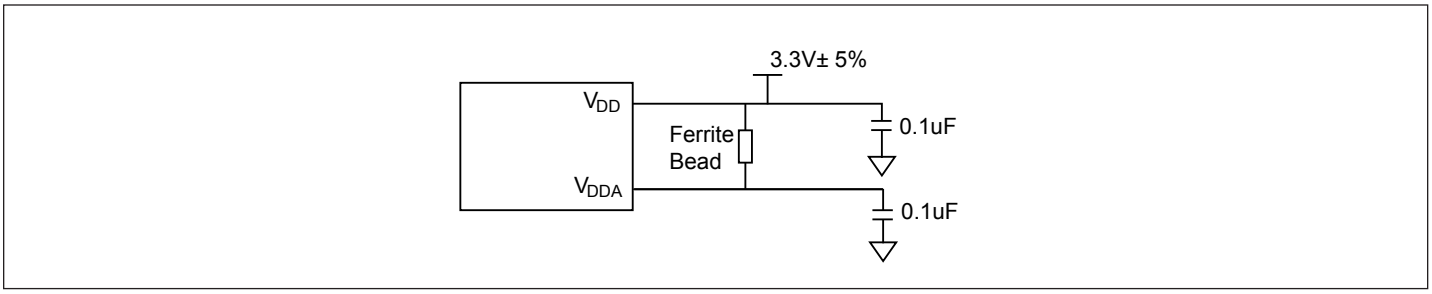


Figure 6. Power Supply Filter

SMBus Serial Data Interface

The PI6CB332000 is a slave only device that supports block read and block write protocol using a single 7-bit address and read/write bit as shown below.

Read and write block transfers can be stopped after any complete byte transfer.

Address Assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	See SMBus Address Selection Table			1/0

Note: SMBus address is latched on SADR pin.

How to Write

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit	8 bits	1 bit		8 bits	1 bit	1 bit
Start Bit	Add.	W(0)	Ack	Beginning Byte Location = N	Ack	Data Byte Count = X	Ack	Beginning Data Byte (N)	Ack	.....	Data Byte (N+X-1)	Ack	Stop Bit

How to Read

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit
Start bit	Address	W(0)	Ack	Beginning Byte Location = N	Ack	Repeat Start Bit	Address	R(1)	Ack	Data Byte Count = X	Ack	Beginning Data Byte (N)	Ack

	8 bits	1 bit	1 bit
.....	Data Byte (N+X-1)	NAck	Stop Bit

Byte 0: Output Enable Register						
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**0**	**1**
7	Reserved	—		1	—	—
6	Q19_OE	Q19 Output Enable	RW	1	Low	Enable
5	Q18_OE	Q18 Output Enable	RW	1	Low	Enable
4	Q17_OE	Q17 Output Enable	RW	1	Low	Enable
3	Q16_OE	Q16 Output Enable	RW	1	Low	Enable
2	Reserved	—	—	0	—	—
1	Reserved	—	—	0	—	—
0	Reserved	—	—	1	—	—

Byte 1: Output Enable Register						
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**0**	**1**
7	Q7_OE	Q7 Output Enable	RW	1	Low	Enable
6	Q6_OE	Q6 Output Enable	RW	1	Low	Enable
5	Q5_OE	Q5 Output Enable	RW	1	Low	Enable
4	Q4_OE	Q4 Output Enable	RW	1	Low	Enable
3	Q3_OE	Q3 Output Enable	RW	1	Low	Enable
2	Q2_OE	Q2 Output Enable	RW	1	Low	Enable
1	Q1_OE	Q1 Output Enable	RW	1	Low	Enable
0	Q0_OE	Q0 Output Enable	RW	1	Low	Enable

Byte 2: Output Enable Register						
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**0**	**1**
7	Q15_OE	Q15 Output Enable	RW	1	Low	Enable
6	Q14_OE	Q14 Output Enable	RW	1	Low	Enable
5	Q13_OE	Q13 Output Enable	RW	1	Low	Enable
4	Q12_OE	Q12 Output Enable	RW	1	Low	Enable
3	Q11_OE	Q11 Output Enable	RW	1	Low	Enable
2	Q10_OE	Q10 Output Enable	RW	1	Low	Enable
1	Q9_OE	Q9 Output Enable	RW	1	Low	Enable
0	Q8_OE	Q8 Output Enable	RW	1	Low	Enable

Byte 3: OE# Pin Realtime Readback Control Register						
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**0**	**1**
7	OE12#	Realtime Readback of OE12#	R	Realtime	OE12# = Low	OE12# = High
6	OE11#	Realtime Readback of OE11#	R	Realtime	OE11# = Low	OE11# = High
5	OE10#	Realtime Readback of OE10#	R	Realtime	OE10# = Low	OE10# = High
4	OE9#	Realtime Readback of OE9#	R	Realtime	OE9# = Low	OE9# = High
3	OE8#	Realtime Readback of OE8#	R	Realtime	OE8# = Low	OE8# = High
2	OE7#	Realtime Readback of OE7#	R	Realtime	OE7# = Low	OE7# = High
1	OE6#	Realtime Readback of OE6#	R	Realtime	OE6# = Low	OE6# = High
0	OE5#	Realtime Readback of OE5#	R	Realtime	OE5# = Low	OE5# = High

Note:

1. B1[5] must be set to 1 for these bits to have any effect on the part.

Byte 4: Reserved						
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**0**	**1**
7:0	Reserved	—	—	0	—	—

Byte 5: Revision and Vendor ID Register						
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**0**	**1**
7	RID3	Revision ID	R	0	Rev = 0000	
6	RID2		R	0		
5	RID1		R	0		
4	RID0		R	0		
3	PVID3	Vendor ID	R	0	Diodes = 0011	
2	PVID2		R	0		
1	PVID1		R	1		
0	PVID0		R	1		

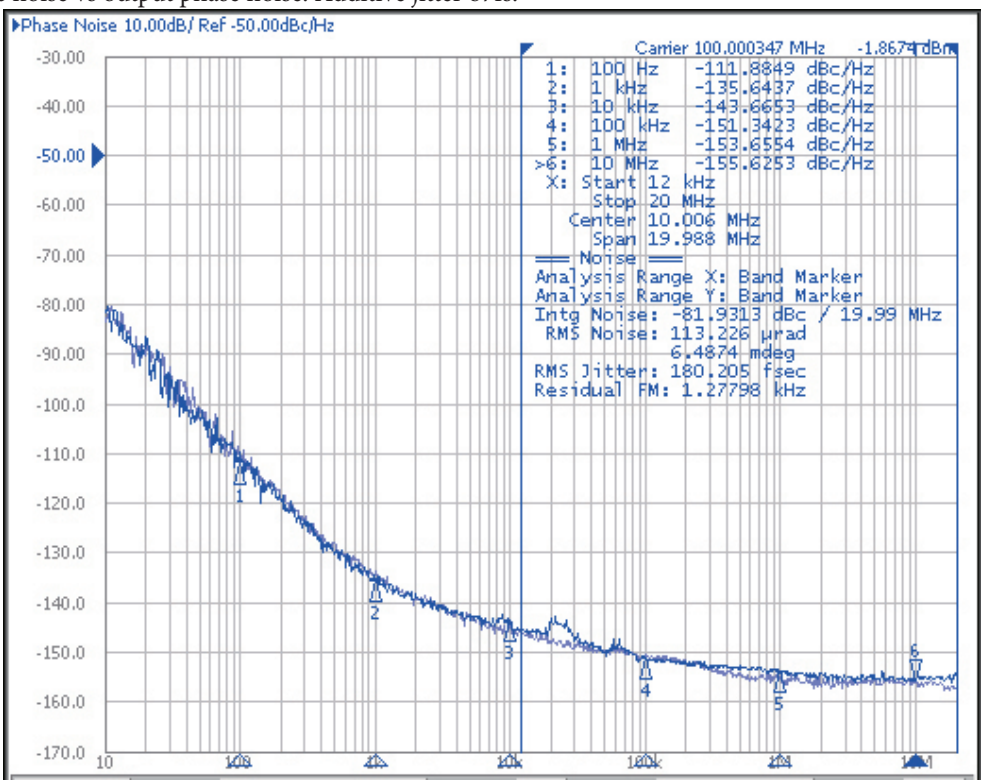
Byte 6: Device Type/Device ID Register						
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**0**	**1**
7	DID7	Device ID	R	0		
6	DID6		R	1		
5	DID5		R	0		
4	DID4		R	0		
3	DID3		R	1		
2	DID2		R	0		
1	DID1		R	0		
0	DID0		R	0		

Byte 7: Byte Count Register						
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**0**	**1**
7	Reserved	—	—	0	—	—
6	Reserved	—	—	0	—	—
5	Reserved	—	—	0	—	—
4	BC4	Byte Count Programming	RW	0	Writing to this register configures how many bytes are read back; default is 8 bytes	
3	BC3		RW	1		
2	BC2		RW	0		
1	BC1		RW	0		
0	BC0		RW	0		

Byte 8: Vendor Specific						
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**0**	**1**
7:0	Reserved	—	—	0	—	—

Phase Noise Plots

100MHz input phase noise vs output phase noise. Additive jitter 87fs.



Achievable output phase noise at 156.25MHz

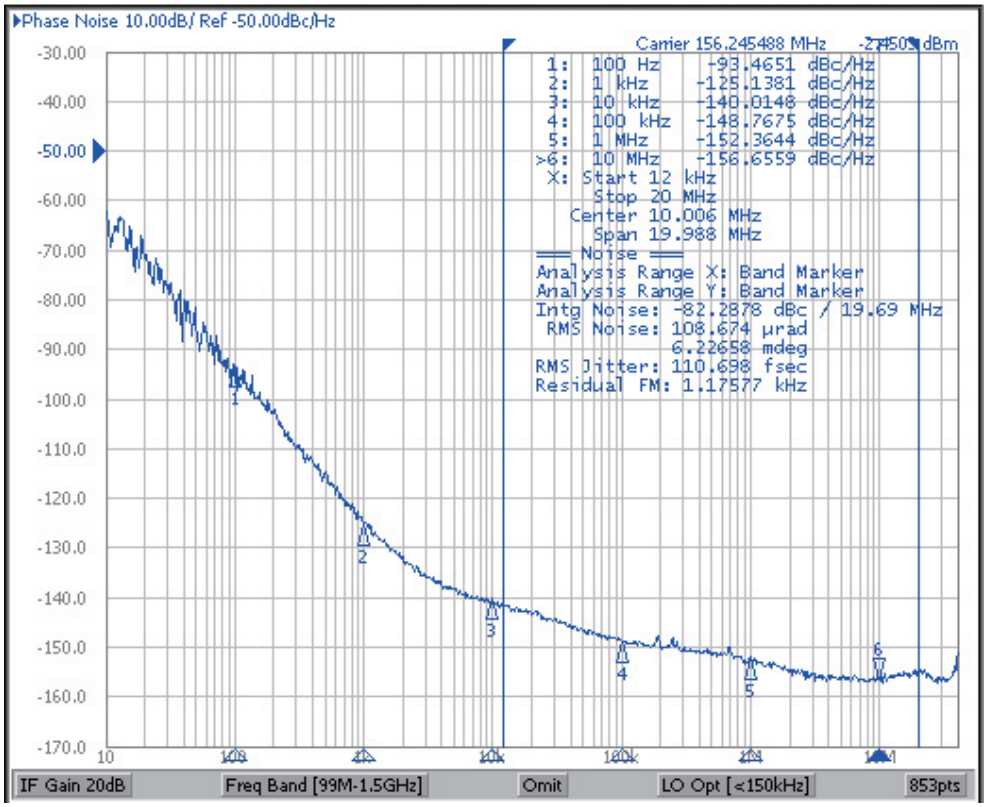


Table 5. Thermal Characteristics

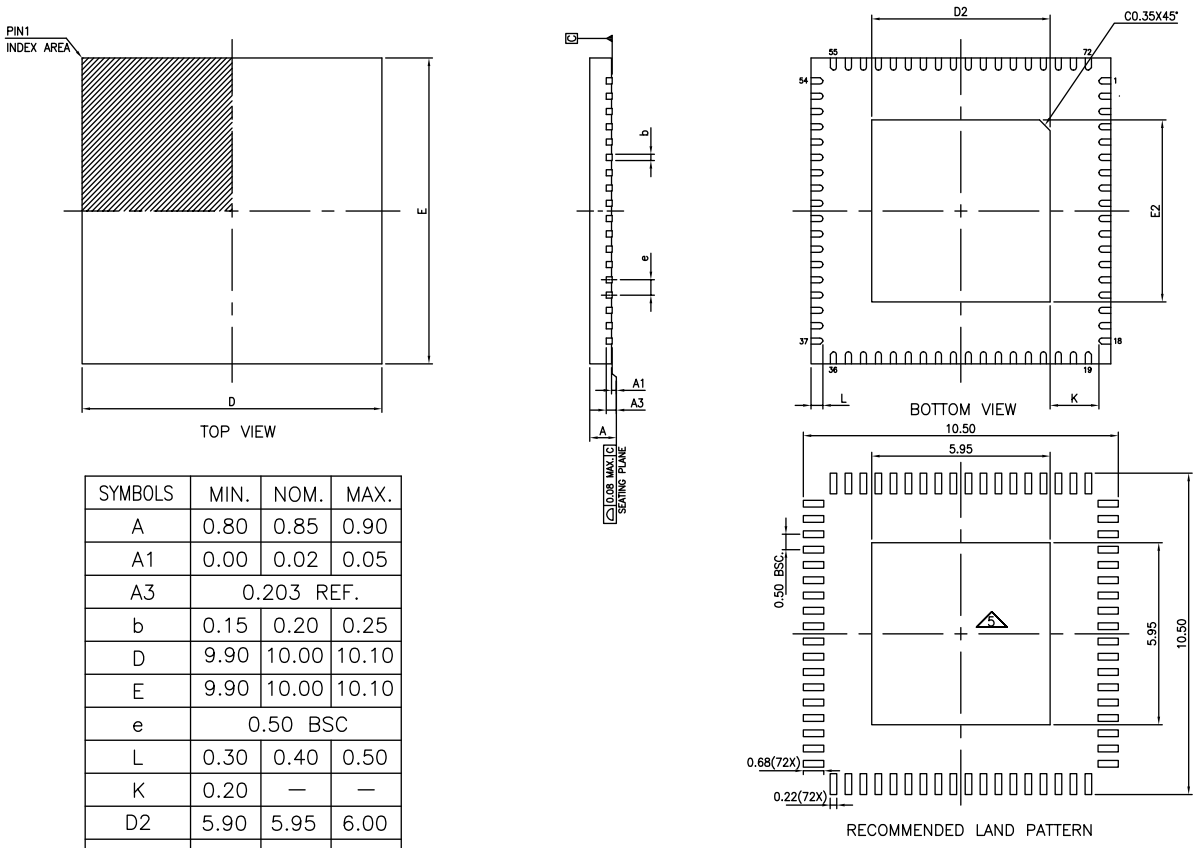
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
θ_{JA}	Thermal Resistance Junction to Ambient	Still air			25.85	°C/W
θ_{JC}	Thermal Resistance Junction to Case				12.55	°C/W

Part Marking

YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

Packaging Mechanical

72-TQFN (ZD)



SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D	9.90	10.00	10.10
E	9.90	10.00	10.10
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
D2	5.90	5.95	6.00
E2	5.90	5.95	6.00

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS
3. REFER JEDEC MO-220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED)

DATE: 09/12/18

DESCRIPTION: 72-Contact, TQFN

PACKAGE CODE: ZD (ZD72)

DOCUMENT CONTROL #: PD-2037 REVISION: E

For latest package information:

See http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/.

Ordering Information

Ordering Code	Package Code	Package Description	Operating Temperature
PI6CB332000ZDIEX	ZD	72-Contact (TQFN)	Industrial

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. I = Industrial
5. E = Pb-free and Green
6. X suffix = Tape/Reel

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