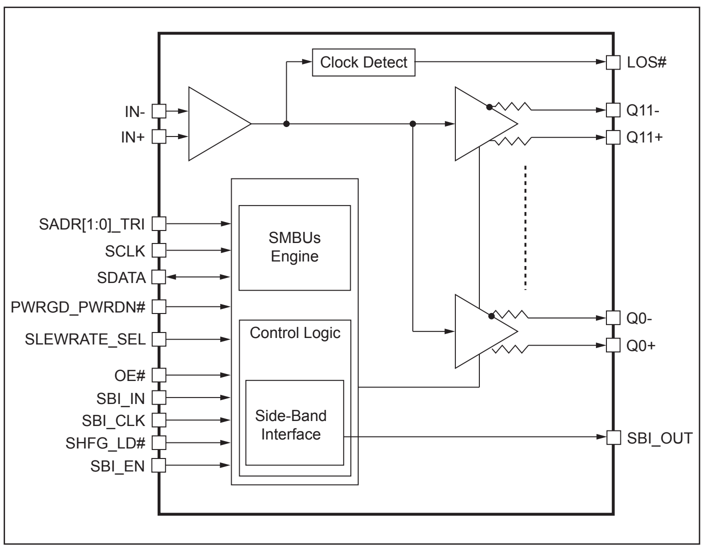
12-Output Low-Power Fanout Clock Buffer for PCIe 6.0 Application

Description

The PI6CB332012A is a low-power PCIe® 5.0/6.0 clock buffer. It takes a reference input to fanout 12 low-power differential HCSL outputs up to 400MHz, with on-chip terminations for 85Ω output impedance. An individual OE pin for each output provides easier power management. The device also supports Power Down Tolerant (PDT), automatic output clock parking upon loss of input clock, and Flexible Startup Sequencing features.

Block Diagram



Features

- 12 Low-Power HCSL Outputs with On-Chip Termination
- 85Ω Output Impedance
- Individual Output Enable
- Power Down Tolerant Inputs
- Flexible Startup Sequencing
- Automatic Output Clock Parking Upon Loss of Input Clock
- Up to 9 Selectable SMBus Addresses
- Supports SBI OE# interface
- Differential Output-to-Output Skew <50ps
- Additive Phase Jitter
  - PCIe 5.0: typical 6fs RMS
  - PCIe 6.0: typical 4fs RMS
  - DB2000QL: typical 10fs RMS
- 3.3V Supply Voltage
- Temperature Range: -40°C to 105°C
- Packaging (Pb-free & Green):
  - 64-Pin, WLGA 5x5mm (FLB)
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration

	1	2	3	4	5	6	7	8	9	10
A	LOS#	Q0-	Q0+	Q1-	Q1+	Q2-	Q2+	Q3-	Q3+	OE4#_ SBI_CLK
B	SADR1_TRI	NC	OE0#	OE1#	VDDCLK	NC	OE2#_ SBI_OUT	OE3#	NC	Q4-
C	SADR0_TRI	SLEWRATE _SEL							VDDCLK	Q4+
D	SCLK	SDATA		GND	GND	GND	GND		NC	Q5-
E	IN+	NC		GND	GND	GND	GND		OE5#	Q5+
F	IN-	VDDDIG		GND	GND	GND	GND		NC	Q6-
G	OE11#	NC		GND	GND	GND	GND		OE6#	Q6+
H	Q11+	VDDCLK							VDDCLK	Q7-
J	Q11-	NC	VDDCLK	OE10# SHFT_LD#	NC	OE9#	NC	OE8#	NC	Q7+
K	SBI_EN	PWRGD_ PWRDN#	NC	Q10+	Q10-	Q9+	Q9-	Q8+	Q8-	OE7#_ SBI_IN

Pin Description

Pin Number	Pin Name	Type		Description
A1	LOS#	Output	Open Drain	Open drain output, needs external pull up, Low output indicates loss of input clock signal, PDT.
A2	Q0-	Output	Diff.	Complementary clock output.
A3	Q0+	Output	Diff.	True clock output.
A4	Q1-	Output	Diff.	Complementary clock output.
A5	Q1+	Output	Diff.	True clock output.
A6	Q2-	Output	Diff.	Complementary clock output.
A7	Q2+	Output	Diff.	True clock output.
A8	Q3-	Output	Diff.	Complementary clock output.
A9	Q3+	Output	Diff.	True clock output.

Pin Number	Pin Name	Type		Description
A10	OE4#_SBI_CLK	Input	CMOS	0 = OE Mode, Enable output 4. 1 = Disable output 4. Enabled by SBI_EN Side-Band mode: SBI clock input. For both OE mode and SBI mode, Internal pull up, PDT
B1	SADR1_tri	Input	Tri-level	SMBus address bit. This is a tri-level input that works in conjunction with SADR0_TRI pin, to decode SMBus addresses. It has internal pull-up/down resistors to bias to VDD/2. See the SMBus Address Selection table.
B2	NC	NC		Not Connected
B3	OE0#	Input	CMOS	Active low input for enabling output 0. 0 = Enable output, 1 = Disable output. Internal pull up, PDT.
B4	OE1#	Input	CMOS	Active low input for enabling output 1. 0 = Enable output, 1 = Disable output. Internal pull up, PDT.
B5	VDDCLK	Power		Clock power supply.
B6	NC	NC		Not Connected
B7	OE2#_SBI_OUT	I/O	CMOS	0 = OE Mode, Enable output 2. 1 = Disable output 2. Side-Band mode: SBI shift register data output. For both OE mode and SBI mode, Internal pull up, PDT
B8	OE3#	Input	CMOS	Active low input for enabling output 3. 0 = Enable output, 1 = Disable output. Internal pull up, PDT.
B9	NC	NC		Not Connected
B10	Q4-	Output	Diff.	Complementary clock output.
C1	SADR0_tri	Input	Tri-level	SMBus address bit. This is a tri-level input that works in conjunction with SADR1_TRI pin, to decode SMBus addresses. It has internal pull-up/down resistors to bias to VDD/2. See the SMBus Address Selection table.
C2	SLEWRATE_SEL	Input	CMOS	Input to select default slew rate of the outputs. 0 = Slow Slew Rate, 1 = Fast Slew Rate. Internal pull up.
C9	VDDCLK	Power		Clock power supply.
C10	Q4+	Output	Diff.	True clock output.
D1	SCLK	Input	CMOS	Clock pin of SMBus interface.
D2	SDATA	I/O	CMOS	Data pin for SMBus interface.
D4	GND	Power		Ground pin.
D5	GND	Power		Ground pin.
D6	GND	Power		Ground pin.
D7	GND	Power		Ground pin.
D9	NC	NC		Not Connected
D10	Q5-	Output	Diff.	Complementary clock output.

Pin Number	Pin Name	Type		Description
E1	IN+	Input	Diff.	True clock input. PDT. Internal pull down.
E2	NC	NC		Not Connected
E4	GND	Power		Ground pin.
E5	GND	Power		Ground pin.
E6	GND	Power		Ground pin.
E7	GND	Power		Ground pin.
E9	OE5#	Input	CMOS	Active low input for enabling output 5. 0 = Enable output, 1 = Disable output. Internal pull up, PDT.
E10	Q5+	Output	Diff.	True clock output.
F1	IN-	Input	Diff.	Complementary clock input. Internal pull up
F2	VDDDIG	Power		Digital power.
F4	GND	Power		Ground pin.
F5	GND	Power		Ground pin.
F6	GND	Power		Ground pin.
F7	GND	Power		Ground pin.
F9	NC	NC		Not Connected
F10	Q6-	Output	Diff.	Complementary clock output.
G1	OE11#	Input	CMOS	Active low input for enabling output 11. 0 = Enable output, 1 = Disable output. Internal pull up, PDT.
G2	NC	NC		Not Connected
G4	GND	Power		Ground pin.
G5	GND	Power		Ground pin.
G6	GND	Power		Ground pin.
G7	GND	Power		Ground pin.
G9	OE6#	Input	CMOS	Active low input for enabling output 6. 0 = Enable output, 1 = Disable output. Internal pull up, PDT.
G10	Q6+	Output	Diff.	True clock output.
H1	Q11+	Output	Diff.	True clock output.
H2	VDDCLK	Power		Clock power supply.
H9	VDDCLK	Power		Clock power supply.
H10	Q7-	Output	Diff.	Complementary clock output.
J1	Q11-	Output	Diff.	Complementary clock output.
J2	NC	NC		Not Connected
J3	VDDCLK	Power		Clock power supply.

Pin Number	Pin Name	Type		Description
J4	OE10#_SHFT_LD#	Input	CMOS	Active low input for enabling output 10 or SHFTLD# pin for the Side-Band Interface. OE mode: 0 = Enable output, 1 = Disable output. Side-Band mode: 0 = Disable SBI shift register, 1 = Enable SBI shift register. For both OE mode and SBI mode, Internal pull up, PDT
J5	NC	NC		Not Connected
J6	OE9#	Input	CMOS	Active low input for enabling output 9. 0 = Enable output, 1 = Disable output. Internal pull up, PDT.
J7	NC	NC		Not Connected
J8	OE8#	Input	CMOS	Active low input for enabling output 8. 0 = Enable output, 1 = Disable output. Internal pull up, PDT.
J9	NC	NC		Not Connected
J10	Q7+	Output	Diff.	True clock output.
K1	SBI_EN	Input	CMOS	0 = SBI is disabled. Multiplexed pins function as output enables. 1 = SBI is enabled. Multiplexed pins function as SBI control pins. Internal pull down, PDT.
K2	PWRGD_PWRDN#	Input	CMOS	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. Internal Pull UP, PDT.
K3	NC	NC		Not Connected
K4	Q10+	Output	Diff.	True clock output.
K5	Q10-	Output	Diff.	Complementary clock output.
K6	Q9+	Output	Diff.	True clock output.
K7	Q9-	Output	Diff.	Complementary clock output.
K8	Q8+	Output	Diff.	True clock output.
K9	Q8-	Output	Diff.	Complementary clock output.
K10	OE7#_SBI_IN	Input	CMOS	0 = OE Mode, Enable output 7. 1 = Disable output 7. Side-Band mode: SBI shift register data input pin For both OE mode and SBI mode, Internal pull up, PDT

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature.. −65°C to +150°C
Supply Voltage to Ground Potential, V_{DDxx}.................... −0.5V to +3.9V
Input Voltage ....−0.5V to V_{DD} +0.3V, not exceed 3.9V
Input Voltage (PDT Pin) .... −0.5V to +3.9V
ESD Protection (HBM) 2000V
Iout (Output Current Continuous) 30mA
Iout (Output Current Surge)... 60mA
Junction Temperature .... 150°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Conditions

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{DDDIG}, V_{DDCLK}	Power Supply Voltage		2.97	3.3	3.63	V
I_{DD}	Power Supply Current	V_{DD} + V_{DDA}, All outputs active @100MHz		130	180	mA
I_{DD_PD}	Power Supply Power Down(1) Current	V_{DD} + V_{DDA}, All outputs LOW/ LOW		6	7.5	mA
T_A	Ambient Temperature	Industrial grade	−40		105	°C

Note:
1. Input clock is not running.
2. Outputs drive 10 inch trace.

Input Electrical Characteristics

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
R_{pu}	Internal Pull up Resistance			120		KΩ
R_{dn}	Internal Pull down Resistance			120		KΩ
L_{PIN}	Pin Inductance				7	nH

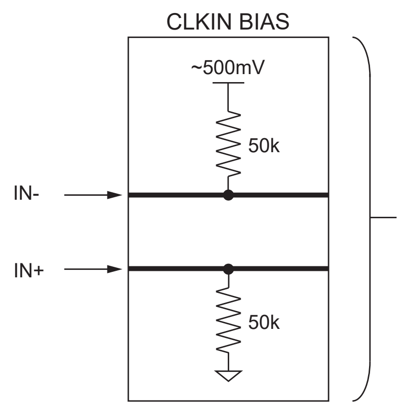


Figure 1. Input Clock Bias Network

SMBus Electrical Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{DDSMB}	Nominal Bus Voltage		2.7		3.6	V
V_{IHSMB}	SMBus Input High Voltage	SMBus, V_{DDSMB} = 3.3V	2.1		3.6	V
		SMBus, V_{DDSMB} < 3.3V	0.65 V_{DDSMB}			
V_{ILSMB}	SMBus Input Low Voltage	SMBus, V_{DDSMB} = 3.3V			0.8	V
		SMBus, V_{DDSMB} < 3.3V			0.8	
$I_{SMBSINK}$	SMBus Sink Current	SMBus, at V_{OLSMB}	4			mA
V_{OLSMB}	SMBus Output Low Voltage	SMBus, at $I_{SMBSINK}$			0.4	V
f_{MAXSMB}	SMBus Operating Frequency	Maximum frequency			400	kHz
t_{RMSB}	SMBus Rise Time	(Max V_{IL} - 0.15) to (Min V_{IH} + 0.15)			300	ns
t_{FMSB}	SMBus Fall Time	(Min V_{IH} + 0.15) to (Max V_{IL} - 0.15)			300	ns

Side-Band Interface Electrical Characteristics

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
t_{PERIOD}	Clock Period	Clock period	40			ns
t_{SETUP}	SHFT Setup Time to Clock	SHFT_LDB high to SBI_CLK rising edge	10			ns
t_{DSU}	SBI_IN Setup Time	SBI_IN setup to SBI_CLK rising edge	5			ns

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
t_{DHOLD}	SBI_IN Hold Time	SBI_IN hold after SBI_CLK rising edge	2			ns
t_{CO}	SBI_CLK to SBI_OUT	SBI_CLK rising edge to SBI_OUT valid	2			ns
t_{SHOLD}	SHFT Hold Time	SHFT_LDB hold (high) after SBI_CLK rising edge (SBI_CLK to SHFT_LDB falling edge)	10			ns
$t_{EN/DIS}$	Enable/Disable Time	Delay from SHFT_LDB falling edge to next output configuration taking effect	4		12	clocks
t_{SLEW}	Slew Rate	SBI_CLK (between 20% and 80%)	0.7		4	V/ns
		SBI_OUT impedance		50		Ω

LVCMOS DC Electrical Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	Single-ended inputs, except SMBus	0.75 VDD		VDD +0.3	V
V_{IM}	Input Mid Voltage	SADR0_TRI, SADR1_TRI	0.4VDD	0.5VDD	0.6VDD	V
V_{IL}	Input Low Voltage	Single-ended inputs, except SMBus	-0.3		0.25 VDD	V
I_{IH}	Input High Current	Single-ended inputs with pullup/ pulldown resistor, $V_{IN} = V_{DD}$			50	uA
I_{IL}	Input Low Current	Single-ended inputs with pullup/ pulldown resistor, V_{IN} = 0V	-50			μA
C_{IN}	Input Capacitance		1.5		5	pF

HCSL Input Characteristics(1)

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Frequency	V_{DD} = 3.3V	1	100	400	MHz
	Autoparking on		25			MHz
	Autoparking off		1			MHz
V_{IHDIF}	Diff. Input High Voltage (3)	IN+, IN-, single-end measurement	330		1150	mV
V_{ILDIF}	Diff. Input Low Voltage (3)	IN+, IN-, single-end measurement	-300	0	300	mV
V_{SWING}	Diff. Input Swing Voltage	Peak to peak value (V_{IHDIF} - V_{ILDIF})	200			mV
V_{COM}	Common mode voltage		100		1200	mV

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
t_{RF}	Diff. Input Slew Rate (2)		0.7			V/ns
I_{IN}	Diff. Input Leakage Current	$V_{IN+} = V_{DD}$, $V_{IN-} = 0.8V$	-40		100	uA
t_{DC}	Diff. Input Duty Cycle	Measured differentially	45		55	%
t_{jc-c}	Diff. Input Cycle to cycle jitter	Measured differentially			125	ps

Note:
1. Guaranteed by design and characterization, not 100% tested in production
2. Slew rate measured through +/-75mV window centered around differential zero
3. The device can be driven by a single-ended clock by driving the true clock and biasing the complement clock input to the Vbias, where Vbias is $(V_{IH}-V_{IL})/2$

HCSL Output Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output voltage high		660	780	900	mV
V_{OL}	Ooutput voltage low		-150	20	150	mV
Vcross absolute	Absolute Crossing point Voltage		250		550	mV
$V_{cross\ \_var}$	Crossing point voltage variation				140	mV
f_{OUT}	Output Frequency			100	400	MHz
t_{RF}	Slew rate (1,2,3)	Scope averaging on, 10 inch trace	1.5	3.0	4	V/ns
Dt_{RF}	Slew rate matching (1,2,4)	Scope averaging on, 10 inch trace			20	%
t_{SKEW}	Output Skew (1,2)	Averaging on, $V_T = 50\%$			50	ps
t_{DC}	Diff. Output Duty Cycle	Measured differentially	45		55	%
T_{pd}	Propagation Delay			2.0	3	ns
t_{OELAT}	Output Enable Latency	Q start after OE# assertion Q stop after OE# deassertion	4	5	10	clocks
t_{PDLAT}	PD# De-assertion	Differential outputs enable after PD# de-assertion		20	300	µs
$t_{LOSAssert}$	LOS Assert Time	Time from disappearance of input clock to LOS assert		50	100	ns
$t_{LOSDeassert}$	LOS De-assert Time	Time from appearance of input clock to LOS de-assert		6	9	clocks

Note:
1. Guaranteed by design and characterization, not 100% tested in production
2. Measured from differential waveform
3. Slew rate is measured through the Vswing voltage range centered around differential 0V, within +/-150mV window
4. Slew rate matching is measured through +/-75mV window centered around differential zero
5. Duty cycle distortion is the difference in duty cycle between the out and input clock

HCSL Output AC Characteristics - Phase Jitter - Normal Conditions

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Condition	Typ.	Max.	Specification Limit	Units
$t_{jphPCIeG1\text{-}CC}$	Additive PCIe Phase Jitter (Common Clocked Architecture) SSC ≤ -0.5%	PCIe Gen 1 (2.5 GT/s)	1300		86,000	fs p-p
$t_{jphPCIeG2\text{-}CC}$		PCIe Gen 2 Hi Band (5.0 GT/s)	4		3,100	fs RMS
		PCIe Gen 2 Lo Band (5.0 GT/s)	58		3,000	
$t_{jphPCIeG3\text{-}CC}$		PCIe Gen 3 (8.0 GT/s)	19		1,000	
$t_{jphPCIeG4\text{-}CC}$		PCIe Gen 4 (16.0 GT/s)	19		500	
$t_{jphPCIeG5\text{-}CC}$		PCIe Gen 5 (32.0 GT/s)	6		150	
$t_{jphPCIeG6\text{-}CC}$		PCIe Gen 6 (64.0 GT/s)	4		100	
$t_{jphPCIeG1\text{-}IR}$	Additive PCIe Phase Jitter (IR Architectures - SRIS, SRNS)SSC ≤ -0.3%	PCIe Gen 1 (2.5 GT/s)	111			fs RMS
$t_{jphPCIeG2\text{-}IR}$		PCIe Gen 2 (5.0 GT/s)	51			
$t_{jphPCIeG3\text{-}IR}$		PCIe Gen 3 (8.0 GT/s)	23			
$t_{jphPCIeG4\text{-}IR}$		PCIe Gen 4 (16.0 GT/s)	22			
$t_{jphPCIeG5\text{-}IR}$		PCIe Gen 5 (32.0 GT/s)	6			
$t_{jphPCIeG6\text{-}IR}$		PCIe Gen 6 (64.0 GT/s)	4			

Note: The Refclk jitter is measured after applying the filter functions found in the PCI Express Base Specification 6.0, Revision 1.0. For the exact measurements

SMBus Serial Data Interface

The PI6CB332012A is a slave only device that supports block and byte protocol using a single 7-bit address and read/write bit as shown below. The highest bit of register address is to distinguish block write/read. when the highest bit is "1", it's the byte operation, and when the highest bit is "0", it is the block operation.

Read and write block transfers can be stopped after any complete byte transfer.

Address Assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	See SMBus Address Selection table				1/0

Note: SMBus address is latched on SADR pin

Byte Write

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit	1 bit
Start bit	Address	W(0)	Ack	Beginning Byte location = N	Ack	data	Ack	Stop bit

Byte Read

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	1 bit	7 bits	1 bit	8 bits	1 bit	1 bit
Start bit	Address	W(0)	Ack	Beginning Byte location = N	Ack	Repeat Start bit	Address	R(1)	data	NAck	Stop bit

Block Write

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit	8 bits	1 bit		8 bits	1 bit	1 bit
Start bit	Address	W(0)	Ack	Beginning Byte Location = N	Ack	Data Byte count = X	Ack	Beginning Date Byte (N)	Ack	....	Data Byte (N+X-1)	Ack	Stop bit

Block Read

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit
Start bit	Address	W(0)	Ack	Beginning Byte Location = N	Ack	Repeat Start bit	Address	R(1)	Ack	Data Byte count = X	Ack	Beginning Date Byte (N)	Ack

	8 bits	1 bit	1 bit
....	Data Byte (N+X-1)	NAck	Stop bit

Side-Band Interface

This interface consists of DATA, CLK and SHFT_LD# pins. When the SHFT_LD# pin is high, the rising edge of CLK can shift DATA into the shift register. After shifting data, the falling edge of SHFT_LD# clocks the shift register contents to the Output register.

When the SBI is enabled, OE[2, 4, 7, 10]# are disabled and SBI_OUT DATA CLK and SHFT_LD# are enabled respectively. Additionally, SMBus registers for masking off the disable function of the shift register (0 value of a bit) become active. When set to a one, the mask register forces its respective output to 'enabled.' This prevents accidentally disabling critical outputs when using the SBI.

An SMBus read back bit in Byte 4 indicates which output enable control interface is enabled.

When the SBI is enabled, and power has been applied, the SBI is active, even if the PWRGD/PWRDN# pin indicates the part is in power down. This allows loading the shift register and transferring the contents to the output register before the assertion of PWRGD. Note that the mask registers are part of the normal SMBus interface and cannot be accessed when the PWRGD/PWRDN# is low. Figure 2 provides a functional description of the SBI.

The SBI and the traditional SMBus output enable registers both default to the 'output enabled' state at power-up. The mask registers default to zero at power-up, allowing the shift bits to disable their respective output. See Figure 2.

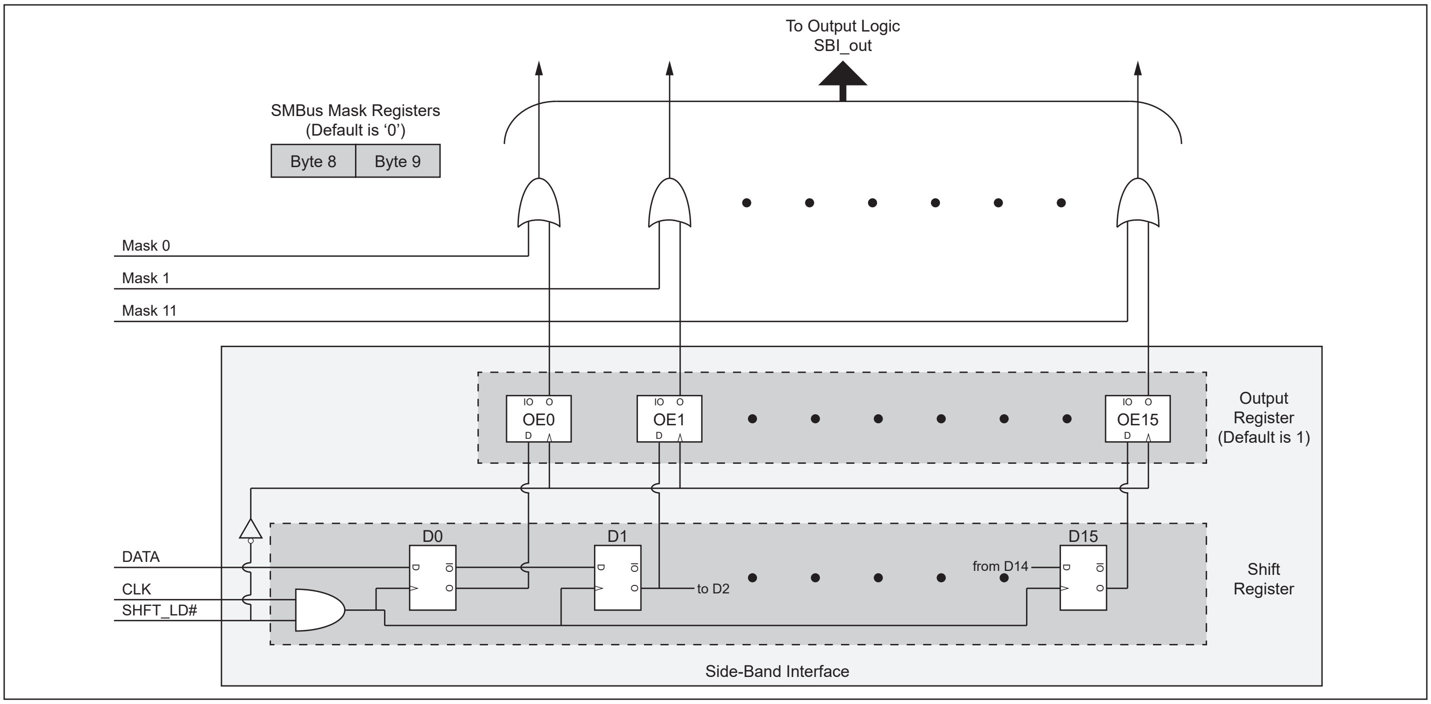


Figure 2. Side Band Interface Control Logic Description

Figures 3 shows the basic timing of the side-band interface. The SHFT_LD# pin goes high to enable the CLK input. Next, the rising edge of CLK clocks enable DATA into the shift register. After the 16th clock for output 16, stop the clock low and drive the SHFT_LD# pin low. The falling edge of SHFT_LD# clocks the shift register contents to the output register, enabling or disabling the outputs. Always shift 16 bits of data into the shift register to control the outputs. Please refer to figure 3 SBI_IN to SBI_OUT register shift order diagram.

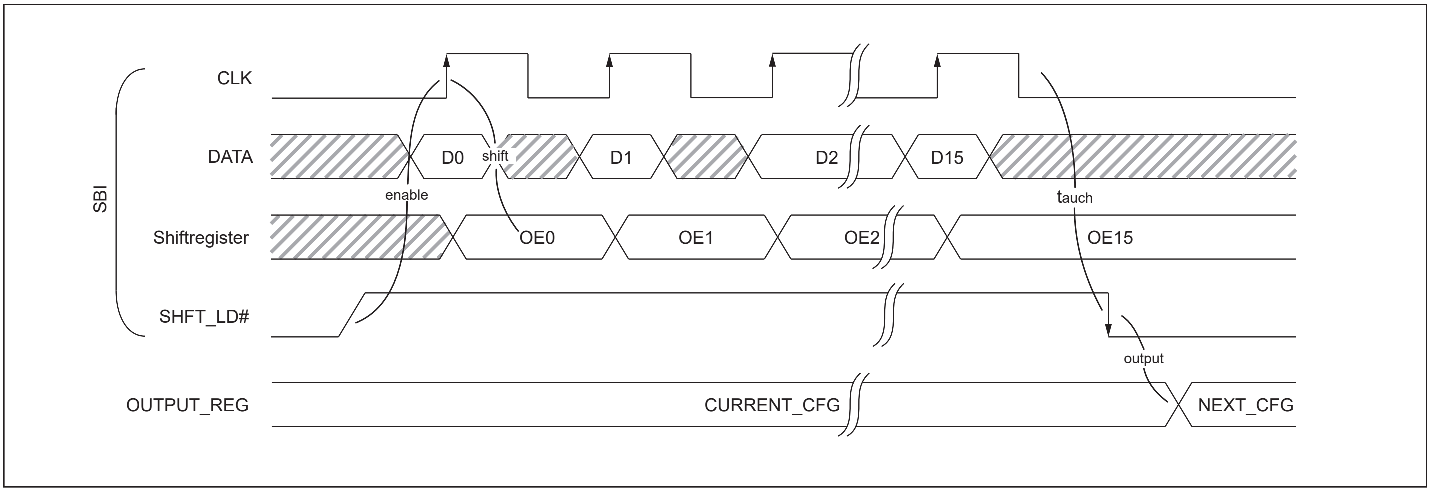


Figure 3. Side Band Interface Functional Timing

The SBI interface supports clock rates up to 10MHz. Multiple devices may share CLK and DATA pins. Dedicating a SHFT_LD# pin to each devices allows its use as a chip-select pin. When the SHFT_LD# pin is low, the PI6CB3320xx ignores any activity on the CLK and DATA pins.

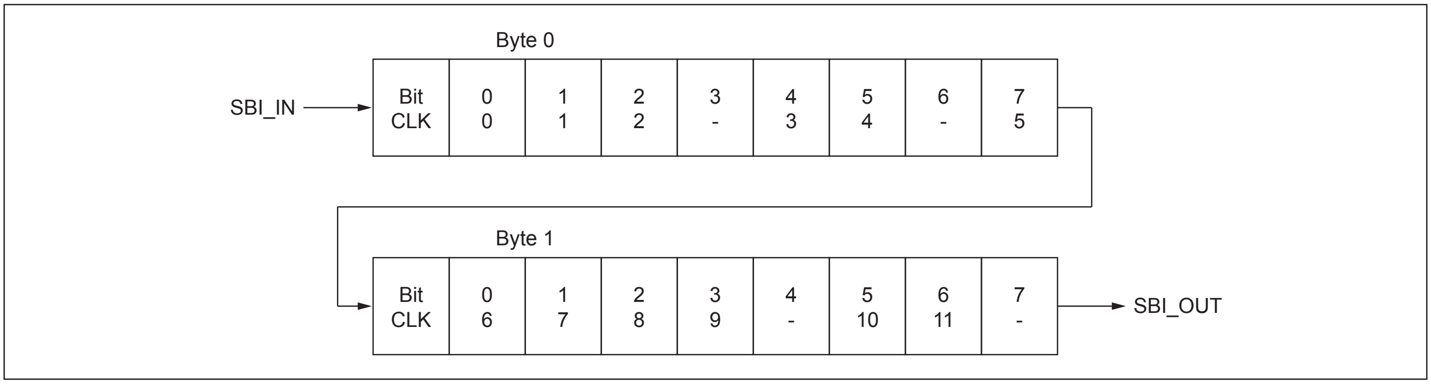


Figure 4. SBI_IN to SBI_OUt Shift Order Diagram

SMBus Address Decode

Address Selection		Binary Value								Hex Value
SADR_tri1	SADR_tri0	7	6	5	4	3	2	1	Read/Write	
0	0	1	1	0	1	1	0	0	0	D8
	M	1	1	0	1	1	0	1	0	DA
	1	1	1	0	1	1	1	1	0	DE
M	0	1	1	0	0	0	0	1	0	C2
	M	1	1	0	0	0	1	0	0	C4
	1	1	1	0	0	0	1	1	0	C6
1	0	1	1	0	0	1	0	1	0	CA
	M	1	1	0	0	1	1	0	0	CC
	1	1	1	0	0	1	1	1	0	CE

SMBus Registers

Byte 0: OUTPUT_ENABLE_0

Bit	Control Function	Description	Type	Power Up Condition	Definition
7	Q5_En	Output Enable for Q5	RW	1	0 = output is disabled 1 = output is enabled
6	Reserved		RW	1	
5	Q4_En	Output Enable for Q4	RW	1	
4	Q3_En	Output Enable for Q3	RW	1	
3	Reserved		RW	1	
2	Q2_En	Output Enable for Q2	RW	1	
1	Q1_En	Output Enable for Q1	RW	1	
0	Q0_En	Output Enable for Q0	RW	1	

Byte 1: OUTPUT_ENABLE_1

Bit	Control Function	Description	Type	Power Up Condition	Definition
7	Reserved		RW	1	0 = output is disabled 1 = output is enabled
6	Q11_EN	Output Enable for Q11	RW	1	
5	Q10_EN	Output Enable for Q10	RW	1	
4	Reserved		RW	1	
3	Q9_EN	Output Enable for Q9	RW	1	
2	Q8_EN	Output Enable for Q8	RW	1	
1	Q7_EN	Output Enable for Q7	RW	1	
0	Q6_EN	Output Enable for Q6	RW	1	

Byte 2: OE_PIN_READBACK_0

Bit	Control Function	Description	Type	Power Up Condition	Definition
7	RB_OE#_5	Status of OE#5	RO	Pin	0 = OE# pin low 1 = OE# pin high
6	Reserved		RO	1	
5	RB_OE#_4	Status of OE#4	RO	Pin	
4	RB_OE#_3	Status of OE#3	RO	Pin	
3	Reserved		RO	1	
2	RB_OE#_2	Status of OE#2	RO	Pin	
1	RB_OE#_1	Status of OE#1	RO	Pin	
0	RB_OE#_0	Status of OE#0	RO	Pin	

Byte 3: OE_PIN_READBACK_1					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	Reserved		RO	1	0 = OE# pin low 1 = OE# pin high
6	RB_OE#_11	Status of OE#11	RO	Pin	
5	RB_OE#_10	Status of OE#10	RO	Pin	
4	Reserved		RO	1	
3	RB_OE#_9	Status of OE#9	RO	Pin	
2	RB_OE#_8	Status of OE#8	RO	Pin	
1	RB_OE#_7	Status of OE#7	RO	Pin	
0	RB_OE#_6	Status of OE#6	RO	Pin	

Byte 4: SBEN_RDBK_ ACP_CONFIG					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	Reserved		RW	1	
6			RW	1	
5			RW	1	
4	ACP_Enable	Enable automatic clock parking to Low/Low when LOS event is detected	RW	1	0 = Disable ACP 1 = Enable ACP
3	Reserved		RW	1	
2			RW	1	
1			RW	0	
0	RB_SBI_ENQ	Status of SBI_ENQ	RO	Pin	0 = pin low 1 = pin high

Byte 5: VENDOR_REVISION_ID					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	RID	REVISION ID, A rev is 0000	RO	0000	
6			RO		
5			RO		
4			RO		
3	VID	VENDOR ID, Diodes	RO	0011	
2			RO		
1			RO		
0			RO		

Byte 6: DEVICE_ID					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	DEVICE_ID	Device ID	RO	PI6CB332012A (85Ω) 0H50	
6			RO		
5			RO		
4			RO		
3			RO		
2			RO		
1			RO		
0			RO		

Byte 7: BYTE_COUNT					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	Reserved		RW	1'b000	
6			RW		
5			RW		
4	BC	Writing to this register configures how many bytes will be read back in a block read.	RW	0x7	
3			RW		
2			RW		
1			RW		
0			RW		

Byte 8: SBI_MASK_0					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	MASK5	Masks off Side-band Disable for Q5	RW	0	0 = SBI may disable the output 1 = SBI cannot disable the output
6	Reserved		RW	0	
5	MASK4	Masks off Side-band Disable for Q4	RW	0	
4	MASK3	Masks off Side-band Disable for Q3	RW	0	
3	Reserved		RW	0	
2	MASK2	Masks off Side-band Disable for Q2	RW	0	
1	MASK1	Masks off Side-band Disable for Q1	RW	0	
0	MASK0	Masks off Side-band Disable for Q0	RW	0	

Byte 9: SBI_MASK_1					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	Reserved		RW	0	0 = SBI may disable the output 1 = SBI cannot disable the output
6	MASK11	Masks off Side-band Disable for Q11	RW	0	
5	MASK10	Masks off Side-band Disable for Q10	RW	0	
4	Reserved		RW	0	
3	MASK9	Masks off Side-band Disable for Q9	RW	0	
2	MASK8	Masks off Side-band Disable for Q8	RW	0	
1	MASK7	Masks off Side-band Disable for Q7	RW	0	
0	MASK6	Masks off Side-band Disable for Q6	RW	0	

Byte 10: RESERVED

Byte 11: SBI_READBACK_0[1]					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	SBI_Q5	Readback of Side-band Disable for Q5	RO	X	0 = bit low 1 = bit high
6	Reserved		RO	1	
5	SBI_Q4	Readback of Side-band Disable for Q4	RO	X	
4	SBI_Q3	Readback of Side-band Disable for Q3	RO	X	
3	Reserved		RO	1	
2	SBI_Q2	Readback of Side-band Disable for Q2	RO	X	
1	SBI_Q1	Readback of Side-band Disable for Q1	RO	X	
0	SBI_Q0	Readback of Side-band Disable for Q0	RO	X	

Byte 12: SBI_READBACK_1[1]					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	Reserved		RO	1	0 = bit low 1 = bit high
6	SBI_Q11	Readback of Side-band Disable for Q11	RO	X	
5	SBI_Q10	Readback of Side-band Disable for Q10	RO	X	
4	Reserved		RO	1	
3	SBI_Q9	Readback of Side-band Disable for Q9	RO	X	
2	SBI_Q8	Readback of Side-band Disable for Q8	RO	X	
1	SBI_Q7	Readback of Side-band Disable for Q7	RO	X	
0	SBI_Q6	Readback of Side-band Disable for Q6	RO	X	

Byte 13-16: RESERVED

Byte 17: LPHCSL_AMP_CTRL					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	AMP	Global Differential output Control 0.625V~1V 25mV/step Default = 0.8V	RW	0x7	
6			RW		
5			RW		
4			RW		
3	Reserved		RW	1'b0000	
2			RW		
1			RW		
0			RW		

Byte 18: POWERDOWN_RESTORE_LOS#					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	AC_IN	Enable receiver bias when IN is AC coupled	RW	0	0 = DC coupled input 1 = AC coupled input
6	Rx_TERM	Enable termination resistors on IN	RW	0	0 = input termination R is disabled 1 = input termination R is enabled
5	Reserved		RW	0	
4	Reserved		RW	0	
3	PD_RESTORE#	Save Configuration in Power Down	RW	1	0 = Config Cleared 1 = Config Saved
2	Reserved		RW	1	
1	Reserved		RW	0	
0	LOS#_RB	Real time read back of loss detect block output	RO	X	0 = LOS event detected 1 = NO LOS event detected.

Byte 19: RESERVED

Byte 20: OUTPUT_SLEW_ RATE_0					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	Q5_SLEWRATE	Q5 Slewrate Control	RW	pin status	0 = low slew rate 1 = high slew rate
6	Reserved		RW	pin status	
5	Q4_SLEWRATE	Q4 Slewrate Control	RW	pin status	
4	Q3_SLEWRATE	Q3 Slewrate Control	RW	pin status	
3	Reserved		RW	pin status	
2	Q2_SLEWRATE	Q2 Slewrate Control	RW	pin status	
1	Q1_SLEWRATE	Q1 Slewrate Control	RW	pin status	
0	Q0_SLEWRATE	Q0 Slewrate Control	RW	pin status	

Byte 21: OUTPUT_SLEW_ RATE_1					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	Reserved		RW	Pin status	0 = low slew rate 1 = high slew rate
6	Q11_SLEWRATE	Q11 Slewrate Control	RW	Pin status	
5	Q10_SLEWRATE	Q10 Slewrate Control	RW	Pin status	
4	Reserved		RW	pin status	
3	Q9_SLEWRATE	Q9 Slewrate Control	RW	Pin status	
2	Q8_SLEWRATE	Q6 Slewrate Control	RW	Pin status	
1	Q7_SLEWRATE	Q7 Slewrate Control	RW	Pin status	
0	Q6_SLEWRATE	Q6 Slewrate Control	RW	Pin status	

Byte 22-37 : RESERVED (Default: 0xXX)

Byte 38: WRITE_LOCK_NOCLEAR					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	Reserved		RW	1'b0000000	
6			RW		
5			RW		
4			RW		
3			RW		
2			RW		
1			RW		
0	WRITE_LOCK	Non-clearable SMBus Write Lock bit. When written to one, the SMBus control registers cannot be written to. This bit can only be cleared by cycling power.	RW	0	0 = SMBus not locked for writing by this bit. See WRITE_LOCK_RW1C bit. 1 = SMBus locked for writing

Byte 39: WRITE_LOCK_CLEAR_ LOS_EVENT					
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**Definition**
7	Reserved		RW1C	1'b000000	
6			RW1C		
5			RW1C		
4			RW1C		
3			RW1C		
2			RW1C		
1	LOS_EVT	LOS Event Status When high, indicates that a LOS event was detected. Can be cleared by writing a 1 to it.	RW1C	0	0 = No LOS event detected 1 = LOS event detected.
0	WRITE_LOCK_ RW1C	Clearable SMBus Write Lock bit. When written to one, the SMBus control registers cannot be written to. This bit can be cleared by writing a 1 to it.	RW1C	0	0 = SMBus not locked for writing by this bit. See WRITE_ LOCK bit. 1 = SMBus locked for writing

Applications Information

Power Down Tolerant Pins

Pins that are Power Down Tolerant (PDT) can be driven by voltages as high as the normal VDD of the chip, even though VDD is not present (the device is not powered). There will be no ill effects to the device and it will power up normally. This feature supports disaggregation, where the PI6CB3320xx may be on one circuit board and devices that interface with it are on other boards. These boards may power up at different times, driving pins on the PI6CB3320xx before it has received power.

Flexible Startup Sequencing

PI6CB3320xx devices support Flexible Startup Sequencing (FSS), IN+/- pins are PDT. FSS allows application of CLKIN at different times in the device/system startup sequence. FSS is an additional feature that helps the system designer manage the impact of disaggregation. Table shows the supported sequences; that is, the PI6CB3320xx devices can have CLKIN running before VDD is applied, and can have VDD applied and sit for extended periods with no input clock.

Loss of Signal and Automatic Clock Parking

The PI6CB3320xx buffers have a Loss of Signal (LOS) circuit to detect the presence or absence of an input clock. The LOS circuit drives the open-drain LOS# pin (the “#” suffix indicates “bar”, or active-low) and sets the LOS_EVT bit in the SMBus register space. There are two slightly different LOS# pin behaviors at power up. Figure 5 shows the LOS# de-assertion timing for 12-output and 24-output buffers.

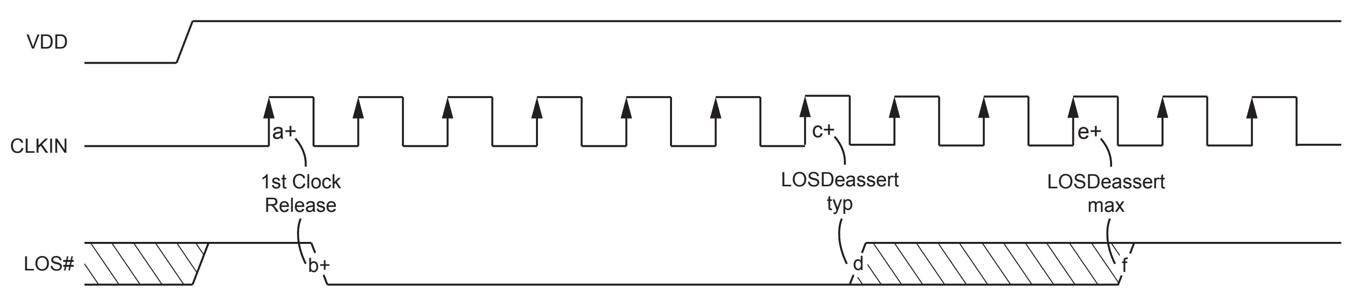


Figure 5. LOS# De-assert Timing

Note: The LOS circuit on the 12-output buffer requires a CLKIN edge to release the LOS# pin after power up. So, the LOS# pin will be high until the first clock edge after power up.

The following diagram shows the LOS# assertion sequence when the CLKIN is lost. It also shows the Automatic Clock Parking (ACP) circuit bring the inputs to a Low/Low state after an LOS event. For exact timing, see Electrical Characteristics.

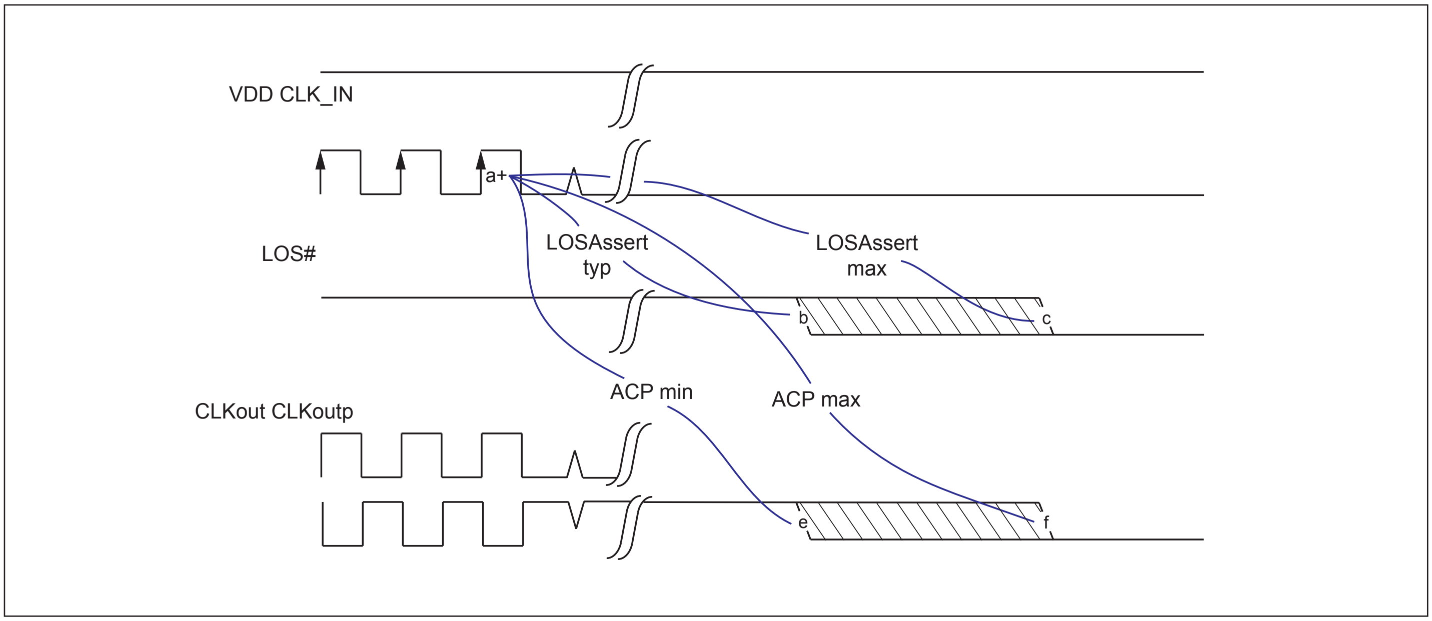


Figure 6. LOS# Assert Timing

Test Load

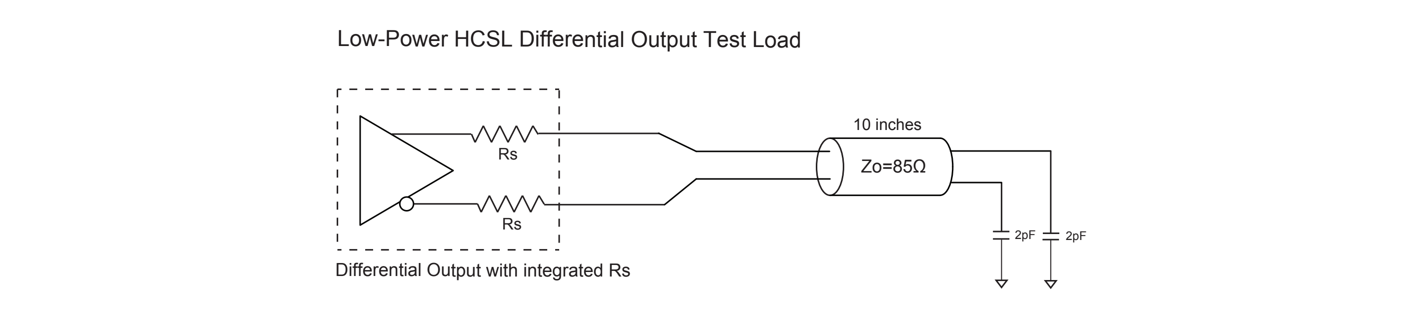


Figure 7. Low Power HCSL Test Circuit

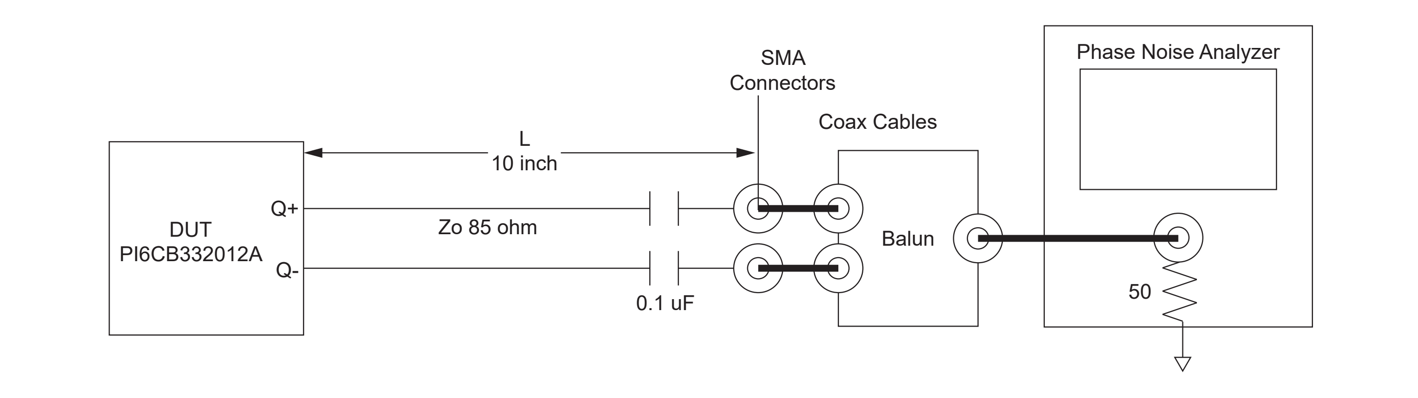


Figure 8. Test Set Up for Phase Jitter Measurement

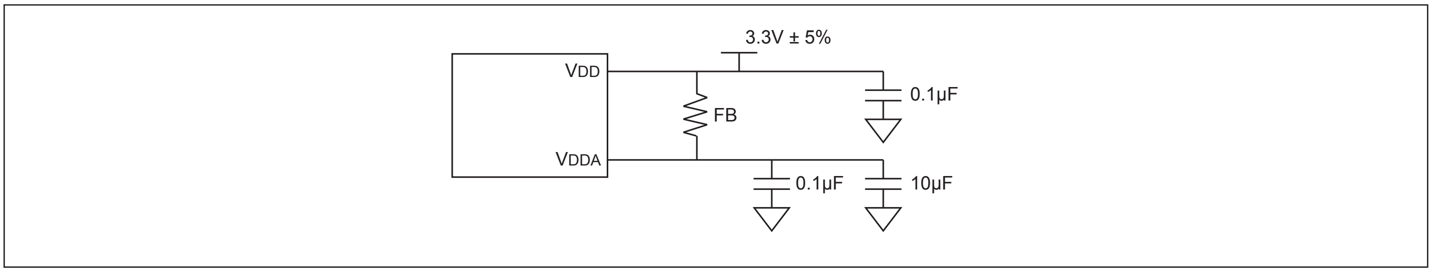
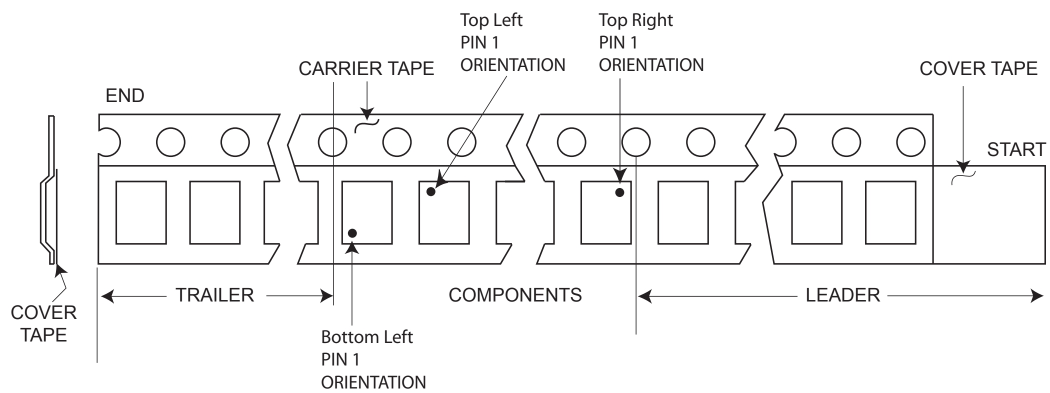


Figure 9. Power Supply Filter

Part Marking

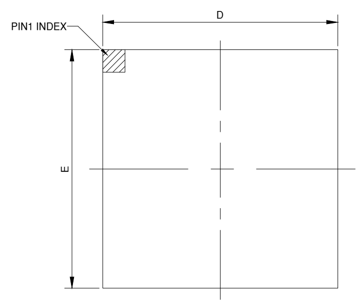
Z: Die Rev
YY: Date Code (Year)
WW: Date Code (Workweek)
1st X: Assembly Site Code
2nd X: Fab Site Code

Package Information

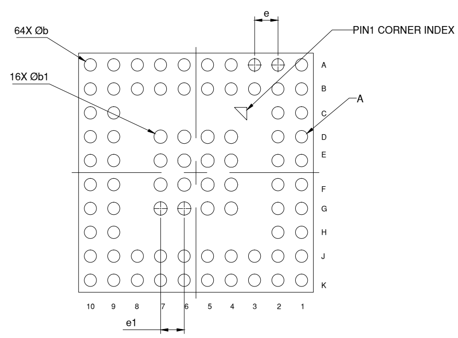


Packaging Mechanical

64-WLGA (FLB)

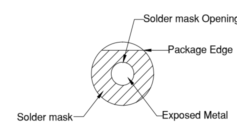


TOP VIEW

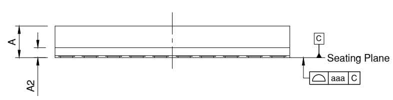


BOTTOM VIEW

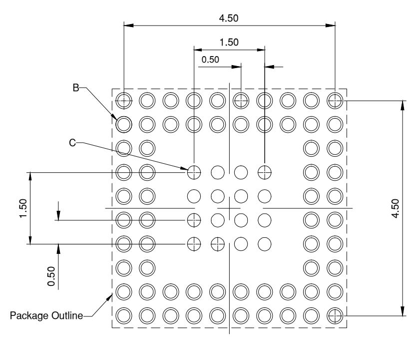
PKG. DIMENSIONS(MM)			
SYMBOL	Min	NOM	Max
A	0.56	0.66	0.76
A2		0.21REF	
D	4.90	5.00	5.10
E	4.90	5.00	5.10
e		0.50 BSC	
e1		0.50 BSC	
b		0.26 BSC	
b1		0.28 BSC	
aaa		0.08 BSC	



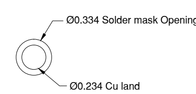
Detail A



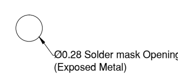
SIDE VIEW



Recommend Land Pattern
（PCB TOP VIEW）



Detail B
(64 Peripheral Pads, NSMD)



Detail C
(16 Center Pads, SMD)

Notes:
1. All dimensions are in mm.
3. Use ±0.05mm for non-toleranced dimensions.

DIODES INCORPORATED / PERICOM ENABLING SERIAL CONNECTIVITY	DATE: 01/12/24
DESCRIPTION: W-LGA5050-64	
PACKAGE CODE: FLB(FLB64)	
DOCUMENT CONTROL#: PD-2289	REVISION:--

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Orderable Part Number	Package Code	Package Description	Pin 1 Orientation	Temperature
PI6CB332012AFLBEX	FLB	64-Contact, 5x5mm (W-LGA5050-64)	Top Right Corner	–40~105°C
PI6CB332012AFLBEX-13R	FLB	64-Contact, 5x5mm (W-LGA5050-64)	Top Left Corner	–40~105°C

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. A = For 85Ω output impedance
5. E = Pb-free and Green
6. X suffix = Tape/Reel
7. For packaging detail, go to our website at: https://www.diodes.com/assets/MediaList-Attachments/Diodes-Package-Information.pdf

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