

**PI6LC4872-01**

**HiFlex™ High Performance Ethernet & Fibre Channel (FC) Clock Generator**

**Features**

- Ethernet and Fibre Channel clock outputs
- Supporting and LVPECL outputs
- Pin selectable output frequencies
- Ultra low phase jitter: < 1ps (156.25MHz, 12KHz to 20MHz integration range)
- 25MHz low noise buffered output
- 33MHz PCI clock
- Selectable reference or Xtal input
- 3.3V supply voltage
- TQFN-40 package

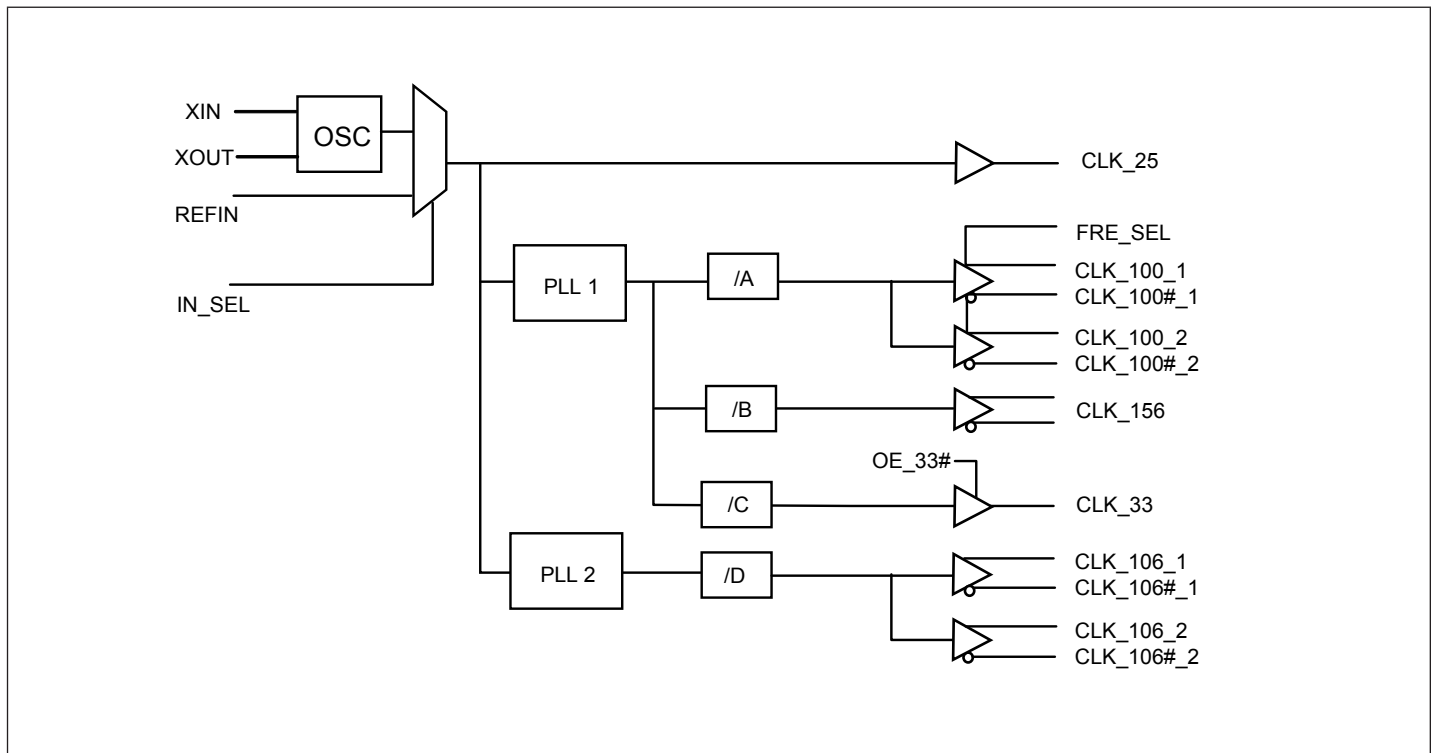
**Description**

The PI6LC4872-01 is high performance clock generator which supports both Ethernet frequencies and Fibre Channel (FC) frequencies. Diodes Incorporated's proprietary PLL technology used in this device generates all these frequencies in the single chip while maintaining ultra low phase jitter. This device is ideal for systems that need both Ethernet and FC clock providing great flexibility.

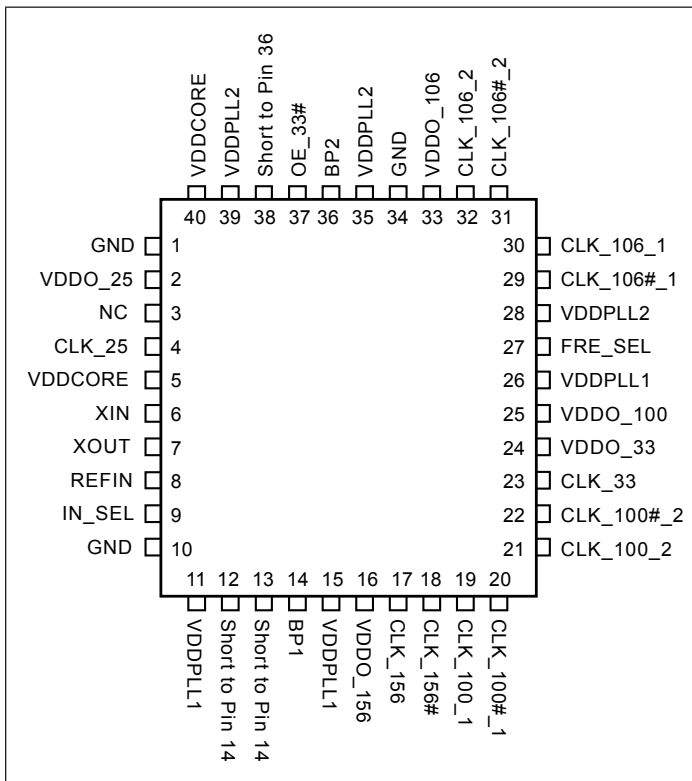
**Applications**

- Switches and Routers with FC interface
- Storage systems

**Block Diagram**



### Pin Configuration



### Pinout Table

Pin Number	Pin Name	Description
1, 10, 34	GND	Ground. Includes external paddle (EPAD).
2	VDDO_25	Power Supply Connection for the 25M CMOS Buffer.
3	NC	No Connect. This pin should be left floating.
4	CLK_25	CMOS 25 MHz Output.
5	VDDCORE	Power Supply Connection for the Crystal Oscillator.
6, 7	XIN, XOUT	External 25 MHz Crystal.
8	REFIN	25 MHz Reference Clock Input. Tie low when not in use.
9	IN_SEL	Logic Input. Used to select the reference source.
11	VDDPLL1	Power Supply Connection for the GbE PLL.
14, 36	BP1, BP2	These pins are for bypassing each LDO to ground with a 220 nF capacitor.
15	VDDPLL1	Power Supply Connection for the GbE VCO.
16	VDDO_156	Power Supply Connection for the 156M LVPECL Output Buffer and Output Dividers.
17	CLK_156	LVPECL Output at 156.25 MHz.
18	CLK_156#	Complementary LVPECL Output at 156.25 MHz.
19	CLK_100_1	LVPECL Output at 100 MHz or 125 MHz. Selected by FRE_SEL pin strapping.
20	CLK_100#_1	Complementary LVPECL/ Output at 100 MHz or 125 MHz.

**Pinout Table** (continued from previous page)

Pin No.	Pin Name	Description
21	CLK_100_2	LVPECL Output at 100 MHz or 125 MHz. Selected by FRE_SEL pin strapping.
22	CLK_100#_2	Complementary LVPECL Output at 100 MHz or 125 MHz.
23	CLK_33	CMOS 33.33 MHz Output.
24	VDDO_33	Power Supply Connection for the 33M CMOS Output Buffer and Output Dividers.
25	VDDO_100	Power Supply Connection for the 100M/125M LVPECL Output Buffer and Output Dividers.
26	VDDPLL1	Power Supply Connection for the GbE PLL Feedback Divider.
27	FRE_SEL	Logic Input. Used to configure output drivers.
28	VDDPLL2	Power Supply Connection for the FC PLL Feedback Divider.
29	CLK_106#_1	Complementary LVPECL Output at 106.25 MHz.
30	CLK_106_1	LVPECL Output at 106.25 MHz.
31	CLK_106#_2	Complementary LVPECL Output at 106.25 MHz.
32	CLK_106_2	LVPECL Output at 106.25 MHz.
33	VDDO_106	Power Supply Connection for the 106.25 MHz LVPECL Output Buffer and Output Dividers.
35	VDDPLL2	Power Supply Connection for the FC VCO.
37	OE_33#	Forces the 33.33 MHz output into a low state.
39	VDDPLL2	Power Supply Connection for the FC PLL.
40	VDDCORE	Power Supply Connection for Miscellaneous Logic.

**Function Tables**

**INSEL Definition**

IN_SEL	Input
0	External reference clock
1 or NC	External Xtal

**FRE\_SEL Definition**

FRE_SEL	Pin 19 and pin 20	Pin 21 and pin 22
0	125 MHz	125 MHz
1	100 MHz	100 MHz
NC	125 MHz	100 MHz

**OE\_33# Definition**

OE_33#	CLK_33
0 or NC	33.33MHz
1	Low

**Maximum Ratings** (Above which the useful life may be impaired. For user guidelines, not tested)

Storage temperature.....	-65°C to +155°C
Ambient Operating Temperature.....	-40°C to +85°C
3.3V Supply Voltage.....	-0.5 to +4.6V
Storage Temperature, T <sub>STG</sub> .....	-65°C to 150°C
ESD Protection (HBM).....	2000V
Junction Temperature .....	125 °C max

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. [This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Recommended Operating Conditions**

Symbol	Description	Test Conditions	Min	Type	Max	Unit
V <sub>DD</sub>	Power supply	-	3.0	-	3.6	V
I <sub>DD</sub>	Total Power Supply Current	All output frequencies.	-	-	400	mA
T <sub>A</sub>	Operating temperature	-	-40		+85	°C

**LVC MOS DC Electrical Characteristics** (Over Operating Conditions)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>IH</sub>	Input High Voltage	IN_SEL, OE_33#, and REFIN	2	-	V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage	IN_SEL, OE_33#, and REFIN	-0.3	-	0.8	V
V <sub>IH</sub>	Input High Voltage	FRE_SEL	2/3V <sub>DD</sub> +0.2	-		V
V <sub>IL</sub>	Input Low Voltage	FRE_SEL		-	1/3V <sub>DD</sub> -0.2	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -1mA	V <sub>DD</sub> -0.1	-	-	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 1mA	-	-	0.1	V
I <sub>IH</sub>	Input High Current	V <sub>IN</sub> = V <sub>DD</sub> , IN_SEL	-	-	1.0	μA
		V <sub>IN</sub> = V <sub>DD</sub> , FRE_SEL			45	
		V <sub>IN</sub> = V <sub>DD</sub> , OE_33#			240	
I <sub>IL</sub>	Input Low Current	V <sub>IN</sub> = 0V, IN_SEL	-155	-		μA
		V <sub>IN</sub> = 0V, FRE_SEL	-30			
		V <sub>IN</sub> = 0V, OE_33#	-3.0			

**LVCMOS DC Electrical Characteristics** (Over Operating Conditions) Continued..

R <sub>PU</sub>	Internal pull up resistance	IN_SEL	-	30		KΩ
		FRE_SEL		150		
R <sub>DN</sub>	Internal pull down resistance	OE_33#	-	16	-	KΩ
		FRE_SEL		100		

**LVPECL DC Electrical Characteristics** (Over Operating Conditions) - For PI6LC4872-01 only

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>OH</sub>	Output High Voltage	-	V <sub>DD</sub> -1.24	-	V <sub>DD</sub> -0.83	V
V <sub>OL</sub>	Output Low Voltage	-	V <sub>DD</sub> -2.07	-	V <sub>DD</sub> -1.62	V
V <sub>OD</sub>	Output differential voltage	-	700	-	950	mV

**AC Switching Characteristics** (Over Operating Conditions), Typical is given for V<sub>DD</sub>=3.3V, T<sub>A</sub>=25C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F <sub>in</sub>	Input Frequency	-		25		MHz
T <sub>OE</sub>	Output enable time				100	ns
T <sub>OEB</sub>	Output disable time				100	ns
T <sub>r</sub> / T <sub>f</sub>	Output Rise/Fall time	Termination =200Ohm to 0V; C <sub>L</sub> =0pf; 20% to 80% measured dif- ferentially		600	880	ps
O <sub>DC</sub>	Output Duty Cycle		49		51	%
J <sub>phase</sub>	Phase jitter (12kHz to 20MHz), RMS	Output frequency: 156.25MHz, output combination=1x156.25MHz, 1x100MHz, 1x125MHz, 2x106.25MHz	-	510	700	fs
		Output frequency: 125MHz, out- put combination=1x156.25MHz, 1x100MHz, 1x125MHz, 2x106.25MHz, 33MHz off	-	560	700	
		Output frequency: 125MHz, out- put combination=1x156.25MHz, 1x100MHz, 1x125MHz, 2x106.25MHz, 33MHz on	-	600	700	
		Output frequency: 106.25MHz, output combination=1x156.25MHz, 1x100MHz, 1x125MHz, 2x106.25MHz	-	530	700	
		Output frequency: 100MHz, out- put combination=1x156.25MHz, 1x100MHz, 1x125MHz, 2x106.25MHz		600	700	

**PI6LC4872-01**

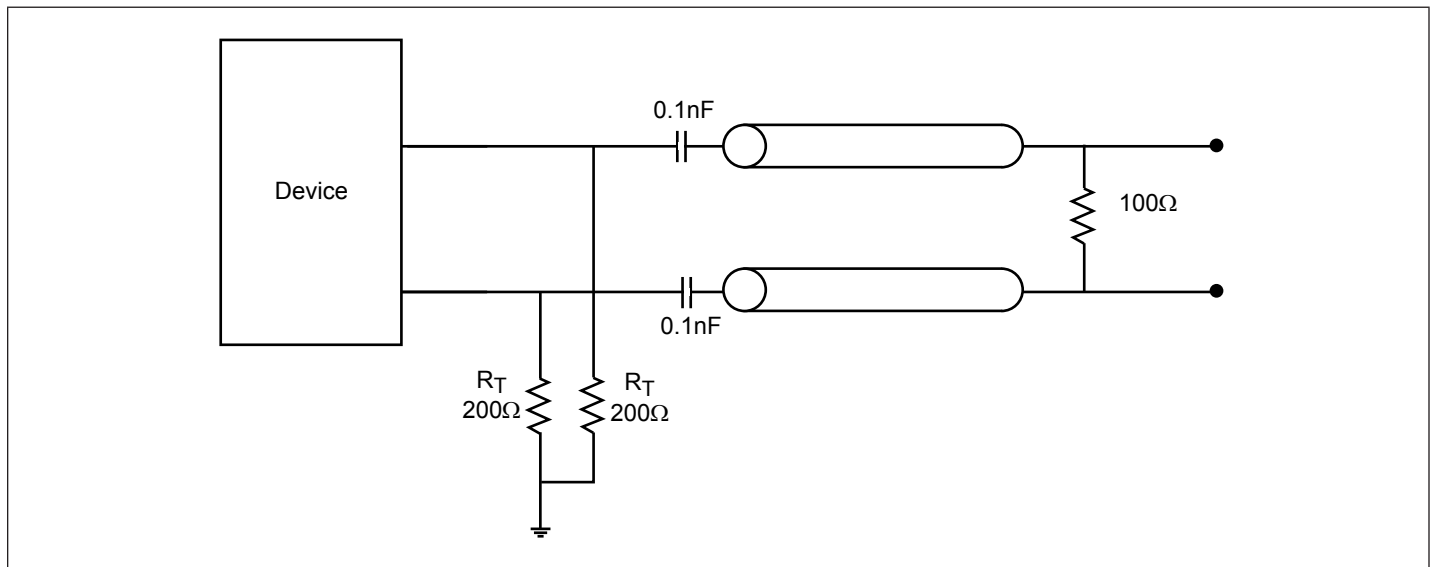
**CMOS AC Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T <sub>r</sub> /T <sub>f</sub>	Output Rise/Fall time	Termination =50Ohm to 0V; CL=5pf; 20% to 80%	250	500	2500	ps
O <sub>DC</sub>	Output Duty Cycle		48		52	%
J <sub>phase</sub>	Phase jitter (12kHz to 5MHz), RMS	Output frequency: 25MHz, out- put combination=1x156.25MHz, 1x100MHz, 1x125MHz, 2x106.25MHz	-	200	-	fs
		Output frequency: 33MHz, out- put combination=1x156.25MHz, 1x100MHz, 1x125MHz, 2x106.25MHz	-	505	-	

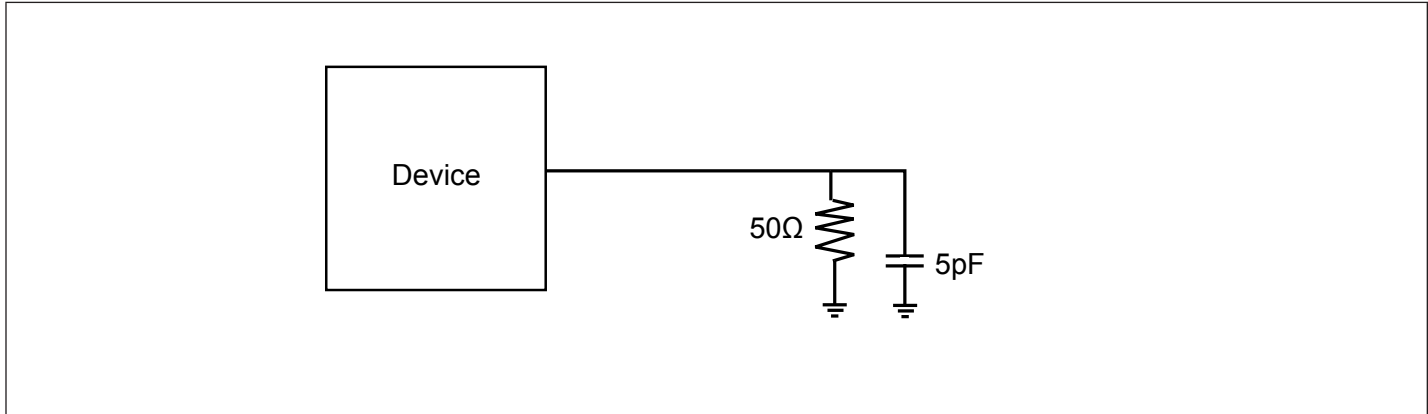
**PI6LC4872-01**

**Crystal Specification**

Parameter	Conditions	Min.	Typ.	Max.	Unit
Frequency	Fundamental mode		25		MHz
ESR				50	$\Omega$
Load capacitance			14		pF
Stability		-30		30	ppm
Phase noise	@ 1kHz offset		-135		dBc/Hz



**Figure 1. Configuration Test Load Board Termination for LVPECL Output**



**Figure 2. Configuration Test Load Board Termination for LVCMOS output**

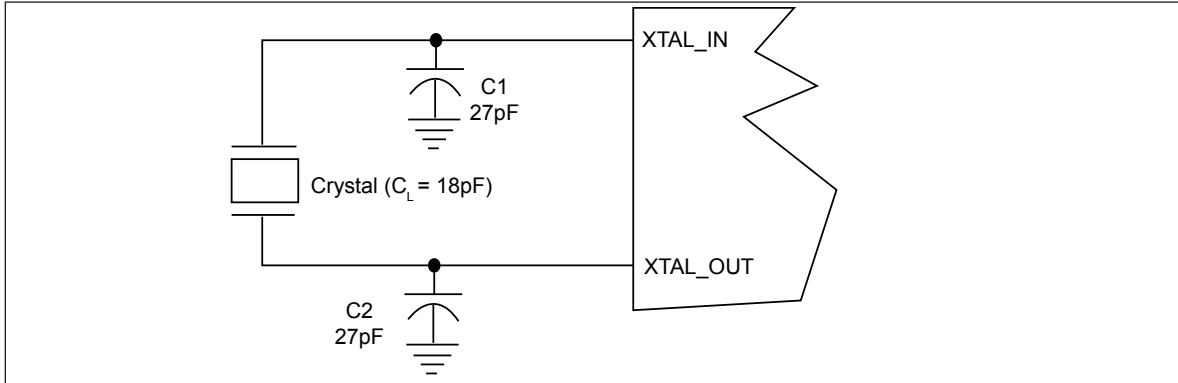


## Application Notes

### Crystal circuit connection

The following diagram shows PI6LC4872-01 crystal circuit connection with a parallel crystal. For the  $C_L=18\text{pF}$  crystal, it is suggested to use  $C1=27\text{pF}$ ,  $C2=27\text{pF}$ .  $C1$  and  $C2$  can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts.

### Crystal Oscillator Circuit

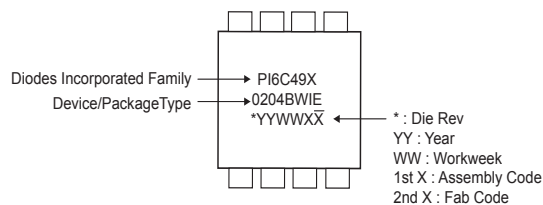


### Recommended Crystal Specification

Pericom recommends:

- a) GC2500003 XTAL 49S/SMD(4.0 mm), 25M,  $CL=18\text{pF}$ ,  $\pm 30\text{ppm}$ , [http://www.pericom.com/pdf/datasheets/se/GC\\_GF.pdf](http://www.pericom.com/pdf/datasheets/se/GC_GF.pdf)
- b) FY2500081, SMD 5x3.2(4P), 25M,  $CL=18\text{pF}$ ,  $\pm 30\text{ppm}$ , [http://www.pericom.com/pdf/datasheets/se/FY\\_F9.pdf](http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf)
- c) FL2500047, SMD 3.2x2.5(4P), 25M,  $CL=18\text{pF}$ ,  $\pm 20\text{ppm}$ , <http://www.pericom.com/pdf/datasheets/se/FL.pdf>

## Part Marking

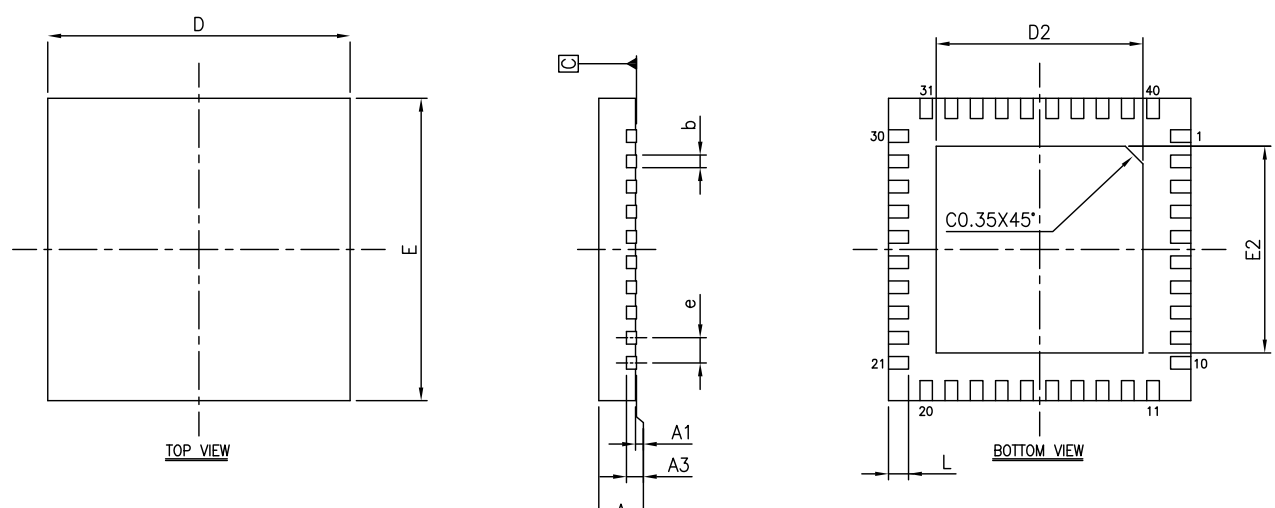


**Note:**

1. For latest datecode info, please check: <https://www.diodes.com/assets/MediaList-Attachments/Pericom-Datecode-Format-Explanation.pdf>

**PI6LC4872-01**

**Packaging Mechanical: 40-Pin QFN (ZD)**



SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.18	0.25	0.30
D	5.90	6.00	6.10
E	5.90	6.00	6.10
e	0.50 BSC		
L	0.35	0.40	0.45
D2	4.40	4.50	4.55
E2	4.40	4.50	4.55

**Notes:**  
 1. All dimensions are in mm.  
 2. Refer JEDEC MO-220.  
 3. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.

**PERICOM**<sup>®</sup>  
Enabling Serial Connectivity

DATE: 07/12/11

DESCRIPTION: 40-contact, Thin Fine Pitch Quad Flat No-Lead, TQFN

PACKAGE CODE: ZD (ZD40)

DOCUMENT CONTROL #: PD-2021

REVISION: C

11-0148

**Ordering Information**

Ordering Code	Package Code	Package Type	Operating Temperature
PI6LC4872-01ZDIEX	ZD	Pb-free & Green, 40-pin QFN	Industrial

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