PERICOM®

PI6UMC10802

Ultra Mobility, Clipped Sinewave, Clock Buffer with 2 Outputs

Features

- Dual Analog Voltage Clipped Sinewave Buffer
- Distributes Two Outputs
- 19.2 MHz to 52 MHz Operation Frequency Range
- Low Power Consumption:
- Typical off ct - <0.2µA
- Typical on current - 0.75mA (one output enabled) @ 26MHz
- Typical on ct - 2.1mA (both outputs enabled) @ 26MHz
- Variable Input Voltage - 0.3V - 1.5V
- Fixed Output Voltage - 1.5V @26MHz
- Low Output Harmonic Level
- 2nd Harmonic -50dBc max
- 3rd Harmonic -15dBc max
- 4th Harmonic -50dBc max
- 5th Harmonic -20dBc max
- Low Phase Noise Output
- Over –70dB reverse isolation between output and input
- Power supply: 1.8V ±5%
- Temperature Range
- -30°C to +85°C extended commercial temp range
- Packaging (Pb-free & Green):
- 10-pin UQFN 1.8 ×1.4 × 0.55 mm (ZM10)

Description

The PI6UMC10802 is a small footprint, low power, clipped sinewave buffer with 2 outputs designed to address mobile clock distribution applications and offers cost savings over using multiple TCXOs.

The PI6UMC10802 features analog voltage buffer with variable input (0.3V-1.5V) and fixed output voltage (1.5V @26MHz).

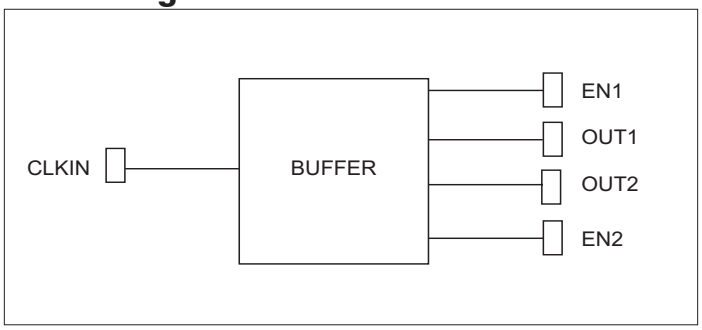
The PI6UMC10802 operates at 1.8V ± 5% and guaranteed over the extended commercial temperature range of -30°C to +85°C.

The buffer provides low harmonic output with very low additive phase noise. There is negligible power consumption in standby mode. EN1 and EN2 signals enable the respective OUT1, OUT2 buffers.

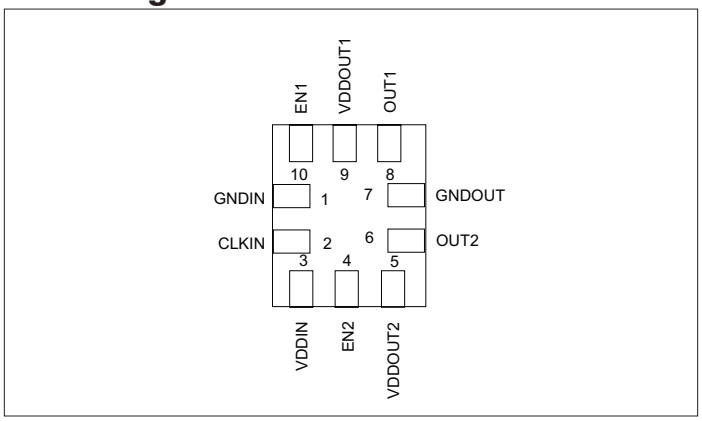
Applications

- Smart phone Clock Reference for RF & Peripheral
- Multimode RF clock reference

Block Diagram



Pin Configuration



Pin Description

Pin	Signal	Description
2	CLKIN	Reference clock input
8, 6	OUT1, OUT2	Clipped Sinewave, Clock outputs with weak pull-down
1	GNDIN	Input Ground
9, 5	VDDOUT1, VDDOUT2	Output Power - 1.8V
10, 4	EN1, EN2	Output Enable for OUT1, OUT 2. Active HIGH. Output is in logic LOW state when the corresponding EN1 or EN2 is LOW (see Truth Table). EN1 = 0 and EN2 = 0 is chip standby mode
7	GNDOUT	Output Ground
3	VDDIN	Input Stage Power - 1.8V

Maximum Ratings(1)

Supply Voltage
V_{DDOUT1}, V_{DDOUT2} ..... -0.5V to +2.5V
Input Current ..... -50mA
Output Current ..... ±50mA
Lead Temperature (soldering, 10 sec.) ..... +260°C
Storage Temperature (Ts)..... -65°C to +150°C
Junction Temperature..... +150°C
ESD Protection ..... 2000V min (HBM)

Operation Ratings(2)

Supply Voltage
V_{DDOUT1}, V_{DDOUT2} ..... 1.8V ± 5%
Ambient Temperature (T_A) ..... -30°C to +85°C

Notes:

1. Stresses greater then those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. θJ_A and ΨJ_B values are determined for a 4-layer board in still-air, unless otherwise stated.

Output Truth Table

EN1	EN2	OUT1	OUT2
0	0	Low	Low
0	1	Low	Enabled
1	0	Enabled	Low
1	1	Enabled	Enabled

DC Electrical Characteristics (V_{DDOUT1}, V_{DDOUT2} = 1.8V ± 5%, T_A=-30°C to 85°C, R_L = 10kΩ, C_L = 10pF, unless otherwise stated.)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
I_{DD}[1]	Supply Current @ 19.2MHz	EN1 = 0, EN2 = 0		0.2	1	µA
		EN1 = 1, EN2 = 0 or EN1 = 0, EN2 = 1		0.55	0.75	mA
		EN1 = 1, EN2 = 1		1.6	2	
I_{DD}[1]	Supply Current @ 26MHz	EN1 = 0, EN2 = 0		0.2	1	µA
		EN1 = 1, EN2 = 0 or EN1 = 0, EN2 = 1		0.75	1	mA
		EN1 = 1, EN2 = 1		2.1	2.5	
I_{DD}[1]	Supply Current @ 38.4MHz	EN1 = 0, EN2 = 0		0.2	1	µA
		EN1 = 1, EN2 = 0 or EN1 = 0, EN2 = 1		1.2	1.5	mA
		EN1 = 1, EN2 = 1		3	3.5	
V_{IH}	EN1, EN2 Input HIGH Voltage		0.65*V_{DD}		1.95	V
V_{IL}	EN1, EN2 Input LOW Voltage		-0.3		0.35*V_{DD}	

Note:

1. No Load.

AC Electrical Characteristics (V_{DDOUT1}, V_{DDOUT2} = 1.8V ± 5%, T_A=-30°C to 85°C, R_L = 10kΩ, C_L = 10pF, unless otherwise stated.)

Parameter	Description	Test Conditions		Min.	Typ.	Max.	Units
F_O	Output frequency	PI6UMC10802-1		19.2		52	MHz
P_N	OUT1, OUT2 Phase Noise degradation	Load as in Fig. 1	1KHz Offset		0	1	dBc/Hz
			100KHz Offset		0	1	
V_{IN}	Input Voltage			0.3		1.5	V
P_H[(1)]	OUT1, OUT2 Harmonic Level	Load as in Fig. 1 @ 19.2MHz I/P duty cycle 50%	2nd Harmonic			-50	dBc
			3rd Harmonic			-15	
			4nd Harmonic			-50	
			5th Harmonic			-20	
P_H [(1)]	OUT1, OUT2 Harmonic Level	Load as in Fig. 1 @ 26MHz I/P duty cycle 50%	2nd Harmonic			-50	dBc
			3rd Harmonic			-15	
			4nd Harmonic			-50	
			5th Harmonic			-20	
P_H [(1)]	OUT1, OUT2 Harmonic Level	Load as in Fig. 1 @ 38.4MHz I/P duty cycle 50%	2nd Harmonic			-50	dBc
			3rd Harmonic			-15	
			4nd Harmonic			-50	
			5th Harmonic			-20	

Continued

Parameter	Description	Test Conditions		Min.	Typ.	Max.	Units
P_H (1)	OUT1, OUT2 Harmonic Level	Load as in Fig. 1 @ 52MHz I/P duty cycle 50%	2nd Harmonic			-40	dBc
			3rd Harmonic			-16	
			4nd Harmonic			-36	
			5th Harmonic			-25	
V_{pp}	Peak-to-Peak output voltage	V_{DD} = 1.8V ± 3%	@19.2MHz	1.56		1.73	V
			@26MHz	1.49		1.63	
			@38.4MHz	1.26		1.40	
			@52MHz	1.03		1.37	
		V_{DD} = 1.8V ± 5%	@19.2MHz	1.53		1.76	
			@26MHz	1.46		1.66	
			@38.4MHz	1.23		1.43	
			@52MHz	1.0		1.40	
P_R	Reverse Isolation	OUT1, OUT2 to CLKIN		70			dB

Note:

1. Harmonics levels are for stated load conditions.

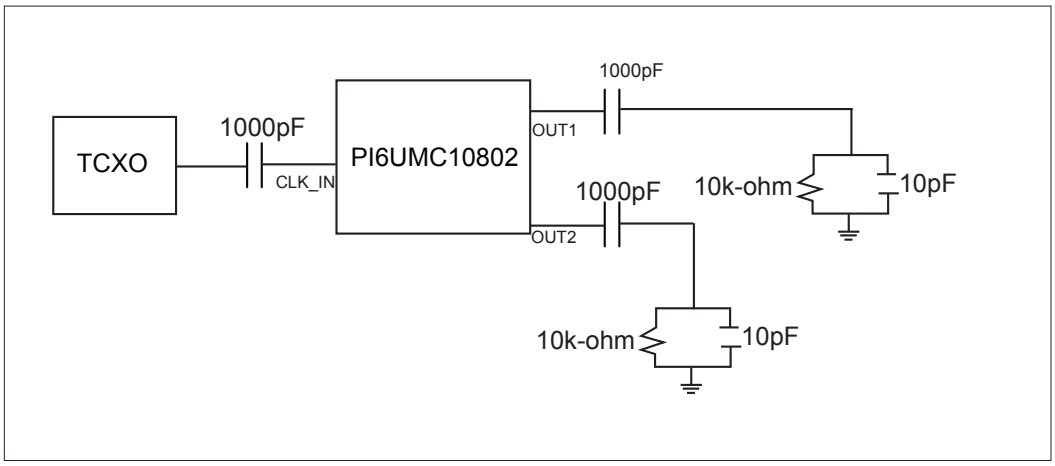


Figure 1. Test Condition

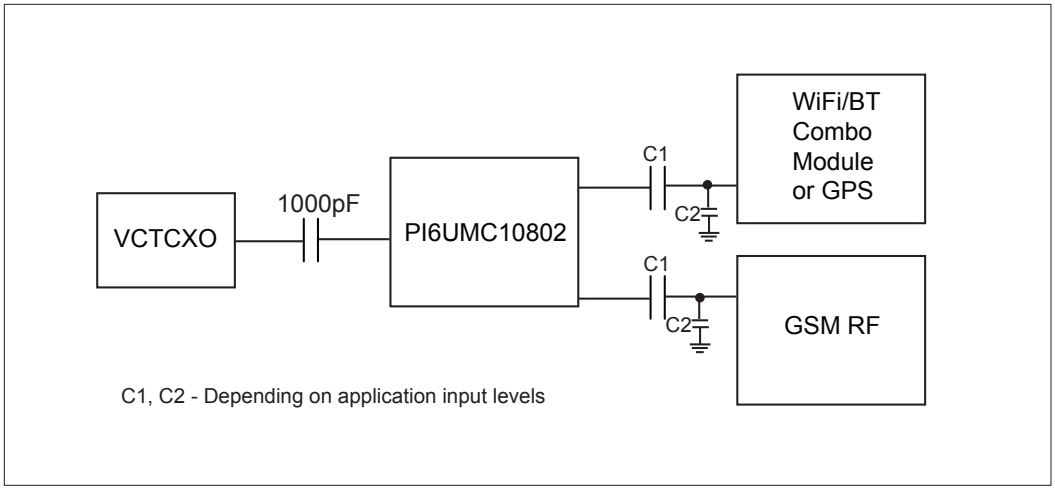
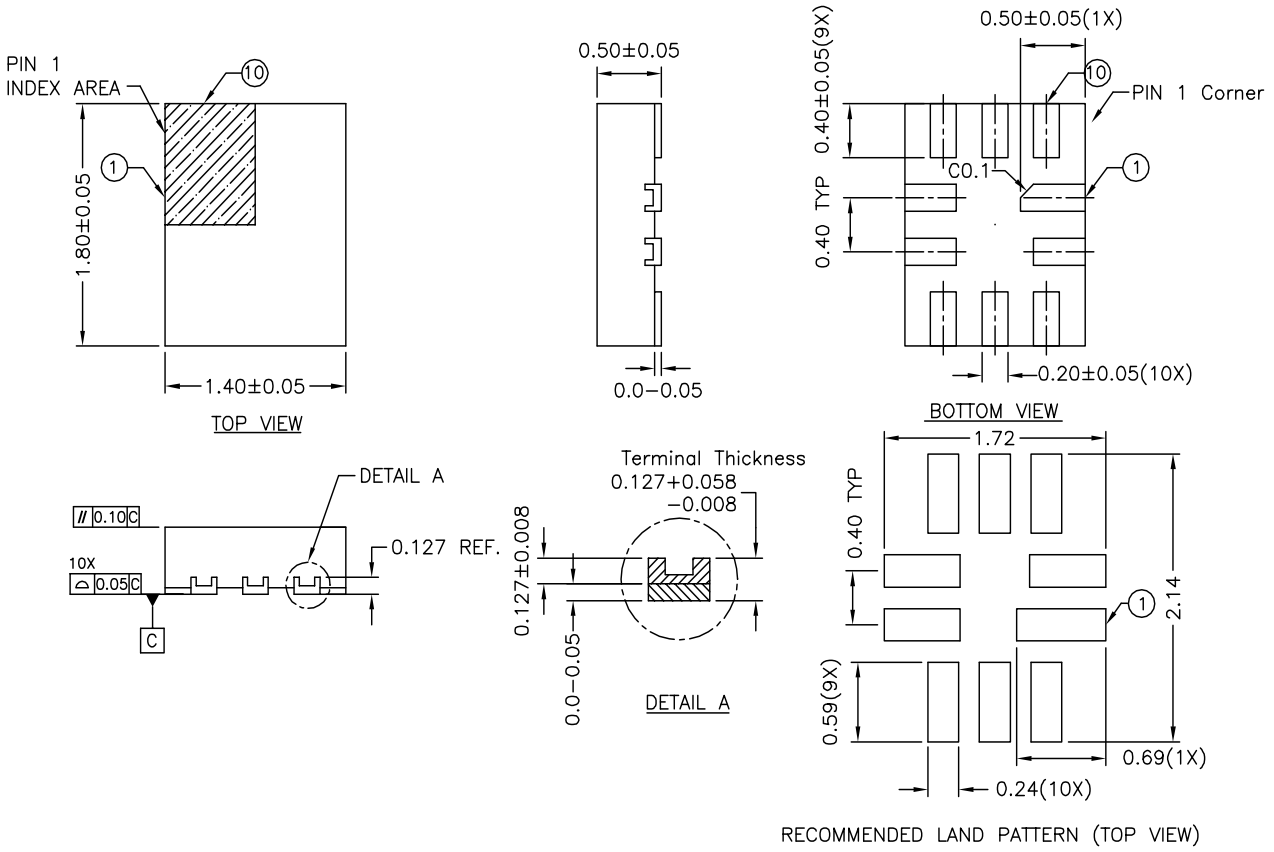


Figure 2. Application in Smart Phone

Application Guide:

Please make sure a low noise supply is used to ensure output phase noise is minimized. We recommend use of an "analog" +1.8V supply which powers only low noise/low power circuits. All the V_{DD} pins are tied to a common 1µF ceramic decoupling capacitor to ground. The decoupling capacitor should be placed close to V_{DDIN} pin. Digital supplies are not recommended. V_{DD} routing for the decoupling capacitor should be done directly to the chip on the top PCB layer without any vias.

Package Mechanical: 10-pin UQFN (ZM10)



NOTE :

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO−236/MO−248
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.

PERICOM Semiconductor Corporation

DATE: 01/29/09

DESCRIPTION: 10-contact, Ultra-thin Quad Flat No-Lead (UQFN)

PACKAGE CODE: ZM10

DOCUMENT CONTROL #: PD-2066 **REVISION: A**

09-0072

Ordering Information(1-3)

Ordering Code	Package Code	Package Type
PI6UMC10802-1ZME	ZM	Pb-free & Green, 10-pin UQFN

Notes:

1. Thermal characteristics can be found on the company website at http://www.pericom.com/packaging/
2. E = Pb−free and Green
3. X Suffix = Tape & Reel