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PCI EXPRESS GEN 2 PACKET SWITCH 3/4/5/6/11/12-Port/ 24-Lane PCI Express Gen 2 Switch ***DATASHEET***

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A Product Line of
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REVISION HISTORY

| Date | Revision Number | Description |
|------------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 08/28/2015 | 0.1 | Preliminary Datasheet (Short-Form) |
| 01/07/2016 | 0.2 | Preliminary Datasheet |
| 02/25/2016 | 0.3 | Added Section 11 Power Sequence |
| 11/04/2016 | 0.4 | Update Section 3.3 Hot Plug Signals Updated Section 3.7 Power Pins Updated Section 4.1 K10 Pin Updated Figure 6-2 Intelligent Adaptor Architecture Added Section 6.15 Hot Plug Support Updated Section 6.15 Hot Plug Support Updated Section 8.2.88 Hot Plug Configuration Register Updated Section 8.2.152 Transaction Layer CSR Register Removed Section 8.2.182 Clock Buffer Control Register Removed Section 8.2.183 Clock Buffer Port Select Register Updated Section 8.3.88 Hot Plug Configuration Register Updated Section 8.3.117 Transaction Layer CSR Register Removed Section 8.3.161 Clock Buffer Control Register Removed Section 8.3.162 Clock Buffer Port Select Register Added Section 8.6 DMA Engine Interface Registers Updated Section 11 Power Sequence Updated Section 13.2 DC Specifications Updated datasheet template |
| 10/16/2017 | 1 | Updated Section 1 Features Updated Section 3 Pin Description Updated Section 7 EEPROM Interface And System Management/I2C Bus Updated Section 8 Register Description Updated Section 13 Electrical and Timing Specifications Added Section 14 Thermal Data Updated Section 16 Ordering Information Revision numbering system changed to whole number |
| 11/07/2017 | 2 | Updated Section 3.7 Power Pins (106 Balls) |
| 01/23/2018 | 3 | Updated 16 Ordering Information Updated Section 7.1 7.1 EEPROM Interface Updated Section 8.2.117 PHY Parameter 2 Register Updated Section 8.2.118 PHY Parameter 3 Register Updated Section 8.2.136 Port MISC 0 Register Updated Table 13-8 Power Consumption Updated Section 16 Ordering Information Added Figure 15-2 Part Marking |
| 05/15/2019 | 4 | Updated Section 1 Features Updated Section 7 EEPROM Interface And I2c Bus Updated Section 8.2.114 Switch Operation Mode Register – Offset 850h (Upstream Port Only) Updated Section 3.1 PCI Express Interface Signals (125 Balls) |
| 05/14/2020 | 5 | Updated Section 1 Features Updated Section 3.2 Port Specific Signals (17 Balls) Updated Section 3.5 Miscellaneous Signals (29 Balls) Updated Section 6.1 PHYSICAL LAYER CIRCUIT Updated Section 8.2.53 Link Control Register 2 Updated Section 8.2.126 EEPROM CONTROL REGISTER Added Section 7.2 SMBUS Interface |
| 12/15/20 | 6 | For Datasheet Status Change |
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| | | Updated Section 8.3.48 NT PORT LINK INTERFACE BAR 4-5 CONFIGURATION REGISTER – OFFSET F4h Updated Table 9-1 AC Switching and DC Electrical Characteristics for REFCLKI_P/N and REFCLKO_P/N[8:1] Updated Table 9-2 AC Switching and DC Electrical Characteristics for REFCLKP/N Updated Section 14 THERMAL DATA Updated Section 2 General Description Removed Section 6.12 Access Control Service Updated Section 8.2.138 PORT MISC 1 REGISTER – OFFSET 8B4h Updated Section 3.5 MISCELLANEOUS SIGNALS (29 BALLS) |

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1 FEATURES

- 24-lane PCI Express® Gen 2 Switch with 12 PCI Express ports
- Supports “Cut-through”(Default) as well as “Store and Forward” mode for packet switching
- 150 ns typical latency for packet routed through Switch without blocking
- Integrated reference clock for downstream ports
- Supports internal Direct Memory Access (DMA) engine to move data between two address locations
- Supports Transparent and Non-Transparent Modes
- Strapped pins configurable with optional EEPROM or I2C Bus
- I2C Slave interface support
- Compliant with I2C Bus Specification, Version 2.1
- Compliant with *PCI Express Base Specification Revision 2.1*
- Compliant with *PCI Express CEM Specification Revision 2.0*
- Compliant with *PCI-to-PCI Bridge Architecture Specification Revision 1.2*
- Compliant with *Advanced Configuration Power Interface (ACPI) Specification*
- Reliability, Availability and Serviceability
 - Supports Data Poisoning and End-to-End CRC
 - Advanced Error Reporting and Logging
- Advanced Power Saving
 - Empty downstream ports are set to idle state to minimize power consumption
- Link Power Management
 - Supports L0, L0s, L1, L2, L2/L3_{Ready} and L3 link power states
 - Active state power management for L0s and L1 states
- Device State Power Management
 - Supports D0, D3_{Hot} and D3_{Cold} device power states
- Port Arbitration: Round Robin (RR), Weighted RR and Time-based Weighted RR
- Extended Virtual Channel capability
 - Two Virtual Channels (VC) and Eight Traffic Class (TC) support
 - Disabled VCs’ buffer is assigned to enabled VCs for resource sharing
 - Independent TC/VC mapping for each port
 - Provides VC arbitration selections: Strict Priority, Round Robin (RR) and Programmable Weighted RR
- Supports Isochronous Traffic
 - Isochronous traffic class mapped to VC1 only
 - Strict time based credit policing
- Supports up to 512-byte maximum payload size
- Programmable driver current and de-emphasis level at each individual port
- Support Access Control Service (ACS) for peer-to-peer traffic
- Support Address Translation (AT) packet for SR-IOV application
- Support Alternative Routing ID Interpretation (ARI)
- Support Multicast
- Support Serial Hot Plug Controller
- Low Power Dissipation: 2.1 W typical in L0 normal mode (Including clock buffer Pd)
- Industrial Temperature Range -40° to 85°C
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. “Green” Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](#) or your local Diodes representative.
<https://www.diodes.com/quality/product-definitions/>
- 324-pin HSBGA 19mm x 19mm package (ULA)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, “Green” and Lead-free.
3. Halogen- and Antimony-free “Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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2 GENERAL DESCRIPTION

Similar to the role of PCI/PCIX Bridge in PCI/PCIX bus architecture, the function of PCI Express (PCIE) Switch is to expand the connectivity to allow more end devices to be reached by host controllers in PCIE serial interconnect architecture. The 24-lane PCIe Switch is in 12-port type configuration. It provides users the flexibility to expand or fan-out the PCI Express lanes based on their application needs.

In the PCI Express Architecture, the PCIe Switch forwards posted and non-posted requests, and completion packets in either downstream or upstream direction concurrently as if a virtual PCI Bridge is in operation on each port. By visualizing the port as a virtual Bridge, the Switch can be logically viewed as two-level cascaded multiple virtual PCI-to-PCI Bridges, where one upstream-port Bridge sits on all downstream-port Bridges. Similar to a PCI Bridge during enumeration, each port is given a unique bus number, device number, and function number by the initiating software. The bus number, device number, and function number are combined to form a destination ID for each specific port. In addition to that, the memory-map and IO address ranges are exclusively allocated to each port as well. After the software enumeration is finished, the packets are routed to the dedicated port based on the embedded address or destination ID. To ensure the packet integrity during forwarding, the Switch is not allowed to split the packets to multiple small packets or merge the received packets into a large transmit packet. Also, the IDs of the requesters and completers are kept unchanged along the path between ingress and egress port.

The Switch employs the architecture of Combined Input and Output Queue (CIOQ) in implementation. The main reason for choosing CIOQ is that the required memory bandwidth of input queue equals to the bandwidth of ingress port rather than increasing proportionally with port numbers as an output queue Switch does. The CIOQ at each ingress port contains separate dedicated queues to store packets. The packets are arbitrated to the egress port based on the PCIe transaction-ordering rule. For the packets without ordering information, they are permitted to pass over each other in case that the addressed egress port is available to accept them. As to the packets required to follow the ordering rule, the Head-Of-Line (HOL) issue becomes unavoidable for packets destined to different egress ports since the operation of producer-consumer model has to be retained; otherwise the system might occur hang-up problem. On the other hand, the Switch places replay buffer at each egress port to defer the packets before sending it out. This can assure the maximum throughput being achieved and therefore the Switch works efficiently. Another advantage of implementing CIOQ in PCIe Switch is that the credit announcement to the counterpart is simplified and streamlined because of the credit-based flow control protocol. The protocol requires that each ingress port maintains the credits independently without checking other ports' credit availability, which is otherwise required by pure output queue architecture.

The Switch supports two virtual channels (VC0, VC1) and eight traffic classes (TC0 ~ TC7) at each port. The ingress port independently assigns packets into the preferred virtual channel while the egress port outputs the packet based on the predefined port and VC arbitration algorithm. For instance, the isochronous packet is given a special traffic class number other than TC0 and mapped into VC1 accordingly. By employing the strict time based credit policy for port arbitration and assigning higher priority to VC1 than VC0, the Switch can therefore guarantee the time-sensitive packet is not blocked by regular traffic to assure the quality of service. In addition, some data-centric applications only carry TC0/VC0 traffic. As a result, there are no packets that would consume VC1 bandwidth. In order to improve the efficiency of buffer usage, the unused VC1 queues can be reassigned to VC0 and enable each of the ingress ports to handle more data traffic bursts. This virtual channel resource relocation feature enhances the performance of the PCIe Switch further.

The built-in Integrated Reference Clock Buffer of the PCI Express Switch supports seven reference clock outputs. The clock buffer is from a single 100MHz clock input, and distributes the clock source to seven outputs, which can be used by the PCI Express Switch and the downstream PCI Express end devices. The clock buffer feature can be enabled and disabled by EEPROM or I2C.

The DIODES™ PI7C9X2G1224GP supports various types of power management ranged from device state, link state to platform-wise power saving mechanism. For device state, the D0, D1, D2, D3-hot, and D3-cold power states represent different amount of power dissipation in PI7C9X2G1224GP. As to link state, each link of the PI7C9X2G1224GP supports the PCI Express Link Power Management with L0, L0s, L1, L2/L3 ready and L2/L3 power states.

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Non-Transparent (NT) Bridging is supported by the packet switch. The NT bridge allows two separate Hosts to be connected together. One single port of the packet switch can be configured to operate in NT mode. While the port is in NT mode, the packet switch allows the isolation of address spaces, and the packet switch acts as an endpoint to the Host to allow inter-processor communication. NT mode is enabled and disabled by toggling the NT_EN_L strapping pin.

The packet switch supports internal Direct Memory Access (DMA) functionality to move data between two address locations. Two types of DMA engines are supported: DMA_UP and DMA_NT. The upstream port uses DMA_UP engine to move data in Host processor address domain. And the non-transparent port uses DMA_NT to move inter-processor data. The DMA engines have two built-in data channels: channel 0 and channel 1. The packet switch also provides a flexibility to manage these DMA engines. If the NT port is not enabled, all of the DMA engines would be allocated to upstream port domain.

3 PIN DESCRIPTION

3.1 PCI EXPRESS INTERFACE SIGNALS (125 BALLS)

| NAME | PIN | TYPE | DESCRIPTION |
|----------------------|---------------------------------------------------------------------------------------------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| REFCLKP REFCLKN | U8 V8 | I | Reference Clock Input Pairs: Connect to 100MHz differential clock. The input clock signals must be delivered to the clock buffer cell through an AC-coupled interface so that only the AC information of the clock is received, converted, and buffered. It is recommended that a 0.1uF be used in the AC-coupling. |
| PERP[23:0] | E4,E5,E6,E7,E9,E10,E11,E12, E14,F14,G14,H14,K14,L14,M14, N14, P12,P11,P10,P9,P7,P6,P5,P4 | I | PCI Express Data Serial Input Pairs: Differential data receive signals in sixteen ports. |
| PERN[23:0] | D4,D5,D6,D7,D9,D10,D11,D12, E15,F15,G15,H15,K15,L15,M15, N15,R12,R11,R10,R9,R7,R6,R5, R4 | I | Please refer to Section 5 for Mapping of the Lanes to transmission and receive pairs and configuration of Port-Lane. |
| PETP[23:0] | B4,B5,B6,B7,B9,B10,B11,B12, E17,F17,G17,H17,K17,L17,M17, N17,U12,U11,U10,U9,U7,U6,U5, U4 | O | PCI Express Data Serial Output Pairs: Differential data transmit signals in sixteen ports. |
| PETN[23:0] | A4,A5,A6,A7,A9,A10,A11,A12, E18,F18,G18,H18,K18,L18,M18, N18,V12,V11,V10,V9,V7,V6,V5, V4 | O | Please refer to Section 5 for Mapping of the Lanes to transmission and receive pairs and configuration of Port-Lane. |
| PERST_L | U1 | I | System Reset (Active LOW): When PERST_L is asserted, the internal states of whole chip except sticky logics are initialized. Please refer to Table 11-2 for PERST_L Spec. |
| REXT[2:0] | D8,J15,R8 | I | External Reference Resistor: Connect an external resistor (1.43K Ohm +/- 1%) to REXT_GND to provide a reference to both the bias currents and impedance calibration circuitry. |
| REXT_GND[2:0] | E8,J14,P8 | I | External Reference Resistor Ground: Connect to an external resistor to REXT. |
| REFCLKIP REFCLKIN | K1 K2 | I | Integrated Reference Clock Input Pair: Connect to external 100MHz differential clock for the integrated reference clock buffer. If the reference clock input is HCSL type, it can be AC or DC coupled. If the 100MHz clock source is not in HCSL protocol (ex: LVPECL, LVDS, etc), please refer to application note to add application circuit. |
| REFCLKOP[8:1] | H3,H1,J3,J1,K3,L3,L1,M3 | O | Integrated Reference Clock Output Pairs: 100MHz external differential HCSL clock outputs for the integrated reference clock buffer. Integrated reference clock outputs are turned on at 324/424/524/624 modes. They are turned off at 1224 and 1124 modes. |
| REFCLKON[8:1] | H4,H2,J4,J2,K4,L4,L2,M4 | | |
| IREF | M1 | I | Differential Reference Clock Output Current Resistor: External resistor (475 Ohm +/- 1%) connection to set the differential reference clock output current. |
| NT RESET_L | T14 | O | Propagate Reset in NT mode: Pulse width is 1 us. |

3.2 PORT SPECIFIC SIGNALS (17 BALLS)

| NAME | PIN | TYPE | DESCRIPTION |
|--------------------------|---------------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PORT_GOOD_L[9,8,6,5,1,0] | U18,P16,G2,F2,E1,F1 | O | <p>Port Good Status: These signals indicate the link status of each port. When continuously deasserts, the device is in the condition of link down. When continuously asserts, the link is up and operates at 5GT/s. When blinking, asserts and deasserts with 0.5-second intervals, the link is up and operates at 2.5GT/s.</p> <p>PORT_GOOD_L[x] is correspondent to Port x, where x=0,1,5,6,8,9.</p> |
| UPS_PORTSEL[3:0] | A15,P15,P14,C13 | I | <p>Upstream Port Selection: These signals decide which port will be the upstream port.</p> <p>Please refer to Section 5 for Port-Lane Mapping.</p> <p>These strapping pins have no built-in internal resistors and can not be left NC. These pins require the external 5.1K-ohm pull-up resistors or 330-ohm pull-down resistors.</p> |
| PORTCFG[2:0] | B13,B3,P13 | I | <p>Port-Lane Configuration: These signals decide Port-Lane configuration.</p> <p>Please refer to Section 5 for Port-Lane Mapping.</p> <p>These strapping pins have no built-in internal resistors and can not be left NC. These pins require the external 5.1K-ohm pull-up resistors or 330-ohm pull-down resistors.</p> |
| NT_EN_L | A3 | I | <p>NT Mode Enable: When tied low, NT mode is enabled. When tied high, NT mode is disabled. This strapping pin has no built-in internal resistor and cannot be left NC. The pin requires an external 5.1K-ohm pull-up resistor or 330-ohm pull-down resistor.</p> |
| NT_P2P_EN_L | U14 | I | <p>NT PCI-to-PCI Bridge Mode Enable: When tied low, NT PCI-to-PCI bridge mode is enabled. When tied high, NT PCI-to-PCI bridge mode is disabled. This pin has internal pull-up. If no board trace is connected to this pin, the internal pull-up resistor of this pin is enough. However, if pin is connected to a board trace and not driven, it is recommended that an external 5.1K-ohm pull-up resistor be used.</p> |
| NT_PORTSEL[1:0] | D3,C3 | I | <p>NT Port Selection: These signals decide which port will be the upstream NT port.</p> <p>Please refer to Section 5 for Port-Lane Mapping.</p> <p>These strapping pins have no built-in internal resistors and cannot be left NC. These pins require the external 5.1K-ohm pull-up resistors or 330-ohm pull-down resistors.</p> |

3.3 HOTPLUG SIGNALS (33 BALLS)

| NAME | PIN | TYPE | DESCRIPTION |
|-------------------|------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| HP_ATNLED_C/B/A_L | C14,H5,U17 | I/O | Hot Plug Attention LED Outputs: It is used to drive the Attention Indicator. Output is asserted low to turn on the LED. |
| HP_BUTTON_C/B/A_L | B16,R1,T17 | I/O | Hot Plug Attention Button Inputs: It is directly connected to the Attention Button. |
| HP_CLKEN_C/B/A_L | C15,P3,R15 | I/O | Hot Plug Reference Clock Enable Outputs: It is used to control the connection of the external REFCLK to the slot. |
| HP_MRL_C/A_L | B15,U16 | I/O | Hot Plug Manually Operated Retention Latch Sensor Inputs: It is connected directly to an optional MRL sensor that is logic low when the latch is close. |
| HP_MRL_B_L | N3 | I | Hot Plug Manually Operated Retention Latch Sensor Inputs: It is connected directly to an optional MRL sensor that is logic low when the latch is close. |
| HP_PERST_C/B/A_L | B14,R2,T16 | I/O | Hot Plug Reset Outputs: It is used to reset the slot. |
| HP_PRSNT_C/B/A_L | B17,T1,V17 | I/O | Hot Plug PRSNT2# Inputs: It is connects to the slot's PRSNT2# signal. |
| HP_PWREN_C/B/A | A16,V1,V16 | I/O | Hot Plug Power Enable Outputs: It is used to control the slot power state. |

| NAME | PIN | TYPE | DESCRIPTION |
|-------------------|------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| HP_PWRFLT_C/B/A_L | A17,P2,R16 | I/O | Hot Plug Power Fault Inputs: It is used to indicate that the slot's external Power Controller detected a power fault. |
| HP_PWR_GOOD_C/B/A | D17,N1,U15 | I | Hot Plug Power Good Inputs: It is used to indicate that the power supplies are active and stable. |
| HP_PWRLED_C/B/A_L | D15,T2,V15 | I/O | Hot Plug Power LED Outputs: It is used to drive the Power Indicator. This output is asserted low to turn on the LED. |
| SHCL_I2C | R14 | OD | I2C Clock Signal of Serial Hot Plug Controller: It is connected to SCL pin of all I2C IO expanders. |
| SHDA_I2C | V14 | OD | I2C Data Signal of Serial Hot Plug Controller: It is connected to SDA pin of all I2C IO expanders. |
| SHPCINT_L | E3 | I | Interrupt Input (Active Low) of Serial Hot Plug Controller: It is connected to INT# output pin of all I2C IO expanders. When asserted, it notifies Hot Plug Controller to access the port registers of all I/O expanders for touching changed status to de-assert INT#. |

3.4 EEPROM and I2C SIGNALS (9 BALLS)

| NAME | PIN | TYPE | DESCRIPTION |
|---------------|----------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EECK | C17 | I/O | EEPROM Clock: Clock signal to 4-wire EEPROM interface. |
| EEDI | C16 | O | EEPROM Data Input: Diodes 2G1224GP outputs data to the Data Input pin of Serial EEPROM. |
| EEDO | D16 | I | EEPROM Data Output: Diodes 2G1224GP inputs data from the Data Output pin of Serial EEPROM. |
| EECS_L | C18 | I/O | EEPROM Chip Select (Active Low): Diodes 2G1224GP asserts this signal to enable Serial EEPROM. EEPROM Bypass Mode (EEPROM_BYPASS): During system initialization, EECS_L acts as the EEPROM_BYPASS pin. When tied high, eeprom function is disabled. When tied low, eeprom function is enabled. This pin has internal pull-up resistor. If no board trace is connected to this pin, the internal pull-up resistor of this pin is enough. However, if pin is connected to a board trace and not driven, it is recommended that an external 5.1K-ohm pull-up resistor be used. |
| SCL_I2C | C1 | OD | I2C Serial Clock: I2C Bus Clock. This pin requires an external 5.1K-ohm pull-up resistor. |
| SDA_I2C | D1 | OD | I2C Serial Data: Bi-Directional I2C Bus Data. This pin requires an external 5.1K-ohm pull-up resistor. |
| I2C_ADDR[2:0] | G4,F3,G1 | I | I2C Slave Address Bit [2:0]: These pins are used to configure the value of the three least significant bits of the PI7C2G1224GP 7-bit Slave address. These pins require the external 5.1K-ohm pull-up resistors or 330-ohm pull-down resistors. |

3.5 MISCELLANEOUS SIGNALS (29 BALLS)

| NAME | PIN | TYPE | DESCRIPTION |
|----------------------------------------------------|-------------------------------------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GPIO[11,10,7,4:2] / PORT_GOOD_L[11,10,7,4:2] | T18,R17,G5,G3, P1,N2 | I/O O | <p>General Purpose Input and Output: When PORT_GOOD_LED_EN tied high, these general-purpose pins are programmed as either input-only or bi-directional pins by writing the GPIO output enable control register.</p> <p>Port Good Status: When PORT_GOOD_LED_EN tied low, these signals indicate the link status of each port. When continuously deasserts, the device is in the condition of link down. When continuously asserts, the link is up and operates at 5GT/s. When blinking, asserts and deasserts with 0.2-second intervals, the link is up and operates at 2.5GT/s.</p> <p>PORT_GOOD_L[x] is correspondent to Port x, where x=2,3,4,7,10,11.</p> |
| GPIO[19:12] | V2,T3,R3,U3, R18,V18,B18, A18 | I/O | <p>General Purpose Input and Output: These eight general-purpose pins are programmed as either input-only or bi-directional pins by writing the GPIO output enable control register.</p> <p>CFG Timer Enable (CFG_TIMER_EN_L): During system initialization, GPIO[18] acts as the CFG_TIMER_EN_L pin. When tied high, TS pkts always advertises support for GENII data rate and autonomous change. When tied low, if the LTSSM fails during the Configuration state, TS pkts only advertises GENI data rate and no autonomous change support in next time the LTSSM exists the Detect state. If the LTSSM fails continuously in Configuration state, the LTSSM continues to alternate between GENI and GENII advertisement every time it exists the Detect state. This pin has internal pull-up. If no board trace is connected to this pin, the internal pull-up resistor of this pin is enough. However, if pin is connected to a board trace and not driven, it is recommended that an external 5.1K-ohm pull-up resistor be used.</p> |
| FATAL_ERR_L | A14 | O | Fatal Error Output: It is asserted low when a Fatal error is detected. |
| INTA_L | B1 | OD | Interrupt Output Enable: When tied low, it indicates that one or more of the following events/errors are detected: Hot Plug events, Link State events, General-Purpose Input Interrupt events, Device-Specific errors, Device-Specific NT Port Link Interface errors and events, NT-Virtual Doorbell events or NT-Link Doorbell events. |
| DEBUG_SEL[1:0] | U2,U13 | I | <p>Test Only Must be pulled up by an external 5.1K-ohm resistor.</p> <p>Port Good Enable (PORT_GOOD_LED_EN): During system initialization, DEBUG_SEL[1] acts as the PORT_GOOD_LED_EN pin. When tied high, PORT_GOOD_L[9,8,6,5,1,0] and GPIO[11:10,7,4:2] are port good status pins. Otherwise, PORT_GOOD_L[9,8,6,5,1,0] does not work and GPIO[11:10,7,4:2] are general purpose input and output pins. This strapping pin has no built-in internal resistor and cannot be left NC. The pin requires an external 5.1K-ohm pull-up resistor or 330-ohm pull-down resistor.</p> |
| FAST_MODE_L | N13 | I | Test Only Must be pulled up by an external 5.1K-ohm resistor |
| SERDES_MODE_EN_L | P18 | I | Test Only Must be pulled up by an external 5.1K-ohm resistor. |
| TESTMODE[2] | T13 | I | <p>Test Only Must be pulled up by an external 5.1K-ohm resistor.</p> <p>Gen1 Cap. Only Enable (GENICAP_ONLY_EN_L): During system initialization, TESTMODE[2] acts as the GENICAP_ONLY_EN_L pin. When tied high, the max. link speed is set to 5.0 G b/s. When tied low, the max. link speed is set to 2.5G b/s. This strapping pin has no built-in internal resistor and can not be left NC. The pin requires an external 5.1K-ohm pull-up resistor or 330-ohm pull-down resistor.</p> |

| NAME | PIN | TYPE | DESCRIPTION |
|---------------|-----------------------|------|--------------------------------------------------------------------------|
| TESTMODE[1:0] | V13,V3 | I | Test Only Must be pulled down by an external 330-ohm resistor. |
| PLL_BYPASS_L | P17 | I | Test Only Must be pulled up by an external 5.1K-ohm resistor. |
| NC | A8,B8,J17,J18, R13 | | No Connection: leaves these pins floating. |

3.6 JTAG BOUNDARY SCAN SIGNALS (5 Balls)

| Name | Pin | Type | Description |
|--------|-----|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TCK | A2 | I | Test Clock: Used to clock state information and data into and out of the chip during boundary scan. When JTAG boundary scan function is not implemented, this pin should be left open (NC). |
| TDI | A1 | I | Test Mode Select: Used to control the state of the Test Access Port controller. When JTAG boundary scan function is not implemented, this pin should be pulled low through a 330-Ohm pull-down resistor. |
| TDO | B2 | O | Test Data Output: When SCAN_EN is high, it is used (in conjunction with TCK) to shift data out of the Test Access Port (TAP) in a serial bit stream. When JTAG boundary scan function is not implemented, this pin should be left open (NC). |
| TMS | E2 | I | Test Data Input: When SCAN_EN is high, it is used (in conjunction with TCK) to shift data and instructions into the TAP in a serial bit stream. When JTAG boundary scan function is not implemented, this pin should be left open (NC). |
| TRST_L | D2 | I | Test Reset (Active LOW): Active LOW signal to reset the TAP controller into an initialized state. When JTAG boundary scan function is not implemented, this pin should be pulled low through a 330-Ohm pull-down resistor. |

3.7 POWER PINS (106 BALLS)

| NAME | PIN | TYPE | DESCRIPTION |
|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|---------------------------------------------------------------------------------|
| VDDC | G7,G9,G11,H8,H10,H12, J7,J9,J11,K8,K10,K12,L7, L9,L11,M8,M10,M12 | P | VDDC Supply (1.0V): Used as digital core power pins. |
| VDDR | F5,F13,L13,N5,T15 | P | VDDR Supply (3.3V): Used as digital I/O power pins. |
| CVDDR | J5,L5 | P | VDDR Supply (3.3V): Used as reference clock power pins. |
| AVDD | F6,F10,F12,G13,H6,K6, K13,M6,N9,N11 | P | AVDD Supply (1.0V): Used as PCI Express analog power pins. |
| AVDDH | F8,J13,N8 | P | AVDDH Supply (3.3V): Used as PCI Express analog high voltage power pins. |
| VSS | A13,C2,C4,C5,C6,C7, C8,C9,C10,C11,C12,D13, D14,D18,E13,E16,F4,F7, F9,F11,F16,G6,G8,G10, G12,G16,H7,H9,H11,H13, H16,J6,J8,J10,J12,J16,K5, K7,K9,K11,K16,L6,L8, L10,L12,L16,M2,M5,M7, M9,M11,M13,M16,N4,N6, N7,N10,N12,N16,T4,T5, T6,T7,T8,T9,T10,T11,T12 | P | Ground: Used as ground pins. |

4 PIN DESCRIPTION

4.1 PIN LIST of 324-BALL HSBGA

| PIN | NAME | PIN | NAME | PIN | NAME | PIN | NAME |
|-----|----------------|-----|----------------|-----|---------------|-----|------------------|
| A1 | TDI | E10 | PERP[18] | K1 | REFCLKIP | P10 | PERP[5] |
| A2 | TCK | E11 | PERP[17] | K2 | REFCLKIN | P11 | PERP[6] |
| A3 | NT_EN_L | E12 | PERP[16] | K3 | REFCLKOP[4] | P12 | PERP[7] |
| A4 | PETN[23] | E13 | VSS | K4 | REFCLKON[4] | P13 | PORTCFG[0] |
| A5 | PETN[22] | E14 | PERP[15] | K5 | VSS | P14 | UPS_PORTSEL[1] |
| A6 | PETN[21] | E15 | PERN[15] | K6 | AVDD | P15 | UPS_PORTSEL[2] |
| A7 | PETN[20] | E16 | VSS | K7 | VSS | P16 | PORT_GOOD_L[8] |
| A8 | NC | E17 | PETP[15] | K8 | VDDC | P17 | PLL_BYPASS_L |
| A9 | PETN[19] | E18 | PETN[15] | K9 | VSS | P18 | SERDES_MODE_EN_L |
| A10 | PETN[18] | F1 | PORT_GOOD_L[0] | K10 | VDDC | R1 | HP_BUTTON_B_L |
| A11 | PETN[17] | F2 | PORT_GOOD_L[5] | K11 | VSS | R2 | HP_PERST_B_L |
| A12 | PETN[16] | F3 | I2C_ADDR[1] | K12 | VDDC | R3 | GPIO[17] |
| A13 | VSS | F4 | VSS | K13 | AVDD | R4 | PERN[0] |
| A14 | FATAL_ERR_L | F5 | VDDR | K14 | PERP[11] | R5 | PERN[1] |
| A15 | UPS_PORTSEL[3] | F6 | AVDD | K15 | PERN[11] | R6 | PERN[2] |
| A16 | HP_PWREN_C | F7 | VSS | K16 | VSS | R7 | PERN[3] |
| A17 | HP_PWRFLT_C_L | F8 | AVDDH | K17 | PETP[11] | R8 | REXT[0] |
| A18 | GPIO[12] | F9 | VSS | K18 | PETN[11] | R9 | PERN[4] |
| B1 | INTA_L | F10 | AVDD | L1 | REFCLKOP[2] | R10 | PERN[5] |
| B2 | TDO | F11 | VSS | L2 | REFCLKON[2] | R11 | PERN[6] |
| B3 | PORTCFG[1] | F12 | AVDD | L3 | REFCLKOP[3] | R12 | PERN[7] |
| B4 | PETP[23] | F13 | VDDR | L4 | REFCLKON[3] | R13 | NC |
| B5 | PETP[22] | F14 | PERP[14] | L5 | CVDDR | R14 | SHCL_I2C |
| B6 | PETP[21] | F15 | PERN[14] | L6 | VSS | R15 | HP_CLKEN_A_L |
| B7 | PETP[20] | F16 | VSS | L7 | VDDC | R16 | HP_PWRFLT_A_L |
| B8 | NC | F17 | PETP[14] | L8 | VSS | R17 | GPIO[10] |
| B9 | PETP[19] | F18 | PETN[14] | L9 | VDDC | R18 | GPIO[15] |
| B10 | PETP[18] | G1 | I2C_ADDR[0] | L10 | VSS | T1 | HP_PRSNT_B_L |
| B11 | PETP[17] | G2 | PORT_GOOD_L[6] | L11 | VDDC | T2 | HP_PWRLED_B_L |
| B12 | PETP[16] | G3 | GPIO[4] | L12 | VSS | T3 | GPIO[18] |
| B13 | PORTCFG[2] | G4 | I2C_ADDR[2] | L13 | VDDR | T4 | VSS |
| B14 | HP_PERST_C_L | G5 | GPIO[7] | L14 | PERP[10] | T5 | VSS |
| B15 | HP_MRL_C_L | G6 | VSS | L15 | PERN[10] | T6 | VSS |
| B16 | HP_BUTTON_C_L | G7 | VDDC | L16 | VSS | T7 | VSS |
| B17 | HP_RESNT_C_L | G8 | VSS | L17 | PETP[10] | T8 | VSS |
| B18 | GPIO[13] | G9 | VDDC | L18 | PETN[10] | T9 | VSS |
| C1 | SCL_I2C | G10 | VSS | M1 | IREF | T10 | VSS |
| C2 | VSS | G11 | VDDC | M2 | VSS | T11 | VSS |
| C3 | NT_PORTSEL[0] | G12 | VSS | M3 | REFCLKOP[1] | T12 | VSS |
| C4 | VSS | G13 | AVDD | M4 | REFCLKON[1] | T13 | TESTMODE[2] |
| C5 | VSS | G14 | PERP[13] | M5 | VSS | T14 | NT_RESET_L |
| C6 | VSS | G15 | PERN[13] | M6 | AVDD | T15 | VDDR |
| C7 | VSS | G16 | VSS | M7 | VSS | T16 | HP_PERST_A_L |
| C8 | VSS | G17 | PETP[13] | M8 | VDDC | T17 | HP_BUTTON_A_L |
| C9 | VSS | G18 | PETN[13] | M9 | VSS | T18 | GPIO[11] |
| C10 | VSS | H1 | REFCLKOP[7] | M10 | VDDC | U1 | PERST_L |
| C11 | VSS | H2 | REFCLKON[7] | M11 | VSS | U2 | DEBUG_SEL[1] |
| C12 | VSS | H3 | REFCLKOP[8] | M12 | VDDC | U3 | GPIO[16] |
| C13 | UPS_PORTSEL[0] | H4 | REFCLKON[8] | M13 | VSS | U4 | PETP[0] |
| C14 | HP_ATNLED_C_L | H5 | HP_ATNLED_B_L | M14 | PERP[9] | U5 | PETP[1] |
| C15 | HP_CLKEN_C_L | H6 | AVDD | M15 | PERN[9] | U6 | PETP[2] |
| C16 | EEDI | H7 | VSS | M16 | VSS | U7 | PETP[3] |
| C17 | EECK | H8 | VDDC | M17 | PETP[9] | U8 | REFCLKP |
| C18 | EECS_L | H9 | VSS | M18 | PETN[9] | U9 | PETP[4] |
| D1 | SDA_I2C | H10 | VDDC | N1 | HP_PWR_GOOD_B | U10 | PETP[5] |
| D2 | TRST_L | H11 | VSS | N2 | GPIO[2] | U11 | PETP[6] |

| PIN | NAME | PIN | NAME | PIN | NAME | PIN | NAME |
|-----|----------------|-----|-------------|-----|---------------|-----|----------------|
| D3 | NT_PORTSEL[1] | H12 | VDDC | N3 | HP_MRL_B_L | U12 | PETP[7] |
| D4 | PERN[23] | H13 | VSS | N4 | VSS | U13 | DEBUG_SEL[0] |
| D5 | PERN[22] | H14 | PERP[12] | N5 | VDDR | U14 | NT_P2P_EN_L |
| D6 | PERN[21] | H15 | PERN[12] | N6 | VSS | U15 | HP_PWR_GOOD_A |
| D7 | PERN[20] | H16 | VSS | N7 | VSS | U16 | HP_MRL_A_L |
| D8 | REXT[2] | H17 | PETP[12] | N8 | AVDDH | U17 | HP_ATNLED_A_L |
| D9 | PERN[19] | H18 | PETN[12] | N9 | AVDD | U18 | PORT_GOOD_L[9] |
| D10 | PERN[18] | J1 | REFCLKOP[5] | N10 | VSS | V1 | HP_PWREN_B |
| D11 | PERN[17] | J2 | REFCLKON[5] | N11 | AVDD | V2 | GPIO[19] |
| D12 | PERN[16] | J3 | REFCLKOP[6] | N12 | VSS | V3 | TESTMODE[0] |
| D13 | VSS | J4 | REFCLKON[6] | N13 | FAST_MODE_L | V4 | PETN[0] |
| D14 | VSS | J5 | CVDDR | N14 | PERP[8] | V5 | PETN[1] |
| D15 | HP_PWRLED_C_L | J6 | VSS | N15 | PERN[8] | V6 | PETN[2] |
| D16 | EEDO | J7 | VDDC | N16 | VSS | V7 | PETN[3] |
| D17 | HP_PWR_GOOD_C | J8 | VSS | N17 | PETP[8] | V8 | REFCLKN |
| D18 | VSS | J9 | VDDC | N18 | PETN[8] | V9 | PETN[4] |
| E1 | PORT_GOOD_L[1] | J10 | VSS | P1 | GPIO[3] | V10 | PETN[5] |
| E2 | TMS | J11 | VDDC | P2 | HP_PWRFLT_B_L | V11 | PETN[6] |
| E3 | SHPINT_L | J12 | VSS | P3 | HP_CLKEN_B_L | V12 | PETN[7] |
| E4 | PERP[23] | J13 | AVDDH | P4 | PERP[0] | V13 | TESTMODE[1] |
| E5 | PERP[22] | J14 | REXT_GND[2] | P5 | PERP[1] | V14 | SHDA_I2C |
| E6 | PERP[21] | J15 | REXT[2] | P6 | PERP[2] | V15 | HP_PWRLED_A_L |
| E7 | PERP[20] | J16 | VSS | P7 | PERP[3] | V16 | HP_PWREN_A |
| E8 | REXT_GND[2] | J17 | NC | P8 | REXT_GND[0] | V17 | HP_PRSNT_A_L |
| E9 | PERP[19] | J18 | NC | P9 | PERP[4] | V18 | GPIO[14] |

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | |
|----------|-----------------|-----------------|---------------|--------------|----------------|-----------|-----------|-------------|-----------|-----------|-----------|-----------|----------------|-----------------|-----------------|-----------------|----------------|------------------|----------|
| A | TDI | TCK | NT_EN_L | PETN [23] | PETN [22] | PETN [21] | PETN [20] | NC | PETN [19] | PETN [18] | PETN [17] | PTEN [16] | VSS | FATAL_ERR_L | UPS_PORTSEL[3] | HP_PWR_EN_C | HP_PWR_FLT_C_L | GPIO[12] | A |
| B | INTA_L | TDO | PORTCFG[1] | PETP [23] | PETP [22] | PTEP [21] | PTEP [20] | NC | PETP [19] | PTEP [18] | PTEP [17] | PTEP [16] | PORTCFG[2] | HP_PERST_C_L | HP_MRL_C_L | HP_BUT_TON_C_L | HP_PRS_NT_C_L | GPIO[13] | B |
| C | SCL_I2C | VSS | NT_PORTSEL[0] | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | UPS_PORTSEL[0] | HP_ATN_LED_C_L | HP_CLK_EN_C_L | EEDI | EECK | EECS_L | C |
| D | SDA_I2C | TRST_L | NT_PORTSEL[1] | PERN [23] | PERN [22] | PERN [21] | PERN [20] | REXT[2] | PERN [19] | PERN [18] | PERN [17] | PERN [16] | VSS | VSS | HP_PWR_LED_C_L | EEDO | HP_PWR_GOOD_C | VSS | D |
| E | PORT_GOOD_L [1] | TMS | SHPINT_L | PERP [23] | PERP [22] | PERP [21] | PERP [20] | REXT_GND[2] | PERP [19] | PERP [18] | PERP [17] | PERP [16] | VSS | PERP [15] | PERN [15] | VSS | PETP [15] | PETN [15] | E |
| F | PORT_GOOD_L [0] | PORT_GOOD_L [5] | I2C_ADDR[1] | VSS | VDDR | AVDD | VSS | AVDDH | VSS | AVDD | VSS | AVDD | VDDR | PERP [14] | PERN [14] | VSS | PETP [14] | PETN [14] | F |
| G | I2C_ADDR[0] | PORT_GOOD_L [6] | GPIO[4] | I2C_ADDR[2] | GPIO[7] | VSS | VDDC | VSS | VDDC | VSS | VDDC | VSS | AVDD | PERP [13] | PERN [13] | VSS | PETP [13] | PETN [13] | G |
| H | REFCLK_OP[7] | REFCLK_ON[7] | REFCLK_OP[8] | REFCLK_ON[8] | HP_ATN_LED_B_L | AVDD | VSS | VDDC | VSS | VDDC | VSS | VDDC | VSS | PERP [12] | PERN [12] | VSS | PETP [12] | PETN [12] | H |
| J | REFCLK_OP[5] | REFCLK_ON[5] | REFCLK_OP[6] | REFCLK_ON[6] | CVDDR | VSS | VDDC | VSS | VDDC | VSS | VDDC | VSS | AVDDH | REXT_GND[1] | REXT[1] | VSS | NC | NC | J |
| K | REFCLK_IP | REFCLK_IN | REFCLK_OP[4] | REFCLK_ON[4] | VSS | AVDD | VSS | VDDC | VSS | VDDC | VSS | VDDC | AVDD | PERP [11] | PERN [11] | VSS | PETP [11] | PETN [11] | K |
| L | REFCLK_OP[2] | REFCLK_ON[2] | REFCLK_OP[3] | REFCLK_ON[3] | CVDDR | VSS | VDDC | VSS | VDDC | VSS | VDDC | VSS | VDDR | PERP [10] | PERN [10] | VSS | PETP [10] | PETN [10] | L |
| M | IREF | VSS | REFCLK_OP[1] | REFCLK_ON[1] | VSS | AVDD | VSS | VDDC | VSS | VDDC | VSS | VDDC | VSS | PERP[9] | PERN[9] | VSS | PETP[9] | PETN[9] | M |
| N | HP_PWR_GOOD_B | GPIO[2] | HP_MRL_B_L | VSS | VDDR | VSS | VSS | AVDDH | AVDD | VSS | AVDD | VSS | FAST_MODE_L | PERP[8] | PERN[8] | VSS | PETP[8] | PETN[8] | N |
| P | GPIO[3] | HP_PWR_FLT_B_L | HP_CLK_EN_B_L | PERP[0] | PERP[1] | PERP[2] | PERP[3] | REXT_GND[0] | PERP[4] | PERP[5] | PERP[6] | PERP[7] | PORTCFG[0] | UPS_PORTSEL [1] | UPS_PORTSEL [2] | PORT_GOOD_L [8] | PLL_BY_PASS_L | SERDES_MODE_EN_L | P |
| R | HP_BUT_TON_B_L | HP_PERST_B_L | GPIO[17] | PERN[0] | PERN[1] | PERN[2] | PERN[3] | REXT[0] | PERN[4] | PERN[5] | PERN[6] | PERN[7] | NC | SHCL_I2C | HP_CLK_EN_A_L | HP_PWR_FLT_A_L | GPIO[10] | GPIO[15] | R |
| T | HP_PRS_NT_B_L | HP_PWR_LED_B_L | GPIO[18] | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | TESTMODE[2] | NT_RESET_L | VDDR | HP_PERST_A_L | HP_BUT_TON_A_L | GPIO[11] | T |
| U | PERST_L | DEBUG_SEL[1] | GPIO[16] | PETP[0] | PETP[1] | PETP[2] | PETP[3] | REFCLK_P | PETP[4] | PETP[5] | PETP[6] | PETP[7] | DEBUG_SEL[0] | NT_P2P_EN_L | HP_PWR_GOOD_A | HP_MRL_A_L | HP_ATN_LED_A_L | PORT_GOOD_L [9] | U |
| V | HP_PWR_EN_B_L | GPIO[19] | TESTMODE[0] | PETN[0] | PETN[1] | PETN[2] | PETN[3] | REFCLK_N | PETN[4] | PETN[5] | PETN[6] | PETN[7] | TESTMODE[1] | SHDA_I2C | HP_PWR_LED_A_L | HP_PWR_EN_A | HP_PRS_NT_A_L | GPIO[14] | V |

Figure 4-1 PI7C9X2G1224GP Ball Assignment

5 MODE SELECTION AND PORT-LANE MAPPING

5.1 MODE SELECTION

The PI7C9X2G1224GP can be configured into 12 Port-24 Lane, 11 Port-24 Lane, 6 Port-24 Lane, 5 Port-24 Lane, 4 Port-24 Lane and 3 Port-24 Lane modes by setting PORTCFG[2:0] pins.

| PORTCFG[2] | PORTCFG[1] | PORTCFG[0] | Functional Mode |
|------------|------------|------------|-----------------------------|
| 1 | 1 | 1 | 12Port-24Lane Configuration |
| 1 | 1 | 0 | 11Port-24Lane Configuration |
| 1 | 0 | 1 | 3Port-24Lane Configuration |
| 1 | 0 | 0 | Reserved |
| 0 | 1 | 1 | 5Port-24Lane Configuration |
| 0 | 1 | 0 | 6Port-24Lane Configuration |
| 0 | 0 | 1 | 4Port-24Lane Configuration |
| 0 | 0 | 0 | Reserved |

5.2 LANE MAPPING

The table below shows the mapping of the lanes to the transmission and receives pairs.

| Lane | TX Pair | RX Pair |
|---------|------------------|------------------|
| Lane 0 | PETP[0]PETN[0] | PERP[0]PERN[0] |
| Lane 1 | PETP[1]PETN[1] | PERP[1]PERN[1] |
| Lane 2 | PETP[2]PETN[2] | PERP[2]PERN[2] |
| Lane 3 | PETP[3]PETN[3] | PERP[3]PERN[3] |
| Lane 4 | PETP[4]PETN[4] | PERP[4]PERN[4] |
| Lane 5 | PETP[5]PETN[5] | PERP[5]PERN[5] |
| Lane 6 | PETP[6]PETN[6] | PERP[6]PERN[6] |
| Lane 7 | PETP[7]PETN[7] | PERP[7]PERN[7] |
| Lane 8 | PETP[8]PETN[8] | PERP[8]PERN[8] |
| Lane 9 | PETP[9]PETN[9] | PERP[9]PERN[9] |
| Lane 10 | PETP[10]PETN[10] | PERP[10]PERN[10] |
| Lane 11 | PETP[11]PETN[11] | PERP[11]PERN[11] |
| Lane 12 | PETP[12]PETN[12] | PERP[12]PERN[12] |
| Lane 13 | PETP[13]PETN[13] | PERP[13]PERN[13] |
| Lane 14 | PETP[14]PETN[14] | PERP[14]PERN[14] |
| Lane 15 | PETP[15]PETN[15] | PERP[15]PERN[15] |
| Lane 16 | PETP[16]PETN[16] | PERP[16]PERN[16] |
| Lane 17 | PETP[17]PETN[17] | PERP[17]PERN[17] |
| Lane 18 | PETP[18]PETN[18] | PERP[18]PERN[18] |
| Lane 19 | PETP[19]PETN[19] | PERP[19]PERN[19] |
| Lane 20 | PETP[20]PETN[20] | PERP[20]PERN[20] |
| Lane 21 | PETP[21]PETN[21] | PERP[21]PERN[21] |
| Lane 22 | PETP[22]PETN[22] | PERP[22]PERN[22] |
| Lane 23 | PETP[23]PETN[23] | PERP[23]PERN[23] |

5.3 PORT-LANE MAPPING

The table below shows the mapping of the lanes to ports in different functional modes via UPS_PORTSEL[3:0] settings.

The table below shows the mapping of the lanes to ports in different functional modes via UPS_PORTSEL[3:0] settings.

| UPS_PORTSEL[3:0] = 0 | Functional Mode | | | | | |
|----------------------|-----------------|------|-----|-----|-----|-----|
| | 1224 | 1124 | 624 | 524 | 424 | 324 |
| Lane 0 | P0 | P0 | P0 | P0 | P0 | P0 |
| Lane 1 | P0 | P0 | P0 | P0 | P0 | P0 |
| Lane 2 | P0 | P0 | P0 | P0 | P0 | P0 |
| Lane 3 | P0 | P0 | P0 | P0 | P0 | P0 |
| Lane 4 | P4 | P5 | P4 | P0 | P0 | P0 |
| Lane 5 | P5 | P5 | P4 | P0 | P0 | P0 |
| Lane 6 | P6 | P6 | P4 | P0 | P0 | P0 |
| Lane 7 | P7 | P6 | P4 | P0 | P0 | P0 |
| Lane 8 | P2 | P2 | P2 | P4 | P2 | P2 |
| Lane 9 | P2 | P2 | P2 | P4 | P2 | P2 |
| Lane 10 | P2 | P7 | P2 | P4 | P2 | P2 |
| Lane 11 | P2 | P7 | P2 | P4 | P2 | P2 |
| Lane 12 | P8 | P4 | P5 | P5 | P5 | P2 |
| Lane 13 | P9 | P4 | P5 | P5 | P5 | P2 |
| Lane 14 | P10 | P10 | P5 | P5 | P5 | P2 |
| Lane 15 | P11 | P10 | P5 | P5 | P5 | P2 |
| Lane 16 | P1 | P1 | P1 | P1 | P1 | P1 |
| Lane 17 | P1 | P1 | P1 | P1 | P1 | P1 |
| Lane 18 | P1 | P8 | P1 | P1 | P1 | P1 |
| Lane 19 | P1 | P8 | P1 | P1 | P1 | P1 |
| Lane 20 | P3 | P3 | P3 | P3 | P1 | P1 |
| Lane 21 | P3 | P3 | P3 | P3 | P1 | P1 |
| Lane 22 | P3 | P9 | P3 | P3 | P1 | P1 |
| Lane 23 | P3 | P9 | P3 | P3 | P1 | P1 |

Notes:

P0: upstream port

P1~P11: downstream ports

The table below shows all acceptable values of UPS_PORTSEL[3:0] and NT_PORTSEL[1:0] in different functional mode.

| Acceptable Values | UPS_PORTSEL[3:0] | NTPORT_SEL[1:0] |
|-------------------|---------------------|---------------------|
| 1224 Mode | 0~3 are allowed | 0~3 are allowed |
| 1124 Mode | 0 is allowed | 1~3 are allowed |
| 624 Mode | 0~5 are allowed | 0~3 are allowed |
| 524 Mode | 0 is allowed | 1 and 3 are allowed |
| 424 Mode | 0 and 1 are allowed | 0 and 1 are allowed |
| 324 Mode | 0~2 are allowed | 0~2 are allowed |

Notes:

- 1) Upstream port is on P0, and NT port is on P1 if NT mode is enabled.
- 2) It is forbidden that NT_PORTSEL[1:0] and UPS_PORTSEL[3:0] have the same values.
- 3) For example, in 1224 mode, by default, Port 0 is mapped to Lane 0~3 and Port 3 is mapped to Lane 20~23.
When UPS_PORTSEL is set to 3, Port 0 will be changed to map to Lane 20~23 and Port 3 be changed to map to Lane 0~3.
- 4) For example, in 1224 mode, by default, Port 1 is NT port and mapped to Lane 16~19 if NT mode is enabled, and Port 2 is mapped to Lane 8~11.
When UPS_PORTSEL is set to 3 and NT_PORTSEL is set to 2,
Port 0 will be changed to map to Lane 20~23 (Up port)
Port 3 will be changed to map to Lane 0~3
Port 1 will be changed to map to Lane 8~11 (NT port)
Port 2 will be changed to map to Lane 16~19

6 FUNCTIONAL DESCRIPTION

Multiple virtual PCI-to-PCI Bridges (VPPB), connected by a virtual PCI bus, reside in the Switch. Each VPPB contains the complete PCIe architecture layers that consist of the physical, data link, and transaction layer. The packets entering the Switch via one of VPPBs are first converted from serial bit-stream into parallel bus signals in physical layer, stripped off the link-related header by data link layer, and then relayed up to the transaction layer to extract out the transaction header. According to the address or ID embedded in the transaction header, the entire transaction packets are forwarded to the destination VPPB for formatting as a serial-type PCIe packet through the transmit circuits in the data link layer and physical layer. The following sections describe these function elements for processing PCIe packets within the Switch.

6.1 PHYSICAL LAYER CIRCUIT

The physical layer circuit design is based on the PHY Interface for PCI Express Architecture (PIPE). It contains Physical Media Attachment (PMA) and Physical Coding Sub-layer (PCS) blocks. PMA includes Serializer/ Deserializer (SERDES), PLL¹, Clock Recovery module, receiver detection circuits, beacon transmitter, electrical idle detector, and input/output buffers. PCS consists of framer, 8B/10B encoder/decoder, receiver elastic buffer, and PIPE PHY control/status circuitries. To provide the flexibility for port configuration, each lane has its own control and status signals for MAC to access individually. The main functions of physical layer circuits include the conversion between serial-link and parallel bus, provision of clock source for the Switch, resolving clock difference in receiver end, and detection of physical layer errors.

In order to meet the needs of different application, the drive amplitude, de-emphasis and equalization of each transmitting channels can be adjusted using EEPROM or I2C individually. De-emphasis of -3.5 db is implemented by the transmitters when full swing signaling is used, while an offset can be individually applied to each channel.

6.1.1 RECEIVER DETECTION

The physical layer circuits implement receiver detection, which detects the presence of an attached 50 ohm to ground termination as per PCI Express Specification. The detect circuits determine if the voltage levels of the receiver have crossed the internal threshold after a configurable time determined by the Receiver Detection Threshold field in the PHY Parameter 2 Register (offset 858h, bit[6:4]) as listed in Table 6-1, which can be configured by EEPROM or I2C settings.

Table 6-1 Receiver Detection Threshold Settings

| Receiver Detection Threshold | Threshold |
|------------------------------|----------------------|
| 000 | 1.0 us |
| 001 | 2.0 us |
| 010 | 4.0 us (Recommended) |
| 011 | 5.0 us |
| 100 | 7.0 us |
| 101 | Reserved |
| 110 | Reserved |
| 111 | Reserved |

¹ Multiple lanes could share the PLL.

6.1.2 RECEIVER SIGNAL DETECTION

Receiver signal idling is detected with levels above a programmable threshold specified by Receiver Signal Detect field in the PHY Parameter 2 Register (offset 858h, bit[21:20]) as listed in Table 6-2, and can be configured on a per-port basis via EEPROM or I2C settings.

Table 6-2 Receiver Signal Detect Threshold

| Receiver Signal Detect | Min (mV ppd) | Max (mV ppd) |
|------------------------|--------------|--------------|
| 00 | 50 | 150 |
| 01 (Recommended) | 65 | 175 |
| 10 | 75 | 200 |
| 11 | 120 | 240 |

6.1.3 RECEIVER EQUALIZATION

The receiver implements programmable equalizer via the Receiver Equalization field in the PHY Parameter 2 Register (offset 858h, bit[25:22] and bit[29:26]) as listed in Table 6-3, which can be configured on a per-port basis via EEPROM or I2C settings.

Table 6-3 Receiver Equalization Settings

| Receiver Equalization | Equalization |
|-----------------------|--------------|
| 0000 (Recommended) | Off |
| 0010 | Low |
| 0110 | Medium |
| 1110 | High |

6.1.4 TRANSMITTER SWING

The PCI Express transmitters support implementations of both full voltage swing and half (low) voltage swing. In full swing signaling mode, the transmitters implement de-emphasis, while in half swing mode, the transmitters do not. The Transmitter Swing field in the PHY Parameter 2 Register (offset 858h, bit[30]) is used for the selection of full swing signaling or half swing signaling, which can be configured on a per-port basis via EEPROM or I2C settings.

Table 6-4 Transmitter Swing Settings

| Transmitter Swing | Mode | De-emphasis |
|-------------------|--------------------|-----------------|
| 0 | Full Voltage Swing | Implemented |
| 1 | Half Voltage Swing | Not implemented |

6.1.5 DRIVE AMPLITUDE AND DE-EMPHASIS SETTINGS

Depending on the operation condition (voltage swing and de-emphasis condition), one of the Drive Amplitude Base Level fields in the PHY Parameter 0 Register (offset 8B0h) and one of the Drive De-Emphasis Base Level fields in the PHY Parameter 1 Register (offset 854h) are active for configuration of the amplitude and de-emphasis.

In addition, optional offset values can be added to the drive amplitude and drive de-emphasis on a per-port basis via EEPROM settings. The final drive amplitude and drive de-emphasis are the summation of the base level value and the offset value. The offset value for drive amplitude is 25 mV pd, and 6.25 mV pd for drive de-emphasis.

The driver output waveform is the synthesis of amplitude and de-emphasis as shown in Figure 6-1. The driver amplitude without de-emphasis is specified as a peak differential voltage level (mVpd), and the driver de-emphasis modifies the driver amplitude.

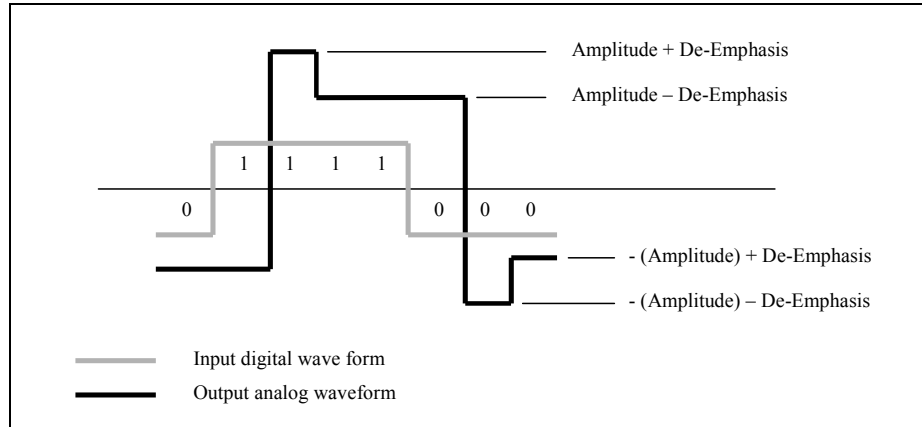


Figure 6-1 Driver Output Waveform

6.1.6 DRIVE AMPLITUDE

Only one of the Drive Amplitude Level field in the PHY Parameter 0 Register (offset 8B0h, bit[20:16], bit[25:21] and bit[30:26]) listed in Table 6-5 is active depending on the de-emphasis and swing condition. The settings and the corresponding values of the amplitude level are listed in Table 6-6, which can be configured by EEPROM or I2C settings.

Table 6-5 Drive Amplitude Base Level Registers

| Active Register | De-Emphasis Condition | Swing Condition |
|---------------------------------|-----------------------|-----------------|
| Drive Amplitude Level (3P5 Nom) | -3.5 db | Full |
| Drive Amplitude Level (6P0 Nom) | -6.0 db | Full |
| Drive Amplitude Level (Half) | N/A | Half |

Table 6-6 Drive Amplitude Base Level Settings

| Setting | Amplitude (mV pd) | Setting | Amplitude (mV pd) | Setting | Amplitude (mV pd) |
|---------|-------------------|---------|-------------------|---------|-------------------|
| 00000 | 0 | 00111 | 175 | 01110 | 350 |
| 00001 | 25 | 01000 | 200 | 01111 | 375 |
| 00010 | 50 | 01001 | 225 | 10000 | 400 |
| 00011 | 75 | 01010 | 250 | 10001 | 425 |
| 00100 | 100 | 01011 | 275 | 10010 | 450 |
| 00101 | 125 | 01100 | 300 | 10011 | 475 |
| 00110 | 150 | 01101 | 325 | Others | Reserved |

Note:

1. Nominal levels. Actual levels will vary with temperature, voltage and board effects.
2. The maximum nominal amplitude of the output driver is 475 mV pd. Combined values of driver amplitude and de-emphasis greater than 475 mV pd should be avoided.
3. At higher amplitudes, actual swings will be less than the theoretical value due to process variations and environment factors, such as voltage overhead compression, package losses, board losses, and other effects.

6.1.7 DRIVE DE-EMPHASIS

The Drive De-Emphasis Level field in the PHY Parameter 1 Register (offset 854h, bit[20:16], bit[25:21] and bit[30:26]) listed in Table 6-7 controls the de-emphasis base level. The settings and the corresponding values of the de-emphasis level are listed in Table 6-8, which can be configured by EEPROM or I2C settings.

Table 6-7 Drive De-Emphasis Base Level Register

| Register | De-Emphasis Condition |
|-------------------------|-----------------------|
| C_EMP_POST_GEN1_3P5_NOM | -3.5 db |
| C_EMP_POST_GEN2_3P5_NOM | -3.5 db |
| C_EMP_POST_GEN2_6P0_NOM | -6.0 db |

Table 6-8 Drive De-Emphasis Base Level Settings

| Setting | De-Emphasis (mV pd) | Setting | De-Emphasis (mV pd) | Setting | De-Emphasis (mV pd) |
|---------|---------------------|---------|---------------------|---------|---------------------|
| 00000 | 0.0 | 01011 | 68.75 | 10110 | 137.5 |
| 00001 | 6.25 | 01100 | 75.0 | 10111 | 143.75 |
| 00010 | 12.5 | 01101 | 81.25 | 11000 | 150.0 |
| 00011 | 18.75 | 01110 | 87.5 | 11001 | 156.25 |
| 00100 | 25.0 | 01111 | 93.75 | 11010 | 162.5 |
| 00101 | 31.25 | 10000 | 100.0 | 11011 | 168.75 |
| 00110 | 37.5 | 10001 | 106.25 | 11100 | 175.0 |
| 00111 | 43.75 | 10010 | 112.5 | 11101 | 181.25 |
| 01000 | 50.0 | 10011 | 118.75 | 11110 | 187.5 |
| 01001 | 56.25 | 10100 | 125.0 | 11111 | 194.75 |
| 01010 | 62.5 | 10101 | 131.25 | - | - |

Note:

1. Nominal levels. Actual levels will vary with temperature, voltage and board effects.
2. The maximum nominal amplitude of the output driver is 475 mV pd. Combined values of driver amplitude and de-emphasis greater than 475 mV pd should be avoided.
3. At higher amplitudes, actual swings will be less than the theoretical value due to process variations and environment factors, such as voltage overhead compression, package losses, board losses, and other effects.

6.1.8 TRANSMITTER ELECTRICAL IDLE LATENCY

After the last character of the PCI Express transmission, the output current is reduced, and a differential voltage of less than 20 mV with common mode of VTX-CM-DC is established within 20 UI. This delay time is programmable via Transmitter PHY Latency field in the PHY Parameter 2 Register (offset 858h, bit[3:0]), which can be configured by EEPROM or I2C settings.

6.2 DATA LINK LAYER (DLL)

The Data Link Layer (DLL) provides a reliable data transmission between two PCI Express points. An ACK/NACK protocol is employed to guarantee the integrity of the packets delivered. Each Transaction Layer Packet (TLP) is protected by a 32-bit LCRC for error detection. The DLL receiver performs LCRC calculation to determine if the incoming packet is corrupted in the serial link. If an LCRC error is found, the DLL transmitter would issue a NACK data link layer packet (DLLP) to the opposite end to request a re-transmission, otherwise an ACK DLLP would be sent out to acknowledge on reception of a good TLP.

In the transmitter, a retry buffer is implemented to store the transmitted TLPs whose corresponding ACK/NACK DLLP have not been received yet. When an ACK is received, the TLPs with sequence number equals to and smaller than that carried in the ACK would be flushed out from the buffer. If a NACK is received or no ACK/NACK is returned from the link partner

after the replay timer expires, then a replay mechanism built in DLL transmitter is triggered to re-transmit the corresponding packet that receives NACK or time-out and any other TLP transmitted after that packet.

Meanwhile, the DLL is also responsible for the initialization, updating, and monitoring of the flow-control credit. All of the flow control information is carried by DLLP to the other end of the link. Unlike TLP, DLLP is guarded by 16-bit CRC to detect if data corruption occurs.

In addition, the Media Access Control (MAC) block, which is consisted of LTSSM, multiple lanes de-skew, scrambler/de-scrambler, clock correction from inserting skip order-set, and PIPE-related control/status circuits, is implemented to interface physical layer with data link layer.

6.3 TRANSACTION LAYER RECEIVE BLOCK (TLP DECAPSULATION)

The receiving end of the transaction layer performs header information retrieval and TC/VC mapping (see section 5.5), and it validates the correctness of the transaction type and format. If the TLP is found to contain an illegal header or the indicated packet length mismatches with the actual packet length, then a Malformed TLP is reported as an error associated with the receiving port. To ensure end-to-end data integrity, a 32-bit ECRC is checked against the TLP at the receiver if the digest bit is set in header.

6.4 ROUTING

The transaction layer implements three types of routing protocols: ID-based, address-based, and implicit routing. For configuration reads, configuration writes, transaction completion, and user-defined messages, the packets are routed by their destination ID constituted of bus number, device number, and function number. Address routing is employed to forward I/O or memory transactions to the destination port, which is located within the address range indicated by the address field carried in the packet header. The packet header indicates the packet types including memory read, memory write, IO read, IO write, Message Signaling Interrupt (MSI) and user-defined message. Implicit routing is mainly used to forward system message transactions such as virtual interrupt line, power management, and so on. The message type embedded in the packet header determines the routing mechanism.

If the incoming packet cannot be forwarded to any other port due to a miss to hit the defined address range or targeted ID, this is considered as Unsupported Request (UR) packet, which is similar to a master abort event in PCI protocol.

6.5 TC/VC MAPPING

The 3-bit TC field defined in the header identifies the traffic class of the incoming packets. To enable the differential service, a TC/VC mapping table at destination port that is pre-programmed by system software or EEPROM pre-load is utilized to cast the TC labeled packets into the desired virtual channel. Note that TC0 traffic is mapped into VC0 channel by default. After the TC/VC mapping, the receive block dispatches the incoming request, completion, or data into the appropriate VC0 and VC1 queues.

6.6 QUEUE

In PCI Express, it defines six different packet types to represent request, completion, and data. They are respectively Posted Request Header (PH), Posted Request Data payload (PD), Non-Posted Request Header (NPH), Non-Posted Data Payload (NPD), Completion Header (CPLH) and Completion Data payload (CPLD). Each packet with different type would be put into a separate queue in order to facilitate the following ordering processor. Since NPD usually contains one DW, it can be merged with the corresponding NPH into a common queue named NPHD. Except NPHD, each virtual channel (VC0 or VC1)

has its own corresponding packet header and data queue. When only VC0 is needed in some applications, VC1 can be disabled and its resources assigned to VC0 by asserting VC1_EN (Virtual Channel 1 Enable) to low.

6.6.1 PH

PH queue provides TLP header spaces for posted memory writes and various message request headers. Each header space occupies sixteen bytes to accommodate 3 DW or 4 DW headers. There are two PH queues for VC0 and VC1 respectively.

6.6.2 PD

PD queue is used for storing posted request data. If the received TLP is of the posted request type and is determined to have payload coming with the header, the payload data would be put into PD queue. There are two PD queues for VC0 and VC1 respectively.

6.6.3 NPHD

NPHD queue provides TLP header spaces for non-posted request packets, which include memory read, IO read, IO write, configuration read, and configuration write. Each header space takes twenty bytes to accommodate a 3-DW header, s 4-DW header, s 3-WD header with 1-DW data, and a 4-DW header with 1-DW data. There is only one NPHD queue for VC0, since non-posted request cannot be mapped into VC1.

6.6.4 CPLH

CPLH queue provides TLP header space for completion packets. Each header space takes twelve bytes to accommodate a 3-DW header. Please note that there are no 4-DW completion headers. There are two CPLH queues for VC0 and VC1 respectively.

6.6.5 CPLD

CPLD queue is used for storing completion data. If the received TLP is of the completion type and is determined to have payload coming with the header, the payload data would be put into CPLD queue. There are two CPLD queues for VC0 and VC1 respectively.

6.7 TRANSACTION ORDERING

Within a VPPB, a set of ordering rules is defined to regulate the transactions on the PCI Express Switch including Memory, IO, Configuration and Messages, in order to avoid deadlocks and to support the Producer-Consumer model. The ordering rules defined in table 6-9 apply within a single Traffic Class (TC). There is no ordering requirement among transactions within different TC labels. Since the transactions with the same TC label are not allowed to map into different virtual channels, it implies no ordering relationship between the traffic in VC0 and VC1.

Table 6-9 Summary of PCI Express Ordering Rules

| Row Pass Column | Posted Request | Read Request | Non-posted Write Request | Read Completion | Non-posted Write Completion |
|-----------------|---------------------|------------------|--------------------------|------------------|-----------------------------|
| Posted Request | Yes/No ¹ | Yes ⁵ | Yes ⁵ | Yes ⁵ | Yes ⁵ |

| Row Pass Column | Posted Request | Read Request | Non-posted Write Request | Read Completion | Non-posted Write Completion |
|-----------------------------|---------------------|--------------|--------------------------|-----------------|-----------------------------|
| Read Request | No ² | Yes | Yes | Yes | Yes |
| Non-posted Write Request | No ² | Yes | Yes | Yes | Yes |
| Read Completion | Yes/No ³ | Yes | Yes | Yes | Yes |
| Non-Posted Write Completion | Yes ⁴ | Yes | Yes | Yes | Yes |

1. When the Relaxed Ordering Attribute bit is cleared, the Posted Request transactions including memory write and message request must complete on the egress bus of VPPB in the order in which they are received on the ingress bus of VPPB. If the Relaxed Ordering Attribute bit is set, the Posted Request is permitted to pass over other Posted Requests occurring before it.
2. A Read Request transmitting in the same direction as a previously queued Posted Request transaction must push the posted write data ahead of it. The Posted Request transaction must complete on the egress bus before the Read Request can be attempted on the egress bus. The Read transaction can go to the same location as the Posted data. Therefore, if the Read transaction were to pass the Posted transaction, it would return stale data.
3. When the Relaxed Ordering Attribute bit is cleared, a Read completion must “pull” ahead of previously queued posted data transmitting in the same direction. In this case, the read data transmits in the same direction as the posted data, and the requestor of the read transaction is on the same side of the VPPB as the completer of the posted transaction. The posted transaction must deliver to the completer before the read data is returned to the requestor. If the Relaxed Ordering Attribute bit is set, then a read completion is permitted to pass a previously queued Memory Write or Message Request.
4. Non-Posted Write Completions are permitted to pass a previous Memory Write or Message Request transaction. Such transactions are actually transmitting in the opposite directions and hence have no ordering relationship.
5. Posted Request transactions must be given opportunities to pass Non-posted Read and Write Requests as well as Completions. Otherwise, deadlocks may occur when some older bridges, which do not support delayed transactions are mixed with PCIe Switch in the same system. A fairness algorithm is used to arbitrate between the Posted Write queue and the Non-posted transaction queue

6.8 PORT ARBITRATION

Among multiple ingress ports, the port arbitration built in the egress port determines which incoming packets to be forwarded to the output port. The arbitration algorithm contains hardware fixed Round Robin, 128-phase Weighted Round-Robin and programmable 128-phase time-based WRR. The port arbitration is held within the same VC channel. It means that each port has two port arbitration circuitries for VC0 and VC1 respectively. At the upstream ports, in addition to the inter-port packets, the intra-port packet such as configurations completion would also join the arbitration loop to get the service from Virtual Channel 0.

6.9 VC ARBITRATION

After port arbitration, VC arbitration is executed among different VC channels within the same source. Three arbitration algorithms are provided to choose the appropriate VC: Strict Priority, Round Robin or Weighted Round Robin.

6.10 FLOW CONTROL

PCI Express employs Credit-Based Flow Control mechanism to make buffer utilization more efficient. The transaction layer transmitter ensures that it does not transmit a TLP to an opposite receiver unless the receiver has enough buffer space to accept the TLP. The transaction layer receiver has the responsibility to advertise the free buffer space to an opposite transmitter to avoid packet stale. In this Switch, each port has its own separate queues for different traffic types and the

credits are sent to data link layer on the fly. The data link layer compares the current available credits with the monitored ones and reports the updated credit to the counterpart. If no new credit is acquired, the credit reported is scheduled for every 30 us to prevent the link from entering retrain. On the other hand, the receiver at each egress port gets the usable credits from the opposite end in a link. The output port broadcasts them to all the other ingress ports to get packet transmission.

6.11 TRANSACTION LAYER TRANSMIT BLOCK (TLP ENCAPSULATION)

The transmit portion of transaction layer performs the following functions. They construct the all types of forwarded TLP generated from VC arbiter, respond with the completion packets when the local resource (i.e. configuration register) is accessed, and regenerate the message that terminates at receiver to RC if acting as an upstream port.

6.12 Non-Transparent Bridging (NT Mode Only)

Non-Transparent Bridging function translates Memory Address of the processor, and allows the process to appear as an endpoint. This function allows two separate Hosts to be connected together in a multi-host system, such as a multi-processor server or a control module with a built-in processor. Transactions in Base Address Space between two independent Address Spaces are translated and forwarded to each other.

When NT mode is enabled, one of the ports of the packet switch can be programmed to enter NT mode. While the port is in NT mode, the packet switch allows the isolation of address spaces, and the packet switch acts as an endpoint to the Host. The packet switch in NT mode terminates Type 0 Configuration Register packet. All incoming and outgoing memory-type transaction addresses are translated and forwarded from one domain to another using Base Address Registers (BARs). And the routing ID of the transaction packet is also translated between two host domains.

Registers that are used to notify the system of interrupts are called Interrupts Request (IRQ) registers. Messaging between processor domains achieved through the use of Scratchpad Registers, which both processors from separate process domains can access.

Only one port of the packet switch can be configured to operate in NT mode. NT mode is enabled and disabled by toggling the NT_ENABLE_L strapping pin.

6.12.1 Device Type Identification

The packet switch uses the Class Code Register (Offset 08h) in PCI Configuration Space Registers to identify its own Bridge Class type, and uses the PCI Express Capability register's Device/Port Type field (Offset 68h) to indicate the device/port type.

In Transparent Mode, the Class Code register returns the value 060400h to identify the packet switch as a PCI-to-PCI Bridge. The Device/Port Type field of the PCI Express Capability register (Offset 68h, bits [23:30]) returns 5h at upstream port and 6h at downstream port.

In Non-Transparent Mode, the Class Code register returns the value 068000h to identify the packet switch as an Other Bridge. The Device/Port Type field of the PCI Express Capability register returns 0h to indicate that it is a PCI Express endpoint device.

6.12.2 Intelligent Adaptor

The packet switch supports intelligent adaptor model in NT mode for multi-host systems. The model is implemented in PCI Express specification as in the established PCI specification. The NT bridge implements two Type 0 CSR Headers: Link

Interface and Virtual Interface. NT Port's Link Interface is connected to the System Host, and the Virtual Interface is connected to the internal virtual PCI bus.

In a multi-host system, the Local Host controls all Transparent Port Type 1 and NT Port Virtual Interface Type 0 functions, and the System Host controls only the NT Port Link Interface Type 0 function. The Address Translation between Link Interface and Virtual Interface routes Packets across the Host Domains.

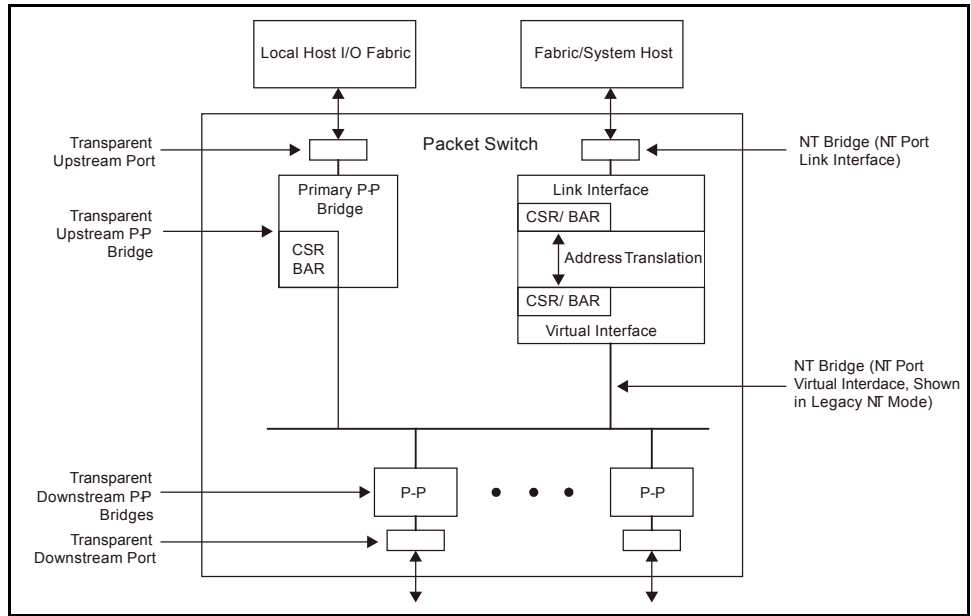


Figure 6-2 Intelligent Adaptor Architecture

6.12.3 Interrupts Request (IRQ) Registers

The Interrupts Request (IRQ) register sets are used to provide interrupt mechanism across the Non-Transparent port of the packet switch. The registers provide 16-bit interrupts signals in Virtual Interface and Link Interfaces through the following registers.

- Virtual Interface IRQ Set register (Offset C4Ch)
- Virtual Interface IRQ Clear register (Offset C50h)
- Virtual Interface IRQ Mask Set register (Offset C54h)
- Virtual Interface IRQ Mask Clear register (Offset C58h)
- Link Interface IRQ Set register (Offset C5Ch)
- Link Interface IRQ Clear register (Offset C60h)
- Link Interface IRQ Mask Set register (Offset C64h)
- Link Interface IRQ Mask Clear register (Offset C68h)

User software sets one or more bits of the Virtual or Link Interface IRQ Set register to signal that an interrupt is asserted on the Virtual or Link Interface of the Non-Transparent port. When bits of the IRQ Set register are set, the corresponding Mask Set register bits are cleared at the same time. User software sets one or more bits of the Virtual or Link Interface IRQ Clear register to signal that an interrupt is de-asserted on the Virtual or Link Interface of the Non-Transparent port. When bits of the IRQ Clear register are set, the corresponding Mask Clear register bits are cleared at the same time.

6.12.4 Scratchpad Registers

Hosts from both side of the Non-Transparent port of the packet switch are able to exchange messages through the implementation of the Scratchpad registers. These registers are readable and writable from both sides, and they provide a mechanism for inter-host communication of Control and Status information, or can be used as generic RW registers. Eight 32-bit register blocks (offset C6Ch to C8Bh) are allocated for Scratchpad registers.

6.12.5 NT Base Address Registers

The Base Address registers (BARs) are implemented to perform address translation in Memory-Map access. One set of BARs is used for Virtual Interface and one set of BARs for Link Interface. The BARs sets up the window size and type and defines the translation address.

BAR0 and BAR1 enable and disable and set up the Memory-Map access to NT-Port Configuration register space. BAR2, BAR3, BAR4, and BAR5 enable and disable and set up the access to other side of the NT-Port.

The BARs is enabled and disabled as indicated in the Memory Space Indicator bits. 32-bit and 64-bit memory window space is supported as indicated in the Memory Map Type bits. The Memory Base Address for memory-mapping is configured in the Base Address bits.

6.12.6 Routing ID Translation

The header of transaction layer packet contains Requester ID and/or Completer ID. The Requester/Completer ID is made up by bus number, device number and function number, and is also called the Routing ID. The routing ID represents an unique resource allocated to the device in a host domain. Since each host in different domain assigns routing ID independently, Routing ID translation is necessary for packets that transverse between link and virtual interface. The Virtual Port Registers (Offset D94h-DF3h) are implemented to support the translation of Routing ID between host domains using lookup tables.

6.13 Integrated DMA Engine

The packet switch has built-in Direct Memory Access (DMA) engine to transfer data between two memory locations. Two DMA engines are implemented for each of the upstream port (DMA_UP) and Non-Transparent port (DMA_NT). Each DMA engine supports two channels: Channel 0 and Channel 1.

Data transfer in the main CPU Memory Address domain is managed by DMA_UP engine while DMA_NT assists DMA_UP to manage data transfer across main and slave CPU Memory Address domains. Then DMA engines support both 32-bit and 64-bit Memory Address domains.

The DMA engine uses a 20-byte descriptor in 64-bit address domain to hold 64-bit source address and 64-bit destination address, 24-bit transfer size and 8-bit control/status bits. The DMA engine uses a 12-byte descriptor in 32-bit address domain to hold 32-bit source address and 32-bit destination address, 24-bit transfer size and 8-bit control/status bits.

The DMA engine supports prefetching function. Each channel of the DMA_UP and DMA_NT engines is capable of prefetching up to eight descriptors in 64-bit addressing mode and up to twelve descriptors in 32-bit addressing mode. Total of 128 descriptors are supported and can be shared in flexible configurations. Both the hardware and software have simultaneous access to the built-in Descriptor Ownership register simultaneously to prevent hardware descriptor status write-back.

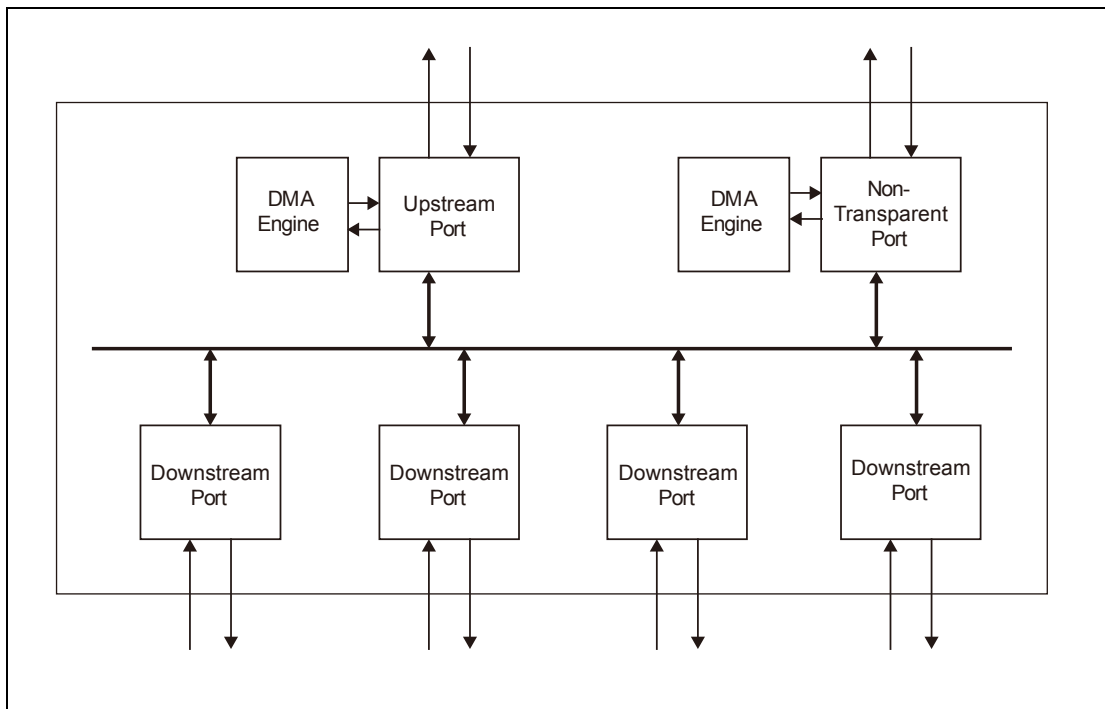


Figure 6-3 Block Diagram of Integrated DMA Engines in Packet Switch

The features of the packet switch’s DMA engines are listed below:

- Two DMA engines are implemented for upstream port (DMA_UP) and non-transparent port (DMA_NT)
- Each DMA engine supports two channels: Channel 0 and Channel 1
- DMA_UP manages the data transfer in main CPU address domain
- DMA_NT assists DMA_UP to manage data transfer across main and slave CPU address domains
- Supports 64-bit addressing domain
- 20-byte descriptor in 64-bit address domain
 - Holds 64-bit source address and 64-bit destination address
 - Holds 24-bit transfer size and 8-bit control/status bits
- 12-byte descriptor in 32-bit address domain
 - Holds 32-bit source address and 32-bit destination address
 - Holds 24-bit transfer size and 8-bit control/status bits
- Each channel of DMA_UP and DMA_NT engines is capable of prefetching
 - Up to 8 descriptors in 64-bit addressing mode
 - Up to 12 descriptors in 32-bit addressing mode
- Supports total of 128 descriptors shared by two channels in flexible configurations

Built-in Descriptors Ownership register is accessed by hardware and software simultaneously to prevent hardware descriptor status write-back.

6.13.1 Data Structure

The DMA descriptors reside in system memory, and they are structured in a ring configuration (see Figure below). The DMA engine fetches the descriptor pointer which points to the next available descriptor. The pointer in DMA engine is continuously advanced. When the last descriptor is reached, the pointer automatically jumps back to the first descriptor in the ring structure.

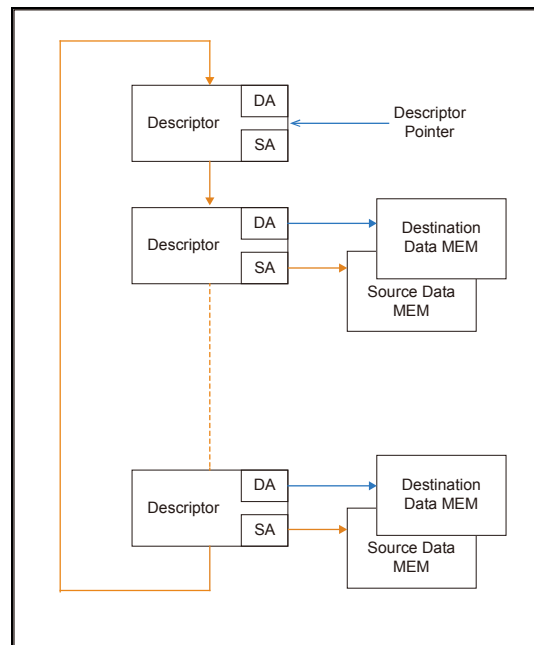


Figure 6-4 DMA Descriptor Ring Structure

DMA_UP engine’s descriptor holds two data pointers, which point to the addresses of source and destination memory blocks. The data are transferred from source to destination memory location as indicated by the addresses indicated by data pointers in the descriptors. In contrast, DMA_NT engine holds only one data pointer, which points to the source or destination location memory block, depending on the DMA traffic direction.

The tables below define the descriptor’s data structure in 32-bit and 64-bit systems.

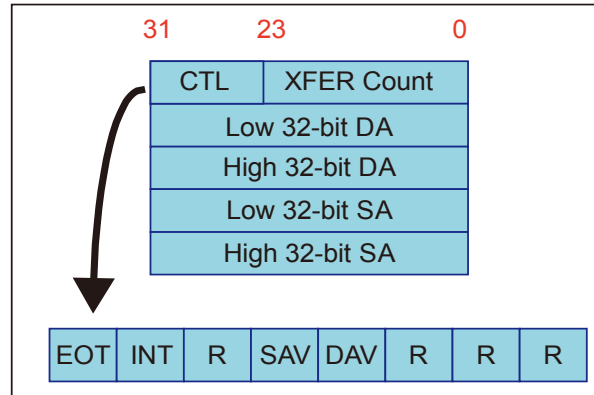


Figure 6-5 64-bit Descriptor Data Structure

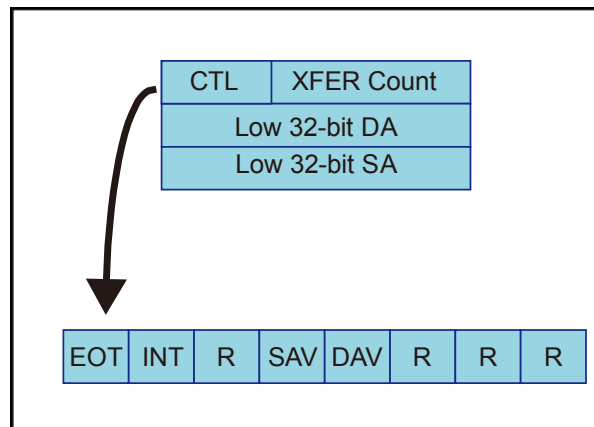


Figure 6-6 32-bit Descriptor Data Structure

Table 6-10 64-bit Descriptor Data Structure

| Bit | Name | Description |
|-----|----------|-------------------------------|
| 7 | EOT | End of Transfer |
| 6 | INT | Issue Interrupt when DMA done |
| 5 | Reserved | Reserved bit |
| 4 | SAV | Source Address Valid |
| 3 | DAV | Destination Address Valid |
| 2:0 | Reserved | Reserved bits |

Note: Source address bit 1-0 must zero

Table 6-11 32-bit Descriptor Data Structure

| Bit | Name | Description |
|-----|------|-------------------------------|
| 7 | EOT | End of Transfer |
| 6 | INT | Issue Interrupt when DMA done |

| Bit | Name | Description |
|-----|----------|---------------------------|
| 5 | Reserved | Reserved bit |
| 4 | SAV | Source Address Valid |
| 3 | DAV | Destination Address Valid |
| 2:0 | Reserved | Reserved bits |

Note: Source address bit 1-0 must zero

6.13.2 Traffic Models

The primary purpose of the DMA engine is to alleviate the workload of CPU to transfer of data from one memory location to another. The DMA engine of the Packet Switch supports the following three data transfer models.

Device-to-Processor Traffic Model

If DMA engines are not implemented, the Device-to-Processor Traffic requires a host CPU to issue read/write commands, transfer data, and process status information reported by the downstream devices. When DMA engines are implemented, they execute the process of data transfer and offload the CPU’s tasks. In this traffic model, only the DMA_UP engine is enabled. The source address points to the downstream device’s memory location and the destination address points to the main memory location. The figure below illustrates the Device-to-Processor Traffic model and the associated descriptor’s data structure.

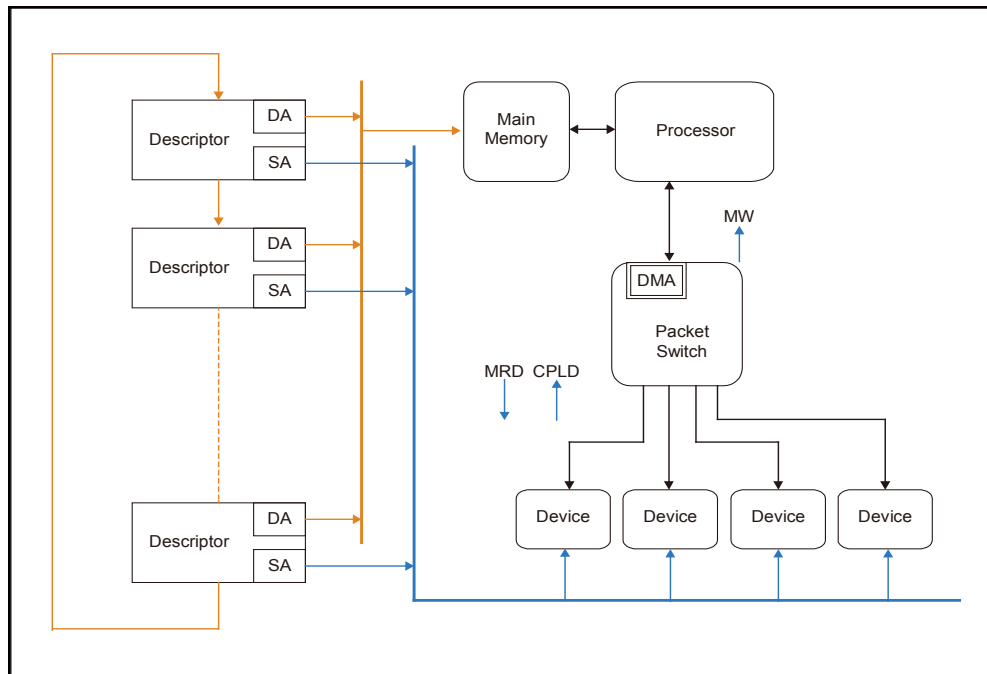


Figure 6-7 Status Information Collection Traffic Model

Peer-to-Peer Traffic Model

In Peer-to-Peer Traffic model, data transfer takes place between the downstream ports. Only the DMA_UP engine is enabled in this traffic model. The DMA_UP engine initiates and executes data transfer between two devices connected to the downstream ports without CPU’s intervention. The source address in the description points to one device’s memory location and the destination address points to another device’s. The data are read from the source device and written to the destination device directly. The figure below illustrates the Peer-to-Peer Traffic model and the associated descriptor’s data structure.

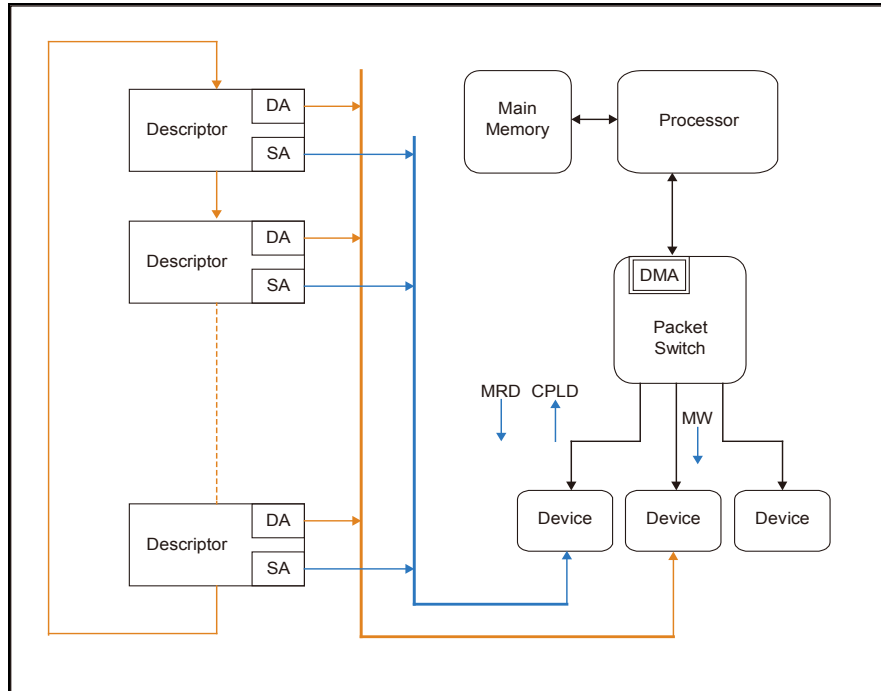


Figure 6-8 Peer-to-Peer Transfer Traffic Model

Inter-processor / Downstream Port to NT Port Traffic Model

In a multi-process application, data is routed from a downstream port to a NT port. The data traffic across processor domains typically consumes a large amount of CPU resources if DMA engines are not implemented. The CPU is responsible for issuing and executing read and write commands to transfer data. The DMA engine in the packet switch is implemented to offload the workload of CPU and move data from one processor domain to another on the behalf of CPU. In inter-processor traffic model, both of the DMA_UP and DMA_NT DMA engines are enabled at the same time to maintain their own descriptor data structures in different memory spaces.

In this traffic model, only one of the source or destination addresses in DMA_UP descriptor is valid, depending on the direction of the traffic. If DMA_UP engine is in the process of receiving data, only the destination address is valid. If DMA_UP engine is in the process of transmitting data, only the source address is valid. The DMA_NT engine's descriptor is used only for the purpose of validating the source pointer, which points to the location of data buffer. The DMA_NT descriptor also defines the SAV and DAV bits to determine the direction of the data traffic. The figure below illustrates the Inter-processor Traffic model and the associated descriptor's data structure.

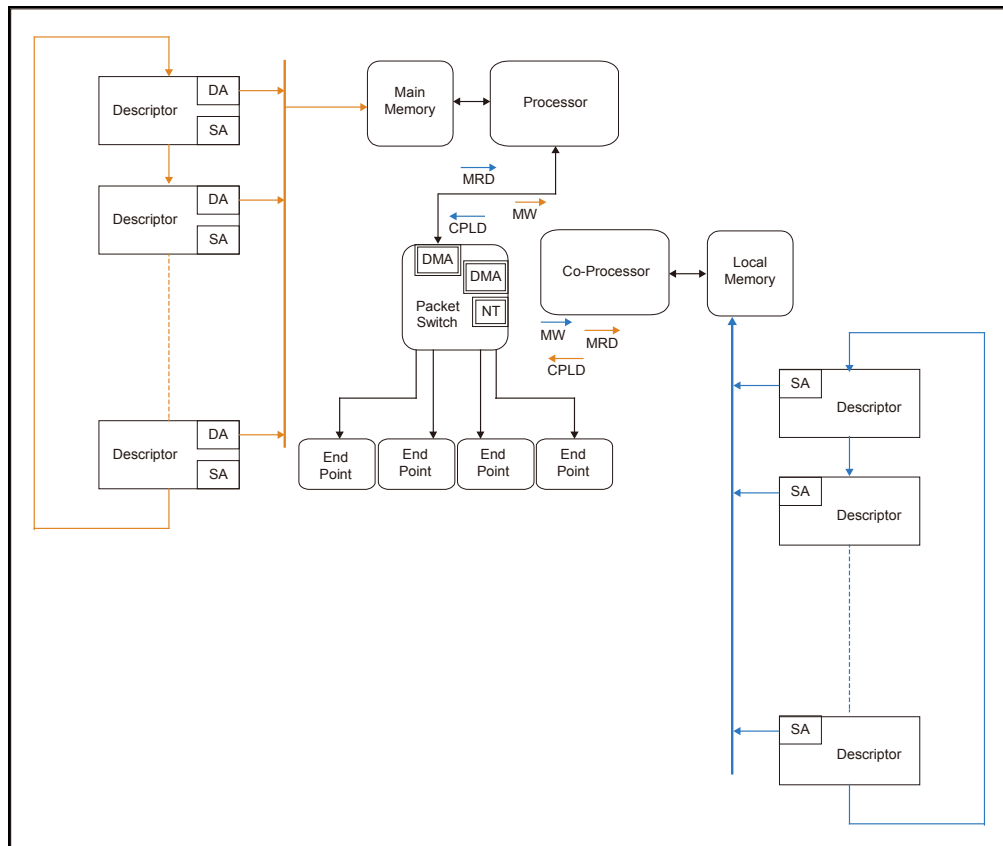


Figure 6-9 Inter-processor / Downstream Port to NT Port Traffic Model

6.13.3 Data Transfer Sequence

DMA engine moves data from one location to another without CPU's intervention. The CPU sets up DMA descriptor and initializes the DMA, and then is freed to perform other processes until it is interrupted to check the transfer status and to refresh the data content.

A typical DMA_UP engine operation sequence and its interaction with CPU and packet switch are described below.

1. CPU initializes the descriptor data structure in main memory.
2. CPU writes all "1" to the on-chip descriptor ownership register to notify DMA_UP engine the availability of descriptors.
3. CPU starts DMA_UP engine.
4. DMA pre-fetches 1 to 32 descriptors.
5. DMA starts processing the descriptors.
6. DMA issues read command to get data from the source location.
7. Completion data (CPLD) arrives at packet switch.
8. Packet switch converts CPLD into Post-Write data packet.
9. DMA issues write command to transmit data to the destination location.
10. More than one iteration from step 6 to step 9 may be required to complete transfer of one descriptor depending on the PCIe max read size, PCIe max payload size and whether the 4K boundary was crossed.
11. After finishing transfer of descriptor, the DMA clears the corresponding descriptor bit in the ownership register and interrupts CPU if INT bit is "1".

12. DMA_UP engine proceeds to the next descriptor and repeats the step 5 to 11.
13. CPU receives and processes interrupts, and then writes “1” to the corresponding bit of the processed descriptor in the ownership register if needed.
14. DMA_UP engine continuously polls the status of Channel X descriptor ownership register and pre-fetches the available descriptors depending on the setting of Channel X prefetch upper limit register.
15. If the EOT bit is set in the last processed descriptor, the data transfer is done. The transfer count will be updated by hardware. The count indicates the number of bytes moved in the last descriptor of a data transfer.

Note – Destination descriptor does not to set EOT. Only DMA sets EOT and updates byte count.

Both of DMA_UP and DMA_NT engines are involved to process inter-processor data transfer. The operation sequence of data moving from local CPU domain to main CPU domain and their interactions with local/main CPUs and packet switch are described below. The descriptor number and transfer size of descriptor are not necessary the same for DMA_UP and DMA_NT.

1. Main CPU and local CPU initialize the descriptors in main memory and local memory respectively.
2. Both CPUs write all “1” to their on-chip descriptor ownership registers to notify DMA_UP and DMA_NT engines the availability of descriptors.
3. Both CPUs start their own DMA engines.
4. DMA_UP and DMA_NT fetch their own 1 to 32 descriptors in advance.
5. DMA_NT and DMA_UP begin to process their own descriptors.
6. DMA_NT issues read command to get data from the source location pointed by SA address in DMA_NT descriptor.
7. Completion data (CPLD) arrives at the NT port of packet switch.
8. Packet switch converts CPLD into Post-Write data packet in packet switch.
9. DMA issues write command to send data to the destination location pointed by DA address in DMA_UP descriptor.
10. More than one iteration from step 6 to step 9 may be required to complete transfer of one descriptor depending on the PCIe max read size, PCIe max payload size and whether the 4K boundary was crossed.
11. After finishing the transfer process of descriptor, the DMA_NT or/and DMA_UP clears the corresponding descriptor bit in the ownership register and interrupts local CPU or/and main CPU if INT bit is “1”.
12. DMA_NT or/and DMA_UP proceed to their own next descriptor and repeat step 5 to 11.
13. Main or local CPU receives and processes interrupts, and then writes “1” to the corresponding bit of processed descriptor in the ownership register if needed.
14. DMA_UP or DMA_NT engine continuously polls the status of Channel X descriptor ownership register and prefetches the available descriptors depending on the setting of Channel X prefetch upper limit register.
15. If the EOT bit is set in the last processed descriptor of DMA_NT, the data transfer is done. The transfer count will be updated by hardware to the descriptor of DMA_UP. The count indicates the remaining bytes moved in the last descriptor of a data transfer. EOT bit will also be set by hardware to notify the software of main CPU the completion of current transfer

The operation sequence repeats through the ring of descriptors if not paused or aborted by CPU. The software is allowed to stop the DMA engine's operation. The software may stop the DMA engines to re-synchronize the event handling of software and hardware under certain conditions. The DMA transfer may be aborted for other reasons, such as when transfer of large amount of data is no longer required.

6.13.4 DMA Pause

The DMA engine can be paused by setting the “Pause” bit in the Channel X Control/Status Register. After the DMA engine is paused, the DMA engine completes the operation with the current active descriptors. After the completion of the current active descriptors, no descriptors will be processed and prefetched. The “Pause Done” bit in the Channel X Control/Status register will be set, and this will trigger an interrupt to the CPU, indicating that the pause action is completed. At this point, the system software may check the descriptor's ownership status register to determine the progress of the DMA transfer. The

software may clear both of the “Pause Done” and “Pause Control” bits of Channel X Control/Status register to resume DMA operation from the paused status.

6.13.5 DMA Abort

The DMA engine can be aborted by writing “1” to the “Abort” bit in the Channel X Control/Status register. After the DMA operation is aborted, the DMA engine drops the current active descriptor, flushes out all outstanding read commands, and discards all received completion data. After DMA engine drops the active descriptor, no more descriptors are processed and prefetched. The descriptor ownership registers are reset, and the ownership of all descriptors is assigned to the software. Then, the “Abort Done” bit in the Channel X Control/Status register is set to indicate the completion of abort action. The software may examine the descriptor ownership and transfer count status registers to determine the progress of the DMA aborted transfer and the number of the bytes that were transferred. The software may clear both of the “Abort Done” and “Abort Control” bits of Channel X Control/Status register to exit the DMA engine from Abort state. And then the software may attempt to start a new transfer from the current descriptor pointer.

6.13.6 DMA Stop

The DMA engine can be stopped by re-setting the “Start” bit in the Channel X Control/Status register. After the DMA operation is stopped, the current pointer is set to the descriptor ring base pointer. And the DMA engine flushes out all outstanding read commands and discards all completion data that were received. The DMA engine stops processing and prefetching any descriptors. The descriptor ownership registers are reset, and the ownership of all descriptors is assigned to the software. After the DMA engine is stopped, software is free to re-configure the channel mode, descriptor base pointer, and the number of descriptors in order to initialize new data transfers.

6.13.7 Descriptor Prefetch

The DMA engine implements the Descriptor Prefetch function to maximize the channel bandwidth usage. The Descriptor Prefetch function ensures that DMA engine never runs out of descriptors and lower the chance of having to wait for descriptors to arrive from memory in the process of data transfer. Each channel of both DMA engines can store up to 8 descriptors in 64-bit addressing system or 12 descriptors in 32-bit addressing system. The initial descriptor prefetch fills up the descriptor FIFO of each channel to reduce descriptor reading overhead. The prefetch upper limit should never exceed the descriptor ring size, or some of descriptors in descriptor ring will be fetched twice. After the first prefetch is completed, the DMA engine keeps polling the availability of descriptors, which are indicated in Channel X descriptor ownership register.

If new descriptors are found, the DMA engine will prefetch descriptors based on the setting of Channel X prefetch upper limit register. If the end of descriptor ring is reached, the DMA engine stops the read request for descriptors at the end of ring, and issues another read request, which starts at the descriptor ring base pointer.

6.14 Hot Plug Support

Note: *In this chapter, unless stated otherwise, “Hot Plug Controller” reference both the Parallel and Serial Hot Plug Controllers.*

Hot Plug capability allows board insertion and removal from a running system, without adversely affecting the system. Boards are typically inserted or removed to repair faulty boards or re-configure the system without system down time. Hot Plug capability allows systems to isolate faulty boards in the events of a failure.

Diodes PI7C9X2G1224GP can support three sets of 10 Hot Plug signals that can be associated to any three Transparent downstream Ports to implement Hot Plug function. If more than three Ports require Hot Plug signals, the additional Ports can use an external I2C I/O Expander (16-bit Diodes PI4IOE5V9555 per slot or 40-bit NXP PCA9698 per two slots), to provide the external signals.

Hot Plug signals are enabled, configured, and accessed through the **Slot Capability** and **Slot Status and Control** registers (offsets 7Ch and 80h, respectively), in each Port. Also, each Port's **Power Management Hot Plug User Configuration** register (offset 1E0h) provides additional Device-Specific configuration and control, for both Parallel and Serial Hot Plug implementations.

6.14.1 Hot Plug Controller Slot Power-Up/Down Sequence

If a Hot Plug-capable Transparent downstream Port is enabled, the Port's Hot Plug Controller can power-up that slot. This section describes how this process occurs.

6.14.1.1 Slot Power-Up Sequence

If a Hot Plug-capable Transparent downstream Port is connected to a slot, its associated Hot Plug Controller can power up that slot, with or without an external serial EEPROM. Hot Plug Controller sequencing is determined by the states of the following bits:

- **Slot Capability** register *Power Controller Present* bit (offset 7Ch[1])
- **Slot Capability** register *MRL Sensor Present* bit (offset 7Ch[2])
- **Slot Control** register *Power Controller Control* bit (offset 80h[10])

And the HP_MRL_x_L input state, if the *MRL Sensor Present* bit is Set. Hot Plug-configurable features are programmable only by the serial EEPROM and/or I²C.

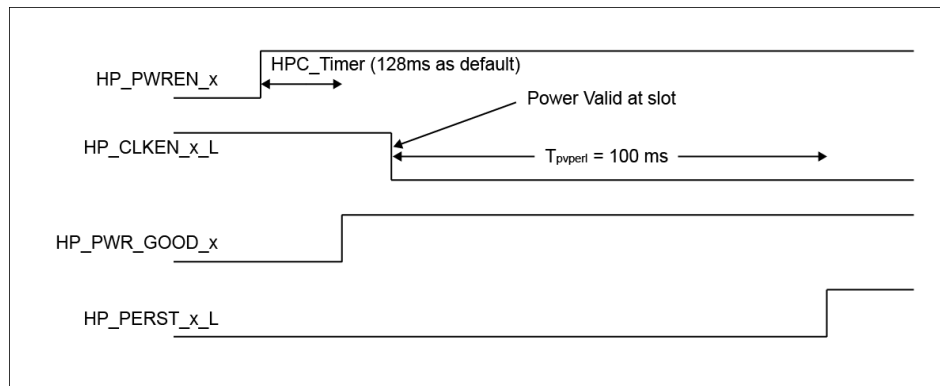


Figure 6-10 Slot Power-Up Timing When Power Controller Present Bit Is Set

6.14.1.2 Slot Power-Down Sequence

Software can power-down slots by Setting the *Power Controller Control* bit (offset 80h[10]). If the *MRL sensor Present* bit (offset 7Ch[2]) is Set, the Hot Plug Controller automatically powers down the slot if the MRL is open. Figure 6-11 illustrates the following power-down timing sequence for either event:

1. HP_PERST_x_L to the Port is asserted.

2. HP_CLKEN_x_L is de-asserted to the slot 100µs after HP_PERST_x_L is asserted.
3. HP_PWREN_x is de-asserted to the slot 100µs after HP_CLKEN_x_L is de-asserted.

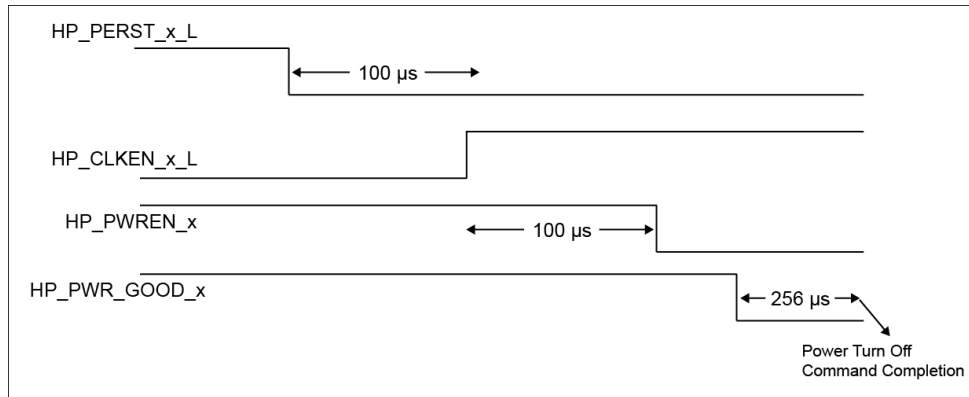


Figure 6-11 Hot Plug Automatic Power-Down Sequence

7 EEPROM INTERFACE AND I2C BUS

7.1 EEPROM INTERFACE

The EEPROM interface consists of four pins: EECK (EEPROM clock), EEDI (EEPROM serial data input), EEDO (EEPROM serial data output) and EECS (EEPROM chip select). The Switch supports 2-, or 3-byte address SPI EEPROM parts and automatically determines the appropriate addressing mode. The EEPROM is used to initialize a number of registers before enumeration. This is accomplished after PERST# is de-asserted, at which time the data from the EEPROM is loaded. The EEPROM interface is organized into a 16-bit base, and the Switch supplies an 8-bit EEPROM word address.

7.1.1 AUTO MODE EEPROM ACCESS

The Switch may access the EEPROM in a WORD format by utilizing the auto mode through a hardware sequencer. The EEPROM start-control, address, and read/write commands can be accessed through the configuration register. Before each access, the software should check the Autoload Status bit before issuing the next start.

7.1.2 EEPROM MODE AT RESET

During a reset, the Switch will automatically load the information/data from the EEPROM if the automatic load condition is met. The first offset in the EEPROM contains a signature. If the signature is recognized, the autoloading initiates right after the reset.

During the autoloading, the Bridge will read sequential words from the EEPROM and write to the appropriate registers. Before the Bridge registers can be accessed through the host, the autoloading condition should be verified by reading bit [4] offset 87Ch (EEPROM Autoload Status). The host access is allowed only after the status of this bit is set to '1' which indicates that the autoloading initialization sequence is complete.

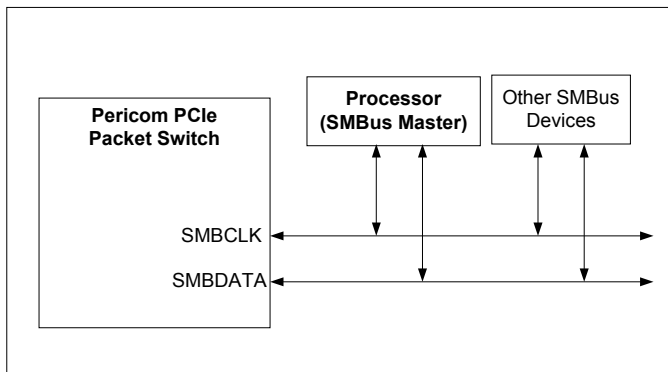
7.1.3 EEPROM SPACE ADDRESS MAP

| EEPROM Address | Value | Description |
|----------------|------------------|-----------------------------------------------------------------------------------------------------------------------------|
| 00h | 1516h | EEPROM signature |
| 02h | EEPROM_BYTE_SIZE | EEPROM size byte count |
| 04h | CFG_OFFSET_ADDR | 1 st Configuration Register Address Bit[9:0]: configuration register dword address Bit[15:10]: port number |
| 06h | CFG_LOW_DATA | 1 st Configuration Register Data (low word) |
| 08h | CFG_HIGH_DATA | 1 st Configuration Register Data (high word) |
| 0Ah | CFG_OFFSET_ADDR | 2 nd Configuration Register Address |
| 0Ch | CFG_LOW_DATA | 2 nd Configuration Register Data (low word) |
| 0Eh | CFG_HIGH_DATA | 2 nd Configuration Register Data (high word) |
| ... | ... | ... |
| FFFh | CFG_HIGH_DATA | Last Configuration Register Data (high word) |

7.2 SMBUS INTERFACE

The Packet Switch provides the System Management Bus (SMBus), a two-wire interface through which a simple device can communicate with the rest of the system. The SMBus interface on the Packet Switch is a bi-directional slave interface. It can receive data from the SMBus master or send data to the master. The interface allows full access to the configuration registers. A SMBus master, such as the processor or other SMBus devices, can read or write to every RW configuration register (read/write register). In addition, the RO and HwInt registers (read-only and hardware initialized registers) that can be auto-loaded by the EEPROM interface can also be read and written by the SMBus interface. This feature allows increases in the system expandability and flexibility in system implementation.

Figure 7-1 SMBus Architecture Implementation



The SMBus interface on the Packet Switch consists of one SMBus clock pin (SCL_I2C), a SMBus data pin (SDA_I2C), and 3 SMBus address pins (I2C_ADDR[2:0]). The SMBus clock pin provides or receives the clock signal. The SMBus data pin facilitates the data transmission and reception. Both of the clock and data pins are bi-directional. The SMBus address pins determine the address to which the Packet Switch responds to. The SMBus address pins generate addresses according to the following table:

Table 7-1 SMBus Address Pin Configuration

| BIT | SMBus Address |
|-----|---------------|
| 0 | I2C_ADDR[0] |
| 1 | I2C_ADDR[1] |
| 2 | I2C_ADDR[2] |
| 3 | 1 |
| 4 | 1 |
| 5 | 1 |
| 6 | 0 |

Software can change the SMBus Slave address, by programming the SMBus/I2C Control Register SMBus/I2C Device Address field.

The PI7C9X2G1224GP also supports Packet Error Checking and Packet Error Code (PEC) generation, as explained in the SMBus v2.0.

PI7C9X2G1224GP supports three commands:

- Block Write (command BEh) is used to write CFG registers
- Block Write (command BAh), followed by Block Read (command BDh), are used to read CFG registers
- Block Read - Block Write Process Call (commands BAh, CDh) can also be used to read CFG registers

7.2.1 SMBUS BLOCK WRITE

The Block Write command is used to write to the PI7C9X2G1224GP registers. General SMBus Block Writes are illustrated in Figure 7-2 and Figure 7-3. Table 7-2 explains the elements used in Figure 7-2 and Figure 7-3.

Figure 7-2 SMBus Block Write Command Format, to Write to a PI7C9X2G1224GP Register without PEC

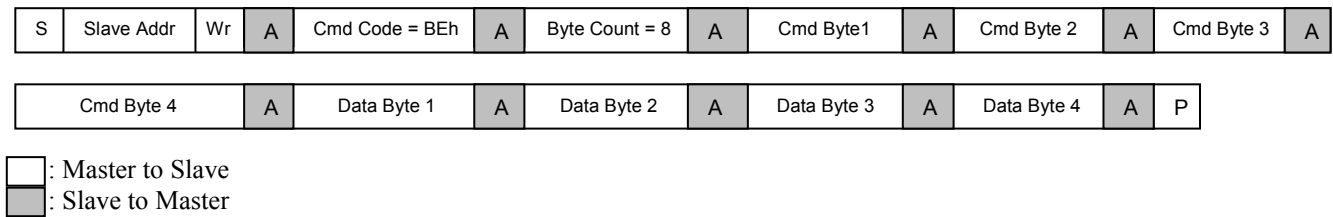
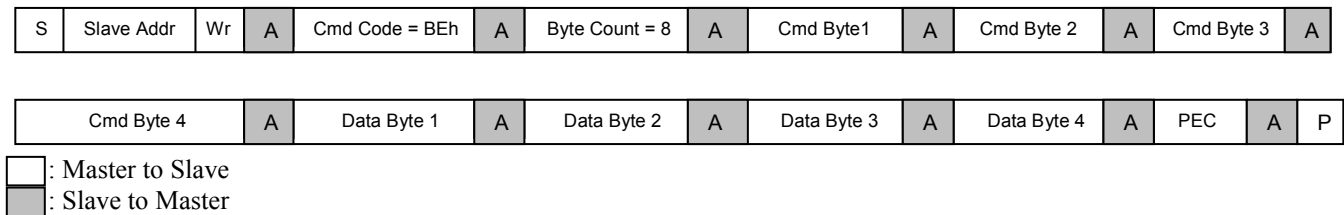


Figure 7-3 SMBus Block Write Command Format, to Write to a PI7C9X2G1224GP Register with PEC



Block Write transactions that are received with incorrect Cmd Code are NACKed, starting from the wrong byte setting, and including subsequent bytes in the packet. For example, if the Byte Count value is not 8, the PI7C9X2G1224GP NACKs the byte corresponding to the Byte Count value, as well as any Data bytes following within the same packet.

The byte after Data Byte 4, if present, is taken as the PEC byte, and if present, the PEC is checked. If a packet fails Packet Error Checking, the PI7C9X2G1224GP drops the packet (ignores the Write), and returns NACK for the PEC byte, to the SMBus Master. Packet Error Checking can be disabled, by setting the SMBus/I²C Control Register PEC Check Disable bit. The Byte Count value, by definition, does not include the PEC byte.

Table 7-2 Bytes for SMBus Block Write

| Field (Byte) On Bus | Bit(s) | Value/ Description |
|---------------------|--------|--------------------------------------------------------------------------------------------------------------------------------------------|
| S | 1 | START condition |
| P | 1 | STOP condition |
| A | 1 | Acknowledge (this bit position may be 0 for an ACK or 1 for a NACK) |
| Command Code | 7:0 | BEh for Block Write |
| Byte Count | 7:0 | 08h = 8 bytes to follow (4 Command and 4 Data bytes). The PEC byte is not counted. |
| Command Byte 1 | 7:3 | Reserved |
| | 2:0 | Command 011b = Write register 100b = Read register |
| | 7:4 | Reserved |
| Command Byte 2 | 3:0 | Port Select[4:1] 2 nd Command byte, bits [3:0], and 3 rd Command byte, bit 7, combine to form a 5-bit Port |

| Field (Byte) On Bus | Bit(s) | Value/ Description | | | | | | | | | | |
|---------------------|--------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------------|---|------------------------------------------------------------------|---|-------------------------------------------------------------------|---|--------------------------------------------------------------------|---|--------------------------------------------------------------------|
| | | Select. | | | | | | | | | | |
| Command Byte 3 | 7 | Port Select[0] 2nd Command byte, bits [3:0], and 3rd Command byte, bit 7, combine to form a 5-bit Port Select. Port Select[4:0] is used to select Port to access. 00h – Port 0 01h – Port 1 or NT Port Link Interface (if NT mode is enabled) 02h ~ 0Fh – Port 2 ~ Port 15 10h for NT Port Virtual Interface 11h – 1Fh are reserved | | | | | | | | | | |
| | 6 | Reserved | | | | | | | | | | |
| | 5:2 | Byte Enable <table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>2</td> <td>Byte Enable for Data Byte 4 (PI7C9X2G1224GP register bits [7:0])</td> </tr> <tr> <td>3</td> <td>Byte Enable for Data Byte 3 (PI7C9X2G1224GP register bits [15:8])</td> </tr> <tr> <td>4</td> <td>Byte Enable for Data Byte 2 (PI7C9X2G1224GP register bits [23:16])</td> </tr> <tr> <td>5</td> <td>Byte Enable for Data Byte 1 (PI7C9X2G1224GP register bits [31:24])</td> </tr> </tbody> </table> 0 = Corresponding PI7C9X2G1224GP register byte will not be modified 1 = Corresponding PI7C9X2G1224GP register byte will be modified | Bit | Description | 2 | Byte Enable for Data Byte 4 (PI7C9X2G1224GP register bits [7:0]) | 3 | Byte Enable for Data Byte 3 (PI7C9X2G1224GP register bits [15:8]) | 4 | Byte Enable for Data Byte 2 (PI7C9X2G1224GP register bits [23:16]) | 5 | Byte Enable for Data Byte 1 (PI7C9X2G1224GP register bits [31:24]) |
| | Bit | Description | | | | | | | | | | |
| 2 | Byte Enable for Data Byte 4 (PI7C9X2G1224GP register bits [7:0]) | | | | | | | | | | | |
| 3 | Byte Enable for Data Byte 3 (PI7C9X2G1224GP register bits [15:8]) | | | | | | | | | | | |
| 4 | Byte Enable for Data Byte 2 (PI7C9X2G1224GP register bits [23:16]) | | | | | | | | | | | |
| 5 | Byte Enable for Data Byte 1 (PI7C9X2G1224GP register bits [31:24]) | | | | | | | | | | | |
| 1:0 | PI7C9X2G1224GP Register Address [11:10] | | | | | | | | | | | |
| Command Byte 4 | 7:0 | PI7C9X2G1224GP Register Address [9:2] Note: Address bits[1:0] are fixed to 0. | | | | | | | | | | |
| Data Byte 1 | 7:0 | Data write to register bits [31:24] | | | | | | | | | | |
| Data Byte 2 | 7:0 | Data write to register bits [23:16] | | | | | | | | | | |
| Data Byte 3 | 7:0 | Data write to register bits [15:8] | | | | | | | | | | |
| Data Byte 4 | 7:0 | Data write to register bits [7:0] | | | | | | | | | | |
| PEC | 7:0 | Packet Error Code | | | | | | | | | | |

Table 7-3 is a sample to write SSID/SSVID register (offset F8h) in Port 1. The register value is 1234_5678h, with all bytes enabled, and without PEC. The default SMBus Address is 1101000b.

Table 7-3 Sample SMBus Block Write Byte Sequence

| Byte Number | Byte Type | Value | Description |
|-------------|----------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 | Address | 70h | Bits [7:1] for the PI7C9X2G1224GP default Slave address of 38h, with bit 0 Cleared to indicate a Write. |
| 2 | Command Code | BEh | Command Code for register Write, using a Block Write |
| 3 | Byte Count | 08h | Byte Count. Four Command Bytes and Four Data Bytes |
| 4 | Command Byte 1 | 03h | For Write command |
| 5 | Command Byte 2 | 00h | Bits [3:0] - Port Select [4:1] (for Port 1) |
| 6 | Command Byte 3 | BCh | Bit 7 is Port Select[0] Bit 6 is reserved Bits [5:2] are the for Byte Enables; all are active Bits [1:0] are register Address bits [11:10] |
| 7 | Command Byte 4 | 3Eh | PI7C9X2G1224GP Register Address bits [9:2] (for offset F8h) |
| 8 | Data Byte 1 | 12h | Data Byte for register bits [31:24] |
| 9 | Data Byte 2 | 34h | Data Byte for register bits [23:16] |
| 10 | Data Byte 3 | 56h | Data Byte for register bits [15:8] |
| 11 | Data Byte 4 | 78h | Data Byte for register bits[7:0] |

7.2.2 SMBUS BLOCK READ

A Block Read command is used to read PI7C9X2G1224GP CFG registers. Similar to CFG register Reads using I²C, a SMBus Write sequence must first be performed to select the register to read, followed by a SMBus Read of the corresponding register. There are two ways a PI7C9X2G1224GP register can be read:

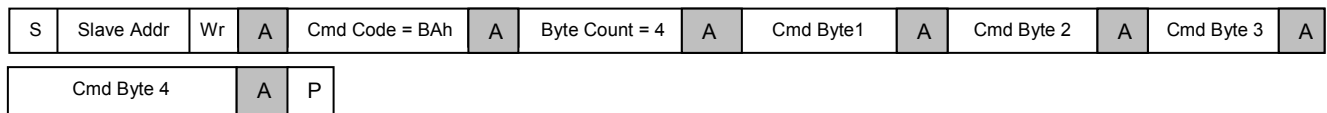
- Use a Block Write, followed by a Block Read. The Block Write sets up the parameters including Port Number, register address and Byte Enables, and the Block Read performs the actual Read operation.

- Use a Block Read - Block Write Process Call. This command is defined by the SMBus v2.0, and performs a Block Write and Block Read, using a single command. The Block Write portion of the message sets up the register to be read, and then a repeated START followed by the Block Read portion of the message returns the register data specified by the Block Write

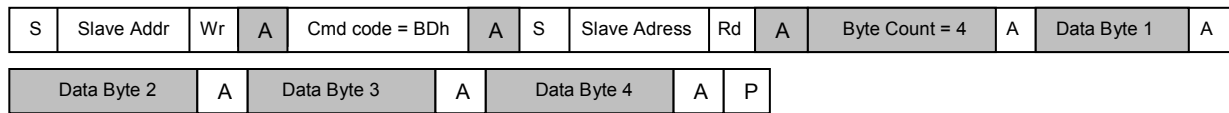
The PI7C9X2G1224GP always NACKs any incorrect command sequences, starting with the wrong Byte. Upon receiving the Block Read command, the PI7C9X2G1224GP returns a PEC to the Master, if after the 4th byte of register data, the Master still requests one more Byte. As a Slave, the PI7C9X2G1224GP recognizes the end of the Master's Read cycle, by observing the Master's NACK response for the last Data Byte transmitted by the PI7C9X2G1224GP.

Incorrect command sequences are always NACK, starting with the byte that is incorrect. (Refer to Table 7-4.) On the Block Read command, a PEC is returned to the Master, if after the 4th byte of CSR data, the return Master still requests for one additional byte. As a Slave, the PI7C9X2G1224GP will know the end of the Master Read cycle, by observing the NACK for the last byte read from the Master.

Figure 7-4 SMBus Block Write to Set up Read, and Resulting Read that Returns CFG Register Value



A Block Write to set up Read



A Block Read which returns CFG Register Value

□ : Master to Slave
 ■ : Slave to Master

Table 7-4 Bytes for SMBus Block Read

| Field (Byte) On Bus | Bit(s) | Value/ Description |
|---------------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| S | 1 | START condition |
| P | 1 | STOP condition |
| A | 1 | Acknowledge (this bit position may be 0 for an ACK or 1 for a NACK) |
| Command Code | 7:0 | BAh , to set up Read, using Block Writes |
| Byte Count | 7:0 | 04h , 4 Command bytes |
| Command Byte 1 | 7:3 | Reserved |
| | 2:0 | Command 011b = Write register 100b = Read register |
| Command Byte 2 | 7:4 | Reserved |
| | 3:0 | Port Select[4:1] 2 nd Command byte, bits [3:0], and 3 rd Command byte, bit 7, combine to form a 5-bit Port Select. |
| | 7 | Port Select[0] 2 nd Command byte, bits [3:0], and 3 rd Command byte, bit 7, combine to form a 5-bit Port Select. Port Select[4:0] is used to select Port to access. 00h – Port 0 01h – Port 1 or NT Port Link Interface (if NT mode is enabled) 02h ~ 0Fh – Port 2 ~ Port 15 10h for NT Port Virtual Interface 11h – 1Fh are reserved |
| | 6 | Reserved |
| | 5:2 | Byte Enable |

| Field (Byte) On Bus | Bit(s) | Value/ Description |
|---------------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Command Byte 3 | | Bit Description 2 Byte Enable for Data Byte 4 (PI7C9X2G1224GP register bits [7:0]) 3 Byte Enable for Data Byte 3 (PI7C9X2G1224GP register bits [15:8]) 4 Byte Enable for Data Byte 2 (PI7C9X2G1224GP register bits [23:16]) 5 Byte Enable for Data Byte 1 (PI7C9X2G1224GP register bits [31:24]) 0 = Corresponding PI7C9X2G1224GP register byte will not be modified 1 = Corresponding PI7C9X2G1224GP register byte will be modified |
| | 1:0 | PI7C9X2G1224GP Register Address [11:10] |
| Command Byte 4 | 7:0 | PI7C9X2G1224GP Register Address [9:2] Note: Address bits[1:0] are fixed to 0. |
| | 7:0 | BDh for Block Read |
| Command Code | 7:0 | BDh for Block Read |
| Data Byte 1 | 7:0 | Return value for CFG register bits [31:24] |
| Data Byte 2 | 7:0 | Return value for CFG register bits [23:16] |
| Data Byte 3 | 7:0 | Return value for CFG register bits [15:8] |
| Data Byte 4 | 7:0 | Return value for CFG register bits [7:0] |

Table 7-5, Table 7-6, Table 7-7 and Table 7-8 are a sample to Read SSID/SSVID register (offset F8h) in Port 1. The register value is 0000_0000h, with all bytes enabled, and without PEC. The default SMBus Address is 1101000b.

Table 7-5 SMBus Block Write Portion

| Byte Number | Byte Type | Value | Description |
|-------------|----------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 | Address | 70h | Bits [7:1] for the PI7C9X2G1224GP default Slave address of 38h, with bit 0 Cleared to indicate a Write. |
| 2 | Command Code | BAh | Command Code for register Write, using a Block Write |
| 3 | Byte Count | 04h | Byte Count. Four Command Bytes |
| 4 | Command Byte 1 | 04h | For Read command |
| 5 | Command Byte 2 | 00h | Bits [3:0] - Port Select [4:1] (for Port 1) |
| 6 | Command Byte 3 | BCh | Bit 7 is Port Select[0] Bit 6 is reserved Bits [5:2] are the for Byte Enables; all are active Bits [1:0] are register Address bits [11:10] |
| 7 | Command Byte 4 | 3Eh | PI7C9X2G1224GP Register Address bits [9:2] (for offset F8h) |

Table 7-6 SMBus Block Read Portion

| Byte Number | Byte Type | Value | Description |
|-------------|-------------------------|-------|-------------------------------------------------------------------------------------------------------------------|
| 1 | Address | 70h | Bits [7:1] value for the PI7C9X2G1224GP Slave address of 38h, with bit 0 Cleared to indicate to indicate a Write. |
| 2 | Block Read Command Code | BDh | Command code for Block Read of PI7C9X2G1224GP registers. |

Table 7-7 SMBus Read Command following Repeat START from Master

| Byte Number | Byte Type | Value | Description |
|-------------|-----------|-------|--------------------------------------------------------------------------------------------------|
| 1 | Address | 71h | Bits [7:1] value for the PI7C9X2G1224GP Slave address of 38h, with bit 0 Set to indicate a Read. |

Table 7-8 SMBus Return Bytes

| Byte Number | Byte Type | Value | Description |
|-------------|-------------|-------|------------------------|
| 1 | Byte Count | 04h | Four Bytes in register |
| 2 | Data Byte 1 | 00h | Register data [31:24] |
| 3 | Data Byte 2 | 00h | Register data [23:16] |
| 4 | Data Byte 3 | 00h | Register data [15:8] |
| 5 | Data Byte 4 | 00h | Register data [7:0] |

7.2.3 CSR READ, USING SMBUS BLOCK READ – BLOCK WRITE PROCESS CALL

A general SMBus Block Read - Block Write Process Call sequence is illustrated in Figure 7-5. Alternatively, a general SMBus Block Read - Block Write Process Call with PEC sequence is illustrated in Figure 7-6.

Using this command, the register to be read can be set up and read back with one SMBus cycle (a transaction with a START and ending in STOP). There is no STOP condition before the repeated START condition. The command format for the Block Write part of this command has the same sequence as in Table 7-5, except that the Command Code changes to CDh, as illustrated below. Other Bytes remain the same as used in the sequence for SMBus Block Write followed by Block Read. Table 7-9 lists the Command format for Block Read.

Figure 7-5 CSR Read Operation Using SMBus Block Read – Block Write Process Call

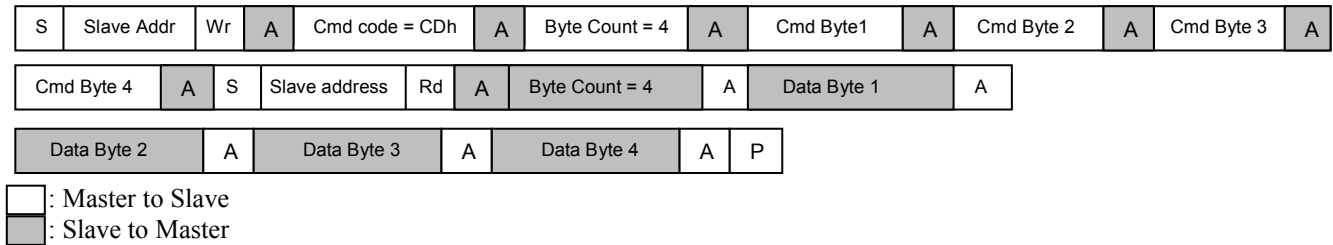


Figure 7-6 CSR Read Operation Using SMBus Block Read – Block Write Process Call with PEC

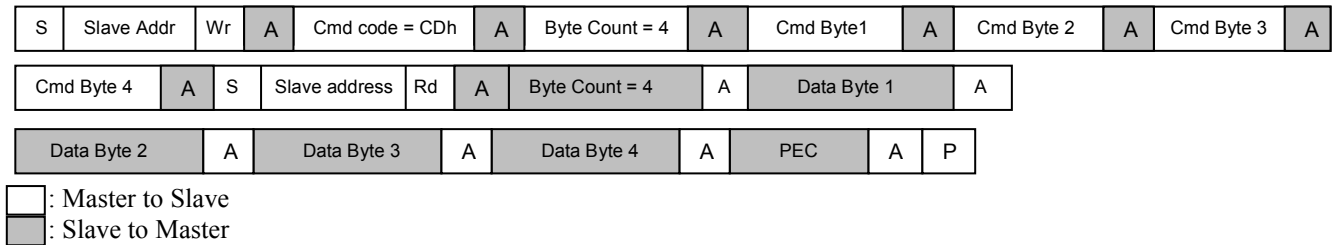


Table 7-9 Command Format for SMBus Block Read

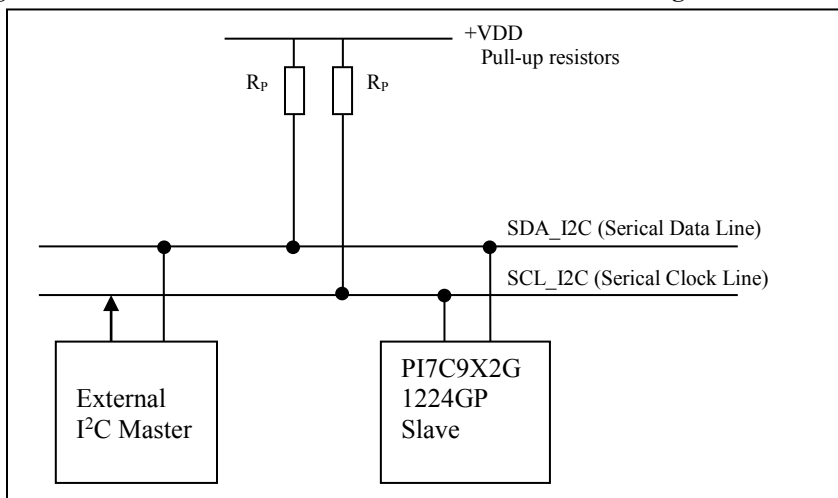
| Field (Byte) On Bus | Bit(s) | Value/Description |
|---------------------|--------|----------------------------------------|
| Command Code | 7:0 | CDh for Block Read (Process Call Read) |

7.3 I²C SLAVE INTERFACE

Inter-Integrated Circuit (I²C) is a bus used to connect Integrated Circuits (ICs). Multiple ICs can be connected to an I²C Bus, and I²C devices that have I²C mastering capability can initiate a Data transfer. I²C is used for Data transfers between ICs at relatively low rates (100 Kbps), and is used in a variety of applications. For further details regarding I²C Buses, refer to the *I²C Bus v2.1*.

The PI7C9X2G1224GP is an I²C Slave. Slave operations allow the PI7C9X2G1224GP Configuration registers to be read from or written to by an I²C Master, external from the device. I²C is a sideband mechanism that allows the device Configuration registers to be programmed, read from, or written to, independent of the PCI Express upstream Link.

Figure 7-7 Standard Devices to I²C Bus Connection Block Diagram



The I²C interface on the Packet Switch consists of a I²C clock pin (SCL_I2C), a I²C data pin (SDA_I2C), and 3 I²C address pins (I2C_ADDR[2:0]). The I²C clock pin provides or receives the clock signal. The I²C data pin facilitates the data transmission and reception. Both of the clock and data pins are bi-directional. The I²C address pins determine the address to which the Packet Switch responds to. The I²C address pins generate addresses according to the following table:

Table 7-10 I²C Address Pin Configuration

| BIT | I2C Address |
|-----|-------------|
| 0 | I2C_ADDR[0] |
| 1 | I2C_ADDR[1] |
| 2 | I2C_ADDR[2] |
| 3 | 1 |
| 4 | 1 |
| 5 | 1 |
| 6 | 0 |

Software can change the I²C Slave address, by programming the I²C Control Register I²C Device Address field.

7.3.1 I²C REGISTER WRITE ACCESS

The PI7C9X2G1224GP Configuration registers can be read from and written to, based upon I²C register Read and Write operations, respectively. An I²C Write packet consists of Address Phase bytes and Command Phase bytes, followed by one to four additional I²C Data bytes. Table 7-11 defines mapping of the I²C Data bytes to the Configuration register Data bytes.

The I²C packet starts with the S (START condition) bit. Data bytes are separated by the A (Acknowledge Control Packet (ACK)) or N (Negative Acknowledge (NAK)) bit. The packet ends with the P (STOP condition) bit.

If the Master generates an invalid command, the targeted PI7C9X2G1224GP register is not modified.

The PI7C9X2G1224GP considers the 1st Data byte of the 4-byte Data phase, following the four Command bytes in the Command phase, as register Byte 3 (bits [31:24]). The next three Data bytes access register Bytes 2 through 0, respectively. Four Data bytes are required, regardless of the Byte Enable Settings in the Command phase. The Master can then generate either a STOP condition (to finish the transfer) or a repeated START condition (to start a new transfer). If the I²C Master sends more than the four Data bytes (violating PI7C9X2G1224GP protocol), further details regarding I²C protocol, the PI7C9X2G1224GP returns a NAK for the extra Data byte(s).

Table 7-12 describes each I²C Command byte for Write access. In the packet described in Figure 7-8, Command Bytes 0 through 3 for Writes follow the format specified in Table 7-12.

Table 7-11 I²C Register Write Access

| I ² C Data Byte Order | PCI Express Configuration Register Byte |
|----------------------------------|-----------------------------------------|
| 0 | Written to register Byte 3 |
| 1 | Written to register Byte 2 |
| 2 | Written to register Byte 1 |
| 3 | Written to register Byte 0 |

Table 7-12 I²C Command Format for Write Access

| Byte | Bit(s) | Description | | | | | | | | | | |
|---------------------|--------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------------|---|------------------------------------------------------------------|---|-------------------------------------------------------------------|---|--------------------------------------------------------------------|---|--------------------------------------------------------------------|
| 1 st (0) | 7:3 | Reserved | | | | | | | | | | |
| | 2:0 | Command 011b = Write register | | | | | | | | | | |
| 2 nd (1) | 7:4 | Reserved | | | | | | | | | | |
| | 3:0 | Port Select[4:1] 2 nd Command byte, bits [3:0], and 3 rd Command byte, bit 7, combine to form a 5-bit Port Select. | | | | | | | | | | |
| 3 rd (2) | 7 | Port Select[0] 2 nd Command byte, bits [3:0], and 3 rd Command byte, bit 7, combine to form a 5-bit Port Select. Port Select[4:0] is used to select Port to access. 00h – Port 0 01h – Port 1 or NT Port Link Interface (if NT mode is enabled) 02h ~ 0Bh – Port 2 ~ Port 11 10h for NT Port Virtual Interface 0Ch – 1Fh are reserved | | | | | | | | | | |
| | 6 | Reserved | | | | | | | | | | |
| | 5:2 | Byte Enable <table border="0"> <thead> <tr> <th>Bit</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>2</td> <td>Byte Enable for Data Byte 4 (PI7C9X2G1224GP register bits [7:0])</td> </tr> <tr> <td>3</td> <td>Byte Enable for Data Byte 3 (PI7C9X2G1224GP register bits [15:8])</td> </tr> <tr> <td>4</td> <td>Byte Enable for Data Byte 2 (PI7C9X2G1224GP register bits [23:16])</td> </tr> <tr> <td>5</td> <td>Byte Enable for Data Byte 1 (PI7C9X2G1224GP register bits [31:24])</td> </tr> </tbody> </table> 0 = Corresponding PI7C9X2G1224GP register byte will not be modified 1 = Corresponding PI7C9X2G1224GP register byte will be modified | Bit | Description | 2 | Byte Enable for Data Byte 4 (PI7C9X2G1224GP register bits [7:0]) | 3 | Byte Enable for Data Byte 3 (PI7C9X2G1224GP register bits [15:8]) | 4 | Byte Enable for Data Byte 2 (PI7C9X2G1224GP register bits [23:16]) | 5 | Byte Enable for Data Byte 1 (PI7C9X2G1224GP register bits [31:24]) |
| | Bit | Description | | | | | | | | | | |
| 2 | Byte Enable for Data Byte 4 (PI7C9X2G1224GP register bits [7:0]) | | | | | | | | | | | |
| 3 | Byte Enable for Data Byte 3 (PI7C9X2G1224GP register bits [15:8]) | | | | | | | | | | | |
| 4 | Byte Enable for Data Byte 2 (PI7C9X2G1224GP register bits [23:16]) | | | | | | | | | | | |
| 5 | Byte Enable for Data Byte 1 (PI7C9X2G1224GP register bits [31:24]) | | | | | | | | | | | |
| 1:0 | PI7C9X2G1224GP Register Address [11:10] | | | | | | | | | | | |
| 4 th (3) | 7:0 | PI7C9X2G1224GP Register Address [9:2] Note: Address bits[1:0] are fixed to 0. | | | | | | | | | | |

Figure 7-8 I²C Write Packet

I²C Write Packet Address Phase Byte

| Address Cycle | | | |
|---------------|---------------------|-----------------------------|---------|
| START | 7654321 | 0 | ACK/NAK |
| S | Slave Address [7:1] | Read/Write Bit 0 = Write | A |

I²C Write Packet Command Phase Byte

| Command Cycle | | | | | | | |
|----------------|---------|----------------|---------|----------------|---------|----------------|---------|
| 76543210 | ACK/NAK | 76543210 | ACK/NAK | 76543210 | ACK/NAK | 76543210 | ACK/NAK |
| Command Byte 0 | A | Command Byte 1 | A | Command Byte 2 | A | Command Byte 3 | A |

I²C Write Packet Data Phase Byte

| Write Cycle | | | | | | | | |
|-----------------|---------|-----------------|---------|-----------------|---------|-----------------|---------|------|
| 76543210 | ACK/NAK | 76543210 | ACK/NAK | 76543210 | ACK/NAK | 76543210 | ACK/NAK | STOP |
| Register Byte 3 | A | Register Byte 2 | A | Register Byte 1 | A | Register Byte 0 | A | P |

The following tables illustrate a sample I²C packet for writing the PI7C9X2G1224GP SSID/SSVID register (offset F8h) for Port 0, with data 1234_5678h.

Note: The PI7C9X2G1224GP has a default I²C Slave address [6:0] value of 38h, with the I²C_ADDR[2:0] input having a value of 000. The byte sequence on the I²C Bus, as listed in the following tables, occurs after the START and before the STOP bits, by which the I²C Master frames the transfer.

Figure 7-9 I²C Register Write Access Example

I²C Register Write Access Example – Address Cycle

| Phase | Value | Description |
|---------|-------|--------------------------------------------------------------------------------------------------------|
| Address | 70h | Bits [7:1] for PI7C9X2G1224GP I ² C Slave Address (38h) with last bit (bit 0) for Write = 0 |

I²C Register Write Access Example – Command Cycle

| Byte | Value | Description |
|------|----------------|-----------------------------------------------------------------------------------------------------------------------------|
| 0 | 03h | [7:3] Reserved [2:0] Command, 011b = Write register |
| 1 | 00h for Port 0 | [7:4] Reserved [3:0] Port Select[4:1] |
| 2 | 3Ch for Port 0 | [7] Port Select[0] [6] Reserved [5:2] Byte Enable, all active. [1:0] PI7C9X2G1224GP Register Address, Bits [11:10] |
| 3 | 3Eh | [7:0] PI7C9X2G1224GP Register Address, Bits [9:2] |

I²C Register Write Access Example – Data Cycle

| Byte | Value | Description |
|------|-------|--------------------------|
| 0 | 12h | Data to Write for Byte 3 |
| 1 | 34h | Data to Write for Byte 2 |
| 2 | 56h | Data to Write for Byte 1 |
| 3 | 78h | Data to Write for Byte 0 |

Figure 7-10 I²C Write Command Packet Example

I²C Write Packet Address Phase Bytes

| 1 st Cycle | | | |
|-----------------------|-------------------------|-----------------------------|---------|
| START | 7654321 | 0 | ACK/NAK |
| S | Slave Address 0111_000b | Read/Write Bit 0 = Write | A |

I²C Write Packet Command Phase Bytes

| Command Cycle | | | | | | | |
|---------------------------------|---------|---------------------------------|---------|---------------------------------|---------|---------------------------------|---------|
| 76543210 | ACK/NAK | 76543210 | ACK/NAK | 76543210 | ACK/NAK | 76543210 | ACK/NAK |
| Command Byte 0 0000 0011b | A | Command Byte 1 0000 0000b | A | Command Byte 2 0011 1100b | A | Command Byte 3 0011 1110b | A |

I²C Write Packet Data Phase Bytes

| Write Cycle | | | | | | | | |
|-----------------|---------|-----------------|---------|-----------------|---------|-----------------|---------|------|
| 76543210 | ACK/NAK | 76543210 | ACK/NAK | 76543210 | ACK/NAK | 76543210 | ACK/NAK | STOP |
| Register Byte 3 | A | Register Byte 2 | A | Register Byte 1 | A | Register Byte 0 | A | P |

7.3.2 I²C REGISTER READ ACCESS

When the I²C Master attempts to read a PI7C9X2G1224GP register, two packets are transmitted. The 1st packet consists of Address and Command Phase bytes to the Slave. The 2nd packet consists of Address and Data Phase bytes.

According to the I²C Bus, v2.1, a Read cycle is triggered when the Read/Write bit (bit 0) of the 1st cycle is Set. The Command phase reads the requested register content into the internal buffer. When the I²C Read access occurs, the internal buffer value is transferred on to the I²C Bus, starting from Byte 3 (bits [31: 24]), followed by the subsequent bytes, with Byte 0 (bits [7:0]) being transferred last. If the I²C Master requests more than four bytes, the PI7C9X2G1224GP re-transmits the same byte sequence, starting from Byte 3 of the internal buffer.

The 1st and 2nd I²C Read packets perform the following functions:

- 1st packet - Selects the register to read
- 2nd packet - Reads the register (sample 2nd packet provided is for a 7-bit PI7C9X2G1224GP I²C Slave address)

Although two packets are shown for the I²C Read, the I²C Master can merge the two packets together into a single packet, by not generating the STOP at the end of the first packet (Master does not relinquish the bus) and generating REPEAT START.

Table 7-13 describes each I²C Command byte for Read access. In the packet described in Figure 7-11, Command Bytes 0 through 3 for Reads follow the format specified in Table 7-13.

Table 7-13 I²C Command Format for Read Access

| Byte | Bit(s) | Description |
|---------------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 st (0) | 7:3 | Reserved |
| | 2:0 | Command 100b = Read register |
| 2 nd (1) | 7:4 | Reserved |
| | 3:0 | Port Select, Bits [4:1] 2 nd Command byte, bit [3:0], and 3 rd Command byte, bit 7, combine to form a 5-bit Port Select. |
| 3 rd (2) | 7 | Port Select[0] 2 nd Command byte, bits [3:0], and 3 rd Command byte, bit 7, combine to form a 5-bit Port Select. Port Select[4:0] is used to select Port to access. 00h – Port 0 01h – Port 1 or NT Port Link Interface (if NT mode is enabled) |

| Byte | Bit(s) | Description | | | | | | | | | | |
|---------------------|--------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------------|---|------------------------------------------------------------------|---|-------------------------------------------------------------------|---|--------------------------------------------------------------------|---|--------------------------------------------------------------------|
| | | 02h ~ 0Bh – Port 2 ~ Port 11 10h for NT Port Virtual Interface 0Ch – 1Fh are reserved | | | | | | | | | | |
| | 6 | Reserved | | | | | | | | | | |
| | 5:2 | Byte Enable <table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>2</td> <td>Byte Enable for Data Byte 4 (PI7C9X2G1224GP register bits [7:0])</td> </tr> <tr> <td>3</td> <td>Byte Enable for Data Byte 3 (PI7C9X2G1224GP register bits [15:8])</td> </tr> <tr> <td>4</td> <td>Byte Enable for Data Byte 2 (PI7C9X2G1224GP register bits [23:16])</td> </tr> <tr> <td>5</td> <td>Byte Enable for Data Byte 1 (PI7C9X2G1224GP register bits [31:24])</td> </tr> </tbody> </table> 0 = Corresponding PI7C9X2G1224GP register byte will not be modified 1 = Corresponding PI7C9X2G1224GP register byte will be modified | Bit | Description | 2 | Byte Enable for Data Byte 4 (PI7C9X2G1224GP register bits [7:0]) | 3 | Byte Enable for Data Byte 3 (PI7C9X2G1224GP register bits [15:8]) | 4 | Byte Enable for Data Byte 2 (PI7C9X2G1224GP register bits [23:16]) | 5 | Byte Enable for Data Byte 1 (PI7C9X2G1224GP register bits [31:24]) |
| Bit | Description | | | | | | | | | | | |
| 2 | Byte Enable for Data Byte 4 (PI7C9X2G1224GP register bits [7:0]) | | | | | | | | | | | |
| 3 | Byte Enable for Data Byte 3 (PI7C9X2G1224GP register bits [15:8]) | | | | | | | | | | | |
| 4 | Byte Enable for Data Byte 2 (PI7C9X2G1224GP register bits [23:16]) | | | | | | | | | | | |
| 5 | Byte Enable for Data Byte 1 (PI7C9X2G1224GP register bits [31:24]) | | | | | | | | | | | |
| | 1:0 | PI7C9X2G1224GP Register Address [11:10] | | | | | | | | | | |
| 4 th (3) | 7:0 | PI7C9X2G1224GP Register Address [9:2] Note: Address bits[1:0] are fixed to 0. | | | | | | | | | | |

Figure 7-11 I²C Read Command Packet

I²C Read Command Packet Address Phase Byte (1st Packet)

| 1 st Cycle | | | |
|-----------------------|--------------------|-----------------------------|----------------|
| START | 7654321 | 0 | ACK/NAK |
| S | Slave Address[7:1] | Read/Write Bit 0 = Write | A |

I²C Read Command Packet Command Phase Byte (1st Packet)

| Write Cycle | | | | | | | |
|-------------------|----------------|-------------------|----------------|-------------------|----------------|-------------------|----------------|
| 76543210 | ACK/NAK | 76543210 | ACK/NAK | 76543210 | ACK/NAK | 76543210 | ACK/NAK |
| Command Byte 0 | A | Command Byte 1 | A | Command Byte 2 | A | Command Byte 3 | A |

I²C Read Data Packet Address Phase Byte (2nd Packet)

| 1 st Cycle | | | |
|-----------------------|--------------------|----------------------------|----------------|
| START | 7654321 | 0 | ACK/NAK |
| S | Slave Address[7:1] | Read/Write Bit 1 = Read | A |

I²C Read Data Packet Data Phase Byte (2nd Packet)

| Write Cycle | | | | | | | | |
|--------------------|----------------|--------------------|----------------|--------------------|----------------|--------------------|----------------|-------------|
| 76543210 | ACK/NAK | 76543210 | ACK/NAK | 76543210 | ACK/NAK | 76543210 | ACK/NAK | STOP |
| Register Byte 3 | A | Register Byte 2 | A | Register Byte 1 | A | Register Byte 0 | A | P |

The following tables illustrate a sample I²C packet for reading the PI7C9X2G1224GP SSID/SSVID register (offset F8h) for Port 0. The default value for SSID/SSVID register is 0000_0000h.

Note: The PI7C9X2G1224GP has a default I²C Slave address [6:0] value of 38h, with the I2C_ADDR[2:0] inputs having a value of 000. The byte sequence on the I²C Bus, as listed in the following tables, occurs after the START and before the STOP bits, by which the I²C Master frames the transfer.

Figure 7-12 I²C Register Read Access Example

I²C Register Read Access Example – Address Cycle (1st Packet)

| Phase | Value | Description |
|---------|-------|--------------------------------------------------------------------------------------------------------|
| Address | 70h | Bits [7:1] for PI7C9X2G1224GP I ² C Slave Address (38h) with last bit (bit 0) for Write = 0 |

I²C Register Read Access Example – Command Cycle (1st Packet)

| Byte | Value | Description |
|------|----------------|-----------------------------------------------------------------------------------------------------------------------------|
| 0 | 04h | [7:3] Reserved [2:0] Command , 100b = Read register |
| 1 | 00h for Port 0 | [7:4] Reserved [3:0] Port Select[4:1] |
| 2 | 3Ch for Port 0 | [7] Port Select[0] [6] Reserved [5:2] Byte Enable, All active. [1:0] PI7C9X2G1224GP Register Address, Bits [11:10] |
| 3 | 3Eh | [7:0] PI7C9X2G1224GP Register Address, Bits [9:2] |

I²C Register Read Access Example – 2nd Packet

| Phase | Value | Description |
|---------|-------|------------------------------------------------------------------------------------------|
| Address | 71h | Bits [7:1] for PI7C9X2G1224GP I2C Slave Address (38h) with last bit (bit 0) for Read = 1 |
| Read | 00h | Byte 3 of Register Read |
| | 00h | Byte 2 of Register Read |
| | 00h | Byte 1 of Register Read |
| | 00h | Byte 0 of Register Read |

Figure 7-13 I²C Read Command Packet

I²C Read Command Packet Address Phase Bytes (1st Packet)

| 1 st Cycle | | | |
|-----------------------|-------------------------|-----------------------------|---------|
| START | 7654321 | 0 | ACK/NAK |
| S | Slave Address 0111_000b | Read/Write Bit 0 = Write | A |

I²C Read Command Packet Command Phase Bytes (1st Packet)

| Command Cycle | | | | | | |
|---------------------------------|---------|---------------------------------|---------|---------------------------------|---------|---------------------------------|
| 76543210 | ACK/NAK | 76543210 | ACK/NAK | 76543210 | ACK/NAK | 76543210 |
| Command Byte 0 0000 0100b | A | Command Byte 1 0000 0000b | A | Command Byte 2 0011 1100b | A | Command Byte 3 0011 1110b |

I²C Read Data Packet Address Phase Bytes (2nd Packet)

| 1 st Cycle | | | |
|-----------------------|-------------------------------|----------------------------|---------|
| START | 7654321 | 0 | ACK/NAK |
| S | Slave Address [7:1] 0111_000b | Read/Write Bit 1 = Read | A |

I²C Read Data Packet Data Phase Bytes (2nd Packet)

| Command Cycle | | | | | | | |
|------------------------------|---------|------------------------------|---------|------------------------------|---------|-------------------------------|------|
| 76543210 | ACK/NAK | 76543210 | ACK/NAK | 76543210 | ACK/NAK | 76543210 | Stop |
| Register Byte3 0000 0000b | A | Register Byte2 0000 0000b | A | Register Byte1 0000 0000b | A | Register Byte0 0000 00000b | P |

8 REGISTER DESCRIPTION

8.1 REGISTER TYPES

This chapter details the Packet Switch registers, including

- Bit names
- Description of register functions
- Type, refer to Table 8-1
- Whether the default value can be modified by EEPROM and/or I2C
- Default value

Table 8-1 Register Types

| REGISTER TYPE | DEFINITION |
|---------------|---------------------------------|
| HwInt | Hardware Initialization |
| RO | Read Only |
| RW | Read / Write |
| RWIC | Read / Write 1 to Clear |
| RsvdP | RO and must return 0 when read. |

8.2 TRANSPARENT MODE CONFIGURATION REGISTERS

When the port of the Switch is set to operate at the transparent mode, it is represented by a logical PCI-to-PCI Bridge that implements type 1 configuration space header. The following table details the allocation of the register fields of the PCI 2.3 compatible type 1 configuration space header.

| 31 – 24 | 23 – 16 | 15 – 8 | 7 – 0 | BYTE OFFSET |
|-------------------------------------------------------------------|------------------------|----------------------------------|--------------------|-------------|
| Device ID | | Vendor ID | | 00h |
| Primary Status | | Command | | 04h |
| Class Code | | Revision ID | | 08h |
| Reserved | Header Type | Primary Latency Timer | Cache Line Size | 0Ch |
| Base Address 0 for Upstream Port) / Reserved for Downstream Ports | | | | 10h |
| Base Address 1 for Upstream Port) / Reserved for Downstream Ports | | | | 14h |
| Secondary Latency Timer | Subordinate Bus Number | Secondary Bus Number | Primary Bus Number | 18h |
| Secondary Status | | I/O Limit Address | I/O Base Address | 1Ch |
| Memory Limit Address | | Memory Base Address | | 20h |
| Prefetchable Memory Limit Address | | Prefetchable Memory Base Address | | 24h |
| Prefetchable Memory Base Address Upper 32-bit | | | | 28h |
| Prefetchable Memory Limit Address Upper 32-bit | | | | 2Ch |
| I/O Limit Address Upper 16-bit | | I/O Base Address Upper 16-bit | | 30h |
| Reserved | | Capability Pointer to 40h | | 34h |
| Reserved | | | | 38h |
| Bridge Control | | Interrupt Pin | Interrupt Line | 3Ch |
| Power Management Capabilities | | Next Item Pointer=48h | Capability ID=01h | 40h |
| PM Data | PPB Support Extensions | Power Management Data | | 44h |
| Message Control | | Next Item Pointer=68h | Capability ID=05h | 48h |
| Message Address | | | | 4Ch |
| Message Upper Address | | | | 50h |
| Reserved | | Message Data | | 54h |
| Reserved | | | | 58h – 64h |
| PCI Express Capabilities Register | | Next Item Pointer=A4h | Capability ID=10h | 68h |
| Device Capabilities | | | | 6Ch |
| Device Status | | Device Control | | 70h |
| Link Capabilities | | | | 74h |
| Link Status | | Link Control | | 78h |

| 31 – 24 | 23 – 16 | 15 – 8 | 7 – 0 | BYTE OFFSET |
|-----------------------|---------|-----------------------|---------------------------------|-------------|
| Slot Capabilities | | | | 7Ch |
| Slot Status | | Slot Control | | 80h |
| Reserved | | | | 84h – 88h |
| Device Capabilities 2 | | | | 8Ch |
| Device Status 2 | | Device Control 2 | | 90h |
| Link Capabilities 2 | | | | 94h |
| Link Status 2 | | Link Control 2 | | 98h |
| Slot Capabilities 2 | | | | 9Ch |
| Slot Status 2 | | Slot Control 2 | | A0h |
| Reserved | | Next Item Pointer=00h | SSID/SSVID Capability ID=0Dh | A4h |
| SSID | | SSVID | | A8h |
| Reserved | | | | ACh – E0h |
| BAR 0-1 Configuration | | | | E4h |
| Reserved | | | | E8h - FCh |

Other than the PCI 2.3 compatible configuration space header, the Switch also implements PCI express extended configuration space header, which includes advanced error reporting, virtual channel, and power budgeting capability registers. The following table details the allocation of the register fields of PCI express extended capability space header. The first extended capability always begins at offset 100h with a PCI Express Enhanced Capability header and the rest of capabilities are located at an offset greater than 0FFh relative to the beginning of PCI compatible configuration space.

| 31 – 24 | 23 – 16 | 15 – 8 | 7 – 0 | BYTE OFFSET |
|-----------------------------------------------------|-------------------------------------|-----------------|------------------------------------------|-------------|
| Next Capability Offset=FB4h | | Cap. Version | PCI Express Extended Capability ID=0003h | 100h |
| Serial Number Lower DW | | | | 104h |
| Serial Number Upper DW | | | | 108h |
| Reserved | | | | 10Ch – 134h |
| Next Capability Offset=148h | | Cap. Version | PCI Express Extended Capability ID=0004h | 138h |
| Reserved | | | Data Select Register | 13Ch |
| Data Register | | | | 140h |
| Reserved | | | Power Budget Capability Register | 144h |
| Next Capability Offset= 270h (Up) 520h (Down) | | Cap. Version | PCI Express Extended Capability ID=0002h | 148h |
| Port VC Capability Register 1 | | | | 14Ch |
| VC Arbitration Table Offset=4h | Port VC Capability Register 2 | | | 150h |
| Port VC Status | | Port VC Control | | 154h |
| Port Arbitration Table Offset=5h | VC Resource Capability Register (0) | | | 158h |
| VC Resource Control Register (0) | | | | 15Ch |
| VC Resource Status Register (0) | | Reserved | | 160h |
| Port Arbitration Table Offset=6h | VC Resource Capability Register (1) | | | 164h |
| VC Resource Control Register (1) | | | | 168h |
| VC Resource Status Register (1) | | Reserved | | 16Ch |
| Reserved | | | | 170h – 184h |
| VC Arbitration Table 0 | | | | 188h |
| VC Arbitration Table 1 | | | | 18Ch |
| VC Arbitration Table 2 | | | | 190h |
| VC Arbitration Table 3 | | | | 194h |
| Port VC0 Arbitration Table 0 (Low) | | | | 198h |
| Port VC0 Arbitration Table 0 (Upper) | | | | 19Ch |
| Port VC0 Arbitration Table 1 (Low) | | | | 1A0h |
| Port VC0 Arbitration Table 1 (Upper) | | | | 1A4h |
| Port VC1 Arbitration Table 0 (Low) | | | | 1A8h |
| Port VC1 Arbitration Table 0 (Upper) | | | | 1ACh |
| Port VC1 Arbitration Table 1 (Low) | | | | 1B0h |
| Port VC1 Arbitration Table 1 (Upper) | | | | 1B4h |
| Reserved | | | | 1B8h – 1C4h |

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| 31 - 24 | 23 - 16 | 15 - 8 | 7 - 0 | BYTE OFFSET |
|-----------------------------------------------|---------|-----------------------|------------------------------------------|-------------|
| ECC Error Check Disable | | | | 1C8h |
| Reserved | | | | 1CCh - 1D8h |
| NT-UP Port Selection | | | | 1DCh |
| Power Manager Hot Plug Configuration | | | | 1E0h |
| Reserved | | | | 1E4h - 1F0h |
| Software Lane Status | | | | 1F4h |
| Reserved | | | | 1F8h - 204h |
| De-emphasis Control | | Rate Control | | 208h |
| Reserved | | Compliance Mode | | 20Ch |
| Reserved | | | | 210h - 21Ch |
| Even Port Physical Layer Command and Status | | | | 220h |
| Odd Port Physical Layer Command and Status | | | | 224h |
| Reserved | | | | 228h - 22Ch |
| Even Port Disable / Quiet / Test Pattern Rate | | | | 230h |
| Odd Port Disable / Quiet / Test Pattern Rate | | | | 234h |
| Reserved | | | | 238h - 26Ch |
| Next Capability Offset=900h | | Cap version | PCI Express Extended Capability ID=001Eh | 270h |
| L1 PM Substates Capability | | | | 274h |
| L1 PM Substates Control 1 | | | | 278h |
| L1 PM Substates Control 2 | | | | 27Ch |
| Reserved | | | | 280h - 340h |
| I2C Control and Status | | | | 344h |
| Hot Plug Select | | | | 348h |
| Disable Downstream Port Hot Reset | | | | 34Ch |
| Reserved | | | | 350h - 51Ch |
| Next Capability Offset=270h | | Cap version | PCI Express Extended Capability ID=000Dh | 520h |
| ACS Control | | ACS Capability | | 524h |
| Reserved | | Egress Control Vector | | 528h |
| Reserved | | | | 52Ch - 628h |
| GPIO 0-15 Direction Control | | | | 62Ch |
| GPIO 16-31 Direction Control | | | | 630h |
| Reserved | | | | 634h |
| GPIO Input De-bounce | | | | 638h |
| GPIO 0-15 Input Data | | | | 63Ch |
| GPIO 16-31 Input Data | | | | 640h |
| GPIO 0-15 Output Data | | | | 644h |
| GPIO 16-31 Output Data | | | | 648h |
| GPIO 0-31 Interrupt Polarity | | | | 64Ch |
| GPIO 0-31 Interrupt Status | | | | 650h |
| GPIO 0-31 Interrupt Mask | | | | 654h |
| Reserved | | | | 658h-840h |
| XPIP_CSR0 | | | | 844h |
| XPIP_CSR1 | | | | 848h |
| Decode VGA | | Reserved | | 84Ch |
| Switch Operation Mode | | | | 850h |
| PHY Parameter 1 | | XPIP_CSR2 | | 854h |
| PHY Parameter 2 | | | | 858h |
| PHY Parameter 3 | | | | 85Ch |
| PHY Parameter 4 | | | | 860h |
| XPIP_CSR3 | | | | 864h |
| XPIP_CSR4 | | | | 868h |
| XPIP_CSR5 | | | | 86Ch |
| Non Transfer Mode | | | | 870h |
| Operation Mode | | | | 874h |
| Device Specific PM Event | | | | 878h |
| EEPROM Control | | | | 87Ch |
| EEPROM Address and Data | | | | 880h |
| Debugout Control | | | | 884h |
| Debugout Data | | | | 888h |
| LTSSM CSR | | | | 88Ch |
| MAC CSR 1 | | | | 890h |
| Reserved | | | | 894h - 8A0h |

| 31 - 24 | 23 - 16 | 15 - 8 | 7 - 0 | BYTE OFFSET |
|-----------------------------------------------------|-----------|-------------------------|------------------------------------------|-------------|
| Power Saving Disable | | | | 8A4h |
| Transaction Layer CSR | | | | 8A8h |
| ACK Latency Timer | | Replay Time-out Counter | | 8ACh |
| PHY Parameter 0 | | | | 8B0h |
| XPIP_CSR7 | XPIP_CSR6 | Port Misc 0 | | 8B4h |
| Reserved | | Port Misc 1 | | 8B8h |
| Reserved | | Port Misc 2 | | 8BCh |
| LED Display CSR | | | | 8C0h - 8FCh |
| Reserved | | | | 900h |
| Next Capability Offset=000h | | Cap. Version | PCI Express Extended Capability ID=0012h | 904h |
| Multi-Case Control | | Multi-Case Capability | | 908h |
| Multi-Case Base Address 0 | | | | 90Ch |
| Multi-Case Base Address 1 | | | | 910h |
| Multi-Case Receive | | | | 914h |
| Reserved | | | | 918h |
| Multi-Case Block All | | | | 91Ch |
| Reserved | | | | 920h |
| Multi-Case Block Untranslated | | | | 924h - FACH |
| Reserved | | | | FB0h |
| EEPROM Scratchpad | | | | FB4h |
| Next Capability Offset= 138h (Up) 148h (Down) | | Cap. Version | PCI Express Extended Capability ID=0001h | FB8h |
| Uncorrectable Error Status Register | | | | FBCh |
| Uncorrectable Error Mask Register | | | | FC0h |
| Uncorrectable Error Severity Register | | | | FC4h |
| Correctable Error Status Register | | | | FC8h |
| Correctable Error Mask Register | | | | FCCh |
| Advanced Error Capabilities and Control Register | | | | FD0h |
| Header Log Register 0 | | | | FD4h |
| Header Log Register 1 | | | | FD8h |
| Header Log Register 2 | | | | FDCh |
| Header Log Register 3 | | | | FE0h |
| Diagnostic Data 4 | | | | FE4h - FF4h |
| Reserved | | | | FF8h |
| Clock Buffer Control | | | | FFCh |
| Clock Buffer Port Select | | | | |

8.2.1 VENDOR ID REGISTER – OFFSET 00h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-----------|------|--------------------------------------------------|----------------------|---------|
| 15:0 | Vendor ID | RO | Identifies Pericom as the vendor of this device. | Yes | 12D8h |

8.2.2 DEVICE ID REGISTER – OFFSET 00h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------|------|-----------------------------------------------|----------------------|---------|
| 31:16 | Device ID | RO | Identifies this device as the PI7C9X2G1224GP. | Yes | 1224h |

8.2.3 COMMAND REGISTER – OFFSET 04h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|------------------|------|-----------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | I/O Space Enable | RW | 0b: Ignores I/O transactions on the primary interface 1b: Enables responses to I/O transactions on the primary interface | No/Yes | 0 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/I2C-SMBUS | DEFAULT |
|-------|------------------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|---------|
| 1 | Memory Space Enable | RW | 0b: Ignores memory transactions on the primary interface 1b: Enables responses to memory transactions on the primary interface | No/Yes | 0 |
| 2 | Bus Master Enable | RW | 0b: Does not initiate memory or I/O transactions on the upstream port and handles as an Unsupported Request (UR) to memory and I/O transactions on the downstream port. For Non-Posted Requests, a completion with UR completion status must be returned 1b: Enables the Switch Port to forward memory and I/O Read/Write transactions in the upstream direction | No/Yes | 0 |
| 3 | Special Cycle Enable | RsvdP | Not Support. | No | 0 |
| 4 | Memory Write And Invalidate Enable | RsvdP | Not support. | No | 0 |
| 5 | VGA Palette Snoop Enable | RsvdP | Not Support. | No | 0 |
| 6 | Parity Error Response Enable | RW | 0b: Switch may ignore any parity errors that it detects and continue normal operation 1b: Switch must take its normal action when a parity error is detected | No/Yes | 0 |
| 7 | Wait Cycle Control | RsvdP | Not Support. | No | 0 |
| 8 | SERR# enable | RW | 0b: Disables the reporting of Non-fatal and Fatal errors detected by the Switch to the Root Complex 1b: Enables the Non-fatal and Fatal error reporting to Root Complex | No/Yes | 0 |
| 9 | Fast Back-to-Back Enable | RsvdP | Not Support. | No | 0 |
| 10 | Interrupt Disable | RW | Controls the ability of a PCI Express device to generate INTx Interrupt Messages. In the Switch, this bit does not affect the forwarding of INTx messages from the downstream ports. | No/Yes | 0 |
| 15:11 | Reserved | RsvdP | Not Support. | No | 0000 0b |

8.2.4 PRIMARY STATUS REGISTER – OFFSET 04h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/I2C-SMBUS | DEFAULT |
|-------|---------------------------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|---------|
| 18:16 | Reserved | RsvdP | Not Support. | No | 000b |
| 19 | Interrupt Status | RO | Indicates that an INTx Interrupt Message is pending internally to the device. In the Switch, the forwarding of INTx messages from the downstream device of the Switch port is not reflected in this bit. Must be hardwired to 0. | No | 0 |
| 20 | Capabilities List | RO | Set to 1b to enable support for the capability list (offset 34h is the pointer to the data structure). | No | 1 |
| 21 | 66MHz Capable | RO | Does not apply to PCI Express. Must be hardwired to 0. | No | 0 |
| 22 | Reserved | RsvdP | Not Support. | No | 0 |
| 23 | Fast Back-to-Back Capable | RsvdP | Not Support. | No | 0 |
| 24 | Master Data Parity Error | RW1C | Set to 1b (by a requester) whenever a Parity error is detected or forwarded on the primary side of the port in a Switch. If the Parity Error Response Enable bit is cleared, this bit is never set. | No/Yes | 0 |
| 26:25 | DEVSEL# timing | RsvdP | Not Support. | No | 00b |
| 27 | Signaled Target Abort | RsvdP | Not Support. | No | 0 |
| 28 | Received Target Abort | RsvdP | Not Support. | No | 0 |
| 29 | Received Master Abort | RsvdP | Not Support. | No | 0 |
| 30 | Signaled System Error | RW1C | Set to 1b when the Switch sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR Enable bit in the Command register is 1. | No/Yes | 0 |
| 31 | Detected Parity Error | RW1C | Set to 1b whenever the primary side of the port in a Switch receives a Poisoned TLP. | No/Yes | 0 |

8.2.5 REVISION ID REGISTER – OFFSET 08h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|----------|------|--------------------------------------|----------------------|---------|
| 7:0 | Revision | RO | Indicates revision number of device. | Yes | 00h |

8.2.6 CLASS REGISTER – OFFSET 08h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------------------|------|---------------------------------------------------------------------------------------------|----------------------|---------|
| 15:8 | Programming Interface | RO | Read as 00h to indicate no programming interfaces have been defined for PCI-to-PCI Bridges. | No | 00h |
| 23:16 | Sub-Class Code | RO | Read as 04h to indicate device is a PCI-to-PCI Bridge. | No | 04h |
| 31:24 | Base Class Code | RO | Read as 06h to indicate device is a Bridge device. | No | 06h |

8.2.7 CACHE LINE REGISTER – OFFSET 0Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|-----------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 7:0 | Cache Line Size | RW | The cache line size register is set by the system firmware and the operating system cache line size. This field is implemented by PCI Express devices as a RW field for legacy compatibility, but it has no impact on any PCI Express device functionality. | No/Yes | 00h |

8.2.8 PRIMARY LATENCY TIMER REGISTER – OFFSET 0Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-----------------------|-------|--------------|----------------------|---------|
| 15:8 | Primary Latency Timer | RsvdP | Not Support. | No | 00h |

8.2.9 HEADER TYPE REGISTER – OFFSET 0Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------------------|------|-----------------------------------------------------------------------------------------------------|----------------------|------------------------|
| 22:16 | Header Type | RO | Read as 01h to indicate that the register layout conforms to the standard PCI-to-PCI Bridge layout. | No | 01h |
| 23 | Multi-Function Device | RO | 0b: Single function device 1b: Multiple functions device | No | 1 for Up 0 for Down |

8.2.10 BASE ADDRESS 0 REGISTER – OFFSET 10h (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|------------------------|-------|----------------------------------------------------------------------|----------------------|---------|
| 0 | Memory Space Indicator | RO | 0b: indicate Memory Base address 1b: indicate I/O Base address | No | 0 |
| 2:1 | 64-bit Addressing | RO | 00b: 32-bit addressing 10b: 64-bit addressing Others: Reserved | No | 00b |
| 3 | Prefetchable | RO | 0b: Non-prefetchable 1b: Prefetchable | No | 0 |
| 16:4 | Reserved | RsvdP | Not Support. | No | 0-0h |
| 31:17 | Base Address 0 | RW | Use this Memory base address to map the packet switch registers. | No/Yes | 0-0h |

8.2.11 BASE ADDRESS 1 REGISTER – OFFSET 14h (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|----------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|------------|
| 31:0 | Base Address 1 | RO/RW | RO when the Base Address 0 register is not 64-bit addressing (offset 10h[2:1] is not 10b). RW when the Base Address 0 register is 64-bit addressing. Base Address 1 is used to provide the upper 32 Address bits when offset 10h[2:1] is set to 10b. | No/Yes | 0000_0000h |

8.2.12 PRIMARY BUS NUMBER REGISTER – OFFSET 18h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|--------------------|------|-------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 7:0 | Primary Bus Number | RW | Indicates the number of the PCI bus to which the primary interface is connected. The value is set in software during configuration. | No/Yes | 00h |

8.2.13 SECONDARY BUS NUMBER REGISTER – OFFSET 18h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|----------------------|------|---------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 15:8 | Secondary Bus Number | RW | Indicates the number of the PCI bus to which the secondary interface is connected. The value is set in software during configuration. | No/Yes | 00h |

8.2.14 SUBORDINATE BUS NUMBER REGISTER – OFFSET 18h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|------------------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 23:16 | Subordinate Bus Number | RW | Indicates the number of the PCI bus with the highest number that is subordinate to the Bridge. The value is set in software during configuration. | No/Yes | 00h |

8.2.15 SECONDARY LATENCY TIMER REGISTER – OFFSET 18h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-------------------------|-------|--------------|----------------------|---------|
| 31:24 | Secondary Latency Timer | RsvdP | Not Support. | No | 00h |

8.2.16 I/O BASE ADDRESS REGISTER – OFFSET 1Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|--------------------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 3:0 | 32-bit Indicator | RO | Read as 1h to indicate 32-bit I/O addressing. | No | 1h |
| 7:4 | I/O Base Address [15:12] | RW | Defines the bottom address of the I/O address range for the Bridge to determine when to forward I/O transactions from one interface to the other. The upper 4 bits correspond to address bits [15:12] and are writable. The lower 12 bits corresponding to address bits [11:0] are assumed to be 0. The upper 16 bits corresponding to address bits [31:16] are defined in the I/O base address upper 16 bits address register. | No/Yes | 0h |

8.2.17 I/O LIMIT ADDRESS REGISTER – OFFSET 1Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 11:8 | 32-bit Indicator | RO | Read as 1h to indicate 32-bit I/O addressing. | No | 1h |
| 15:12 | I/O Limit Address [15:12] | RW | Defines the top address of the I/O address range for the Bridge to determine when to forward I/O transactions from one interface to the other. The upper 4 bits correspond to address bits [15:12] and are writable. The lower 12 bits corresponding to address bits [11:0] are assumed to be FFFh. The upper 16 bits corresponding to address bits [31:16] are defined in the I/O limit address upper 16 bits address register. | No/Yes | 0h |

8.2.18 SECONDARY STATUS REGISTER – OFFSET 1Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 20:16 | Reserved | RsvdP | Not Support. | No | 0 0000b |
| 21 | 66MHz Capable | RsvdP | Not Support. | No | 0 |
| 22 | Reserved | RsvdP | Not Support. | No | 0 |
| 23 | Fast Back-to-Back Capable | RsvdP | Not Support. | No | 0 |
| 24 | Master Data Parity Error | RW1C | Set to 1b (by a requester) whenever a Parity error is detected or forwarded on the secondary side of the port in a Switch. If the Parity Error Response Enable bit is cleared, this bit is never set. | No/Yes | 0 |
| 26:25 | DEVSEL L timing | RsvdP | Not Support. | No | 00b |
| 27 | Signaled Target Abort | RsvdP | Not Support. | No | 0 |
| 28 | Received Target Abort | RsvdP | Not Support. | No | 0 |
| 29 | Received Master Abort | RsvdP | Not Support. | No | 0 |
| 30 | Received System Error | RW1C | Set to 1b when the Switch sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR Enable bit in the Bridge Control register is 1. | No/Yes | 0 |
| 31 | Detected Parity Error | RW1C | Set to 1b whenever the secondary side of the port in a Switch receives a Poisoned TLP. | No/Yes | 0 |

8.2.19 MEMORY BASE ADDRESS REGISTER – OFFSET 20h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-----------------------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 3:0 | Reserved | RsvdP | Not Support. | No | 0h |
| 15:4 | Memory Base Address [31:20] | RW | Defines the bottom address of an address range for the Bridge to determine when to forward memory transactions from one interface to the other. The upper 12 bits correspond to address bits [31:20] and are able to be written to. The lower 20 bits corresponding to address bits [19:0] are assumed to be 0. | No/Yes | 000h |

8.2.20 MEMORY LIMIT ADDRESS REGISTER – OFFSET 20h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|------------------------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 19:16 | Reserved | RsvdP | Not Support. | No | 0h |
| 31:20 | Memory Limit Address [31:20] | RW | Defines the top address of an address range for the Bridge to determine when to forward memory transactions from one interface to the other. The upper 12 bits correspond to address bits [31:20] and are writable. The lower 20 bits corresponding to address bits [19:0] are assumed to be FFFFh. | No/Yes | 000h |

8.2.21 PREFETCHABLE MEMORY BASE ADDRESS REGISTER – OFFSET 24h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|------------------------------------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 3:0 | 64-bit addressing | RO | Read as 1h to indicate 64-bit addressing. | No | 1h |
| 15:4 | Prefetchable Memory Base Address [31:20] | RW | Defines the bottom address of an address range for the Bridge to determine when to forward memory read and write transactions from one interface to the other. The upper 12 bits correspond to address bits [31:20] and are writable. The lower 20 bits are assumed to be 0. The memory base register upper 32 bits contain the upper half of the base address. | No/Yes | 000h |

8.2.22 PREFETCHABLE MEMORY LIMIT ADDRESS REGISTER – OFFSET 24h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|------------------------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 19:16 | 64-bit addressing | RO | Read as 1h to indicate 64-bit addressing. | No | 1h |
| 31:20 | Memory Limit Address [31:20] | RW | Defines the top address of an address range for the Bridge to determine when to forward memory transactions from one interface to the other. The upper 12 bits correspond to address bits [31:20] and are writable. The lower 20 bits corresponding to address bits [19:0] are assumed to be FFFFh. | No/Yes | 000h |

8.2.23 PREFETCHABLE MEMORY BASE ADDRESS UPPER 32-BITS REGISTER – OFFSET 28h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|---------------------------------------------------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|------------|
| 31:0 | Prefetchable Memory Base Address, Upper 32-bits [63:32] | RW | Defines the upper 32-bits of a 64-bit bottom address of an address range for the Bridge to determine when to forward memory read and write transactions from one interface to the other. | No/Yes | 0000_0000h |

8.2.24 PREFETCHABLE MEMORY LIMIT ADDRESS UPPER 32-BITS REGISTER – OFFSET 2Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|----------------------------------------------------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|------------|
| 31:0 | Prefetchable Memory Limit Address, Upper 32-bits [63:32] | RW | Defines the upper 32-bits of a 64-bit top address of an address range for the Bridge to determine when to forward memory read and write transactions from one interface to the other. | No/Yes | 0000_0000h |

8.2.25 I/O BASE ADDRESS UPPER 16-BITS REGISTER – OFFSET 30h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-----------------------------------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 15:0 | I/O Base Address, Upper 16-bits [31:16] | RW | Defines the upper 16-bits of a 32-bit bottom address of an address range for the Bridge to determine when to forward I/O transactions from one interface to the other. | No/Yes | 0000h |

8.2.26 I/O LIMIT ADDRESS UPPER 16-BITS REGISTER – OFFSET 30h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|------------------------------------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 31:16 | I/O Limit Address, Upper 16-bits [31:16] | RW | Defines the upper 16-bits of a 32-bit top address of an address range for the Bridge to determine when to forward I/O transactions from one interface to the other. | No/Yes | 0000h |

8.2.27 CAPABILITY POINTER REGISTER – OFFSET 34h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|--------------------|------|------------------------------------|----------------------|---------|
| 7:0 | Capability Pointer | RO | Indicates next capability pointer. | Yes | 40h |

8.2.28 INTERRUPT LINE REGISTER – OFFSET 3Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|----------------|------|-------------------------------|----------------------|---------|
| 7:0 | Interrupt Line | RW | Indicates the Interrupt Line. | No/Yes | 00h |

8.2.29 INTERRUPT PIN REGISTER – OFFSET 3Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|---------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|----------------------------|
| 15:8 | Interrupt Pin | RO | The Switch implements INTA virtual wire interrupt signals to represent hot-plug events at downstream ports. 0b: disable INTA 1b: enable INTA | Yes | 00h for Up 01h for Down |

8.2.30 BRIDGE CONTROL REGISTER – OFFSET 3Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|-----------------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 16 | Parity Error Response | RW | 0b: Ignore Poisoned TLPs on the secondary interface 1b: Enable the Poisoned TLPs reporting and detection on the secondary interface | No/Yes | 0 |
| 17 | S_SERR# Enable | RW | 0b: Disables the forwarding of EER_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary interface 1b: Enables the forwarding of EER_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary interface | No/Yes | 0 |
| 18 | ISA Enable | RW | 0b: Forwards downstream all I/O addresses in the address range defined by the I/O Base, I/O Base, and Limit registers 1b: Forwards upstream all I/O addresses in the address range defined by the I/O Base and Limit registers that are in the first 64KB of PCI I/O address space (top 768 bytes of each 1KB block) | No/Yes | 0 |
| 19 | VGA Enable | RW | 0b: Ignores access to the VGA memory or IO address range 1b: Forwards transactions targeted at the VGA memory or IO address range VGA memory range starts from 000A 0000h to 000B FFFFh VGA IO addresses are in the first 64KB of IO address space. AD [9:0] is in the ranges 3B0 to 3BBh and 3C0h to 3DFh. | No/Yes | 0 |
| 20 | VGA 16-bit Decode | RW | 0b: Executes 10-bit address decoding on VGA I/O accesses | No/Yes | 0 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| | | | 1b: Executes 16-bit address decoding on VGA I/O accesses | | |
| 21 | Master Abort Mode | RsvdP | Not Support. | No | 0 |
| 22 | Secondary Bus Reset | RW | 0b: Does not trigger a hot reset on the corresponding PCI Express Port 1b: Triggers a hot reset on the corresponding PCI Express Port At the downstream port, it asserts PORT_RST# to the attached downstream device. At the upstream port, it asserts the PORT_RST# at all the downstream ports. | No/Yes | 0 |
| 23 | Fast Back-to-Back Enable | RsvdP | Not Support. | No | 0 |
| 24 | Primary Master Timeout | RsvdP | Not Support. | No | 0 |
| 25 | Secondary Master Timeout | RsvdP | Not Support. | No | 0 |
| 26 | Master Timeout Status | RsvdP | Not Support. | No | 0 |
| 27 | Discard Timer SERR# Enable | RsvdP | Not Support. | No | 0 |
| 31:28 | Reserved | RsvdP | Not Support. | No | 0h |

8.2.31 POWER MANAGEMENT CAPABILITIES REGISTER – OFFSET 40h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------------|-------|----------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 7:0 | Enhanced Capabilities ID | RO | Read as 01h to indicate that these are power management enhanced capability registers. | No | 01h |
| 15:8 | Next Item Pointer | RO | Indicates next capability pointer. | Yes | 48h |
| 18:16 | Power Management Revision | RO | Read as 011b to indicate the device is compliant to Revision 1.2 of <i>PCI Power Management Interface Specifications</i> . | No | 011b |
| 19 | PME# Clock | RO | Does not apply to PCI Express. Must be hardwired to 0. | No | 0 |
| 20 | Reserved | RsvdP | Not Support. | No | 0 |
| 21 | Device specific Initialization | RO | Read as 0b to indicate Switch does not have device specific initialization requirements. | Yes | 0 |
| 24:22 | AUX Current | RO | Reset to 000b. | Yes | 000b |
| 25 | D1 Power State Support | RO | Read as 0b to indicate Switch does not support the D1 power management state. | Yes | 0 |
| 26 | D2 Power State Support | RO | Read as 0b to indicate Switch does not support the D2 power management state. | Yes | 0 |
| 31:27 | PME# Support | RO | Read as 19h to indicate Switch supports the forwarding of PME# message in D0, D3 and D4 states. | Yes | 19h |

8.2.32 POWER MANAGEMENT DATA REGISTER – OFFSET 44h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|---------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 1:0 | Power State | RW | Indicates the current power state of the Switch. Writing a value of D0 when the previous state was D3 cause a hot reset without asserting DWRST_L. 00b: D0 state 01b: D1 state 10b: D2 state 11b: D3 hot state | No/Yes | 00b |
| 2 | Reserved | RsvdP | Not Support. | No | 0 |
| 3 | No_Soft_Reset | RO | When set, this bit indicates that device transitioning from D3hot to D0 does not perform an internal reset. When clear, an internal reset is performed when power state transits from D3hot to D0. | Yes | 1 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-------------|---------------|------------------------------------------------------------------------------|----------------------|---------|
| 7:4 | Reserved | RsvdP | Not Support. | No | 0h |
| 8 | PME# Enable | RW | When asserted, the Switch will generate the PME# message. | No/Yes | 0 |
| 12:9 | Data Select | RW / RO | Select data registers. RW if offset 870h[1]=1 and RO if offset 870h[1]=0. | No/Yes | 0h |
| 14:13 | Data Scale | RO | Reset to 00b. | No | 00b |
| 15 | PME Status | RW1C | Read as 0b as the PME# message is not implemented. | No | 0 |

8.2.33 PPB SUPPORT EXTENSIONS REGISTER – OFFSET 44h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-------------------------------------|-------|--------------|----------------------|---------|
| 21:16 | Reserved | RsvdP | Not Support. | No | 00h |
| 22 | B2_B3 Support for D3 _{HOT} | RsvdP | Not Support. | No | 0 |
| 23 | Bus Power / Clock Control Enable | RsvdP | Not Support. | No | 0 |

8.2.34 DATA REGISTER – OFFSET 44h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------|------|----------------|----------------------|---------|
| 31:24 | Data Register | RO | Data Register. | Yes | 00h |

8.2.35 MSI CAPABILITIES REGISTER – OFFSET 48h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 7:0 | Enhanced Capabilities ID | RO | Read as 05h to indicate that this is message signal interrupt capability register. | No | 05h |
| 15:8 | Next Item Pointer | RO | Indicates next capability pointer. | Yes | 68h |
| 16 | MSI Enable | RW | 0b: The function is prohibited from using MSI to request service 1b: The function is permitted to use MSI to request service and is prohibited from using its INTx # pin | No/Yes | 0 |
| 19:17 | Multiple Message Capable | RO | Read as 000b. | No | 000b |
| 22:20 | Multiple Message Enable | RW | Reset to 000b. | No/Yes | 000b |
| 23 | 64-bit address capable | RO | 0b: The function is not capable of generating a 64-bit message address 1b: The function is capable of generating a 64-bit message address | No | 1b |
| 31:24 | Reserved | RO | Not Support. | No | 00h |

8.2.36 MESSAGE ADDRESS REGISTER – OFFSET 4Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-----------------|-------|-------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 1:0 | Reserved | RsvdP | Not Support. | No | 00b |
| 31:2 | Message Address | RW | If the message enable bit is set, the contents of this register specify the DWORD aligned address for MSI memory write transaction. | No/Yes | 0-0h |

8.2.37 MESSAGE UPPER ADDRESS REGISTER – OFFSET 50h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-----------------------|------|-----------------------------------------------------------------------------------------|----------------------|------------|
| 31:0 | Message Upper Address | RW | This register is only effective if the device supports a 64-bit message address is set. | No/Yes | 0000_0000h |

8.2.38 MESSAGE DATA REGISTER – OFFSET 54h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|--------------|------|---------------|----------------------|---------|
| 15:0 | Message Data | RW | Message data. | No/Yes | 0000h |

8.2.39 PCI EXPRESS CAPABILITIES REGISTER – OFFSET 68h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|--------------------------|
| 7:0 | Enhanced Capabilities ID | RO | Read as 10h to indicate that these are PCI express enhanced capability registers. | No | 10h |
| 15:8 | Next Item Pointer | RO | Indicates next capability pointer. | Yes | A4h |
| 19:16 | Capability Version | RO | Read as 2h to indicate the device is compliant to Revision .2.0 of <i>PCI Express Base Specifications</i> . | No | 2h |
| 23:20 | Device/Port Type | RO | Indicates the type of PCI Express logical device. 0101b: upstream port 0110b: downstream port | No | 5h for Up 6h for Down |
| 24 | Slot Implemented | RO | Valid for downstream ports only. When set, indicates that the PCIe Link associated with this Port is connected to a slot. This field is valid for downstream ports of the Switch. | Yes | 0 for Up 1 for Down |
| 29:25 | Interrupt Message Number | RO | No MSI messages are generated in the transparent mode. | No | 00_000b |
| 31:30 | Reserved | RsvdP | Not Support. | No | 00b |

8.2.40 DEVICE CAPABILITIES REGISTER – OFFSET 6Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------------------------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 2:0 | Max_Payload_Size Supported | RO | Indicates the maximum payload size that the device can support for TLPs. 000b: 128 payload size 001b: 256 payload size 010b: 512 payload size | Yes | 001b |
| 4:3 | Phantom Functions Supported | RO | Indicates the support for use of unclaimed function numbers as Phantom functions. Read as 00b, since the Switch does not act as a requester. | No | 00b |
| 5 | Extended Tag Field Supported | RO | Indicates the maximum supported size of Tag field as a Requester. Read as 0, since the Switch does not act as a requester. | No | 0 |
| 8:6 | Endpoint L0s Acceptable Latency | RO | Acceptable total latency that an Endpoint can withstand due to the transition from L0s state to the L0 state. For Switch, the ASPM software would not check this value. | No | 000b |
| 11:9 | Endpoint L1 Acceptable Latency | RO | Acceptable total latency that an Endpoint can withstand due to the transition from L1 state to the L0 state. For Switch, the ASPM software would not check this value. | No | 000b |
| 14:12 | Reserved | RsvdP | Not Support. | No | 000b |
| 15 | Role_Based Error Reporting | RO | When set, indicates that the device implements the functionality originally defined in the Error Reporting ECN. | Yes | 1 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------------------------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 17:16 | Reserved | RsvdP | Not Support. | No | 00b |
| 25:18 | Captured Slot Power Limit Value | RO | It applies to Upstream Port only. In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. This value is set by the Set_Slot_Power_Limit message or hardwired to 0. | No | 00h |
| 27:26 | Captured Slot Power Limit Scale | RO | It applies to Upstream Port only. Specifies the scale used for the Slot Power Limit Value. This value is set by the Set_Slot_Power_Limit message or hardwired to 0. | No | 00b |
| 31:28 | Reserved | RsvdP | Not Support. | No | 0h |

8.2.41 DEVICE CONTROL REGISTER – OFFSET 70h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | Correctable Error Reporting Enable | RW | 0b: Disable Correctable Error Reporting 1b: Enable Correctable Error Reporting | No/Yes | 0 |
| 1 | Non-Fatal Error Reporting Enable | RW | 0b: Disable Non-Fatal Error Reporting 1b: Enable Non-Fatal Error Reporting | No/Yes | 0 |
| 2 | Fatal Error Reporting Enable | RW | 0b: Disable Fatal Error Reporting 1b: Enable Fatal Error Reporting | No/Yes | 0 |
| 3 | Unsupported Request Reporting Enable | RW | 0b: Disable Unsupported Request Reporting 1b: Enable Unsupported Request Reporting | No/Yes | 0 |
| 4 | Enable Relaxed Ordering | RO | When set, it permits the device to set the Relaxed Ordering bit in the attribute field of transaction. Since the Switch cannot either act as a requester or alter the content of packet it forwards, this bit always returns '0' when read. | No | 0 |
| 7:5 | Max_Payload_Size | RW | This field sets maximum TLP payload size for the device. Permissible values that can be programmed are indicated by the Max_Payload_Size Supported in the Device Capabilities register. Any value exceeding the Max_Payload_Size Supported written to this register results into clamping to the Max_Payload_Size Supported value. | No/Yes | 000b |
| 8 | Extended Tag Field Enable | RW | Does not apply to PCI Express Switch. Returns '0' when read. | No | 0 |
| 9 | Phantom Function Enable | RW | Does not apply to PCI Express Switch. Returns '0' when read. | No | 0 |
| 10 | Auxiliary (AUX) Power PM Enable | RO | When set, indicates that a device is enabled to draw AUX power independent of PME AUX power. | No | 0 |
| 11 | Enable No Snoop | RO | When set, it permits to set the No Snoop bit in the attribute field of transaction. Since the Switch cannot either act as a requester or alter the content of packet it forwards, this bit always returns '0' when read. | No | 0 |
| 14:12 | Max_Read_Request_Size | RO | This field sets the maximum Read Request size for the device as a Requester. Since the Switch does not generate read request by itself, these bits are hardwired to 0. | No | 000b |
| 15 | Reserved | RsvdP | Not Support. | No | 0 |

8.2.42 DEVICE STATUS REGISTER – OFFSET 70h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|----------------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 16 | Correctable Error Detected | RW1C | Asserted when correctable error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. | No/Yes | 0 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/I2C-SMBUS | DEFAULT |
|-------|------------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|---------|
| 17 | Non-Fatal Error Detected | RW1C | Asserted when non-fatal error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. | No/Yes | 0 |
| 18 | Fatal Error Detected | RW1C | Asserted when fatal error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. | No/Yes | 0 |
| 19 | Unsupported Request Detected | RW1C | Asserted when unsupported request is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. | No/Yes | 0 |
| 20 | AUX Power Detected | RO | Asserted when the AUX power is detected by the Switch | No | 0 |
| 21 | Transactions Pending | RO | Each port of Switch does not issue Non-posted Requests on its own behalf, so this bit is hardwired to 0. | No | 0 |
| 31:22 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.2.43 LINK CAPABILITIES REGISTER – OFFSET 74h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/I2C-SMBUS | DEFAULT |
|-------|----------------------------------------------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|---------------------------------------------------------------------------|
| 3:0 | Maximum Link Speed | RO | Indicates the maximum speed of the Express link. 0001b: 2.5 Gb/s 0010b: 5.0 Gb/s Others: Reserved | No | 2h |
| 9:4 | Maximum Link Width | HWInt RO | Indicates the maximum width of the given PCIe Link. 00_0001b: x1 link 00_0010b: x2 link 00_0100b: x4 link 00_1000b: x8 link Others: Reserved | No | 08h, 04h, 02h or 01h |
| 11:10 | Active State Power Management (ASPM) Support | RO | Indicates the level of ASPM supported on the given PCIe Link. Each port of Switch supports L0s and L1 entry. | Yes | 01b |
| 14:12 | L0s Exit Latency | RO | Indicates the L0s exit latency for the given PCIe Link. The length of time this port requires to complete transition from L0s to L0 is in the range of 256ns to less than 512ns. | Yes | 011b |
| 17:15 | L1 Exit Latency | RO | Indicates the L1 exit latency for the given PCIe Link. The length of time this port requires to complete transition from L1 to L0 is less than 1us. | Yes | 000b |
| 18 | Clock Power Management | RO | For upstream port, a value of 1b indicates that component tolerates the removal of any reference clock via CLKREQ#. For downstream ports, this bit must be hardwired to 0. | Yes | 1 for Up 0 for Down |
| 19 | Surprise Down Capability Enable | RO | Valid for downstream ports only. | Yes | 0 |
| 20 | Data Link Layer Active Reporting Capable | RO | For downstream ports, this bit must be set to 1b if the component supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine. For a hot-plug capable downstream port, this bit must be set to 1b. For upstream port, this bit must be hardwired to 0. | No | 0 |
| 21 | Link BW Notify Cap. | RO | Valid for downstream ports only. | Yes | 0 for Up 1 for Down |
| 23:22 | Reserved | RsvdP | Not Support. | No | 0 |
| 31:24 | Port Number | RO | Indicates the PCIe Port Number for the given PCIe Link. | Yes | 00h for Up 01 h for Port 1 02h for Port 2 03h for Port 3 |

8.2.44 LINK CONTROL REGISTER – OFFSET 78h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------------------------------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 1:0 | Active State Power Management (ASPM) Control | RW | 00b: ASPM is Disabled 01b: L0s Entry Enabled 10b: L1 Entry Enabled 11b: L0s and L1 Entry Enabled Note that the receiver must be capable of entering L0s even when the field is disabled | No/Yes | 00b |
| 2 | Reserved | RsvdP | Not Support. | No | 0 |
| 3 | Read Completion Boundary (RCB) | RsvdP | Not Support. | No | 0 |
| 4 | Link Disable | RW | At upstream port, it is not allowed to disable the link, so this bit is hardwired to '0'. For downstream ports, it disables the link when this bit is set. | No/Yes | 0 |
| 5 | Retrain Link | RW | At upstream port, it is not allowed to retrain the link, so this bit is hardwired to 0. For downstream ports, it initiates Link Retraining when this bit is set. This bit always returns '0' when read. | No/Yes | 0 |
| 6 | Common Clock Configuration | RW | 0b: The components at both ends of a link are operating with synchronous reference clock 1b: The components at both ends of a link are operating with a distributed common reference clock | No/Yes | 0 |
| 7 | Extended Synch | RW | When set, it transmits 4096 FTS ordered sets in the L0s state for entering L0 state and transmits 1024 TS1 ordered sets in the L1 state for entering L0 state. | No/Yes | 0 |
| 8 | Enable Clock Power Management | RW | Valid for upstream port only. 0b: clock power management is disabled and must hold CLKREQ# low 1b: device is permitted to use CLKREQ# to power manage Link clock | No/Yes | 0 |
| 9 | HW Autonomous Width Disable | RW | Reset to 0b. | No/Yes | 0 |
| 10 | Link Bandwidth Management Interrupt Enable | RW | Valid for downstream ports only. | No/Yes | 0 |
| 11 | Link Autonomous Bandwidth Interrupt Enable | RW | Valid for downstream ports only. | No/Yes | 0 |
| 15:12 | Reserved | RsvdP | Not Support. | No | 0h |

8.2.45 LINK STATUS REGISTER – OFFSET 78h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|----------|
| 19:16 | Link Speed | RO | Indicate the negotiated speed of the Express link. 0001b: 2.5 Gb/s 0010b: 5.0 Gb/s | No | 1h |
| 25:20 | Negotiated Link Width | RO | Indicates the negotiated width of the given PCIe link. 00_0001b: x1 link 00_0010b: x2 link 00_0100b: x4 link 00_1000b: x8 link | No | 00_0001b |
| 26 | Training Error | RO | When set, indicates a Link training error occurred. This bit is cleared by hardware upon successful training of the link to the L0 link state. | No | 0 |
| 27 | Link Training | RO | When set, indicates the link training is in progress. Hardware clears this bit once link training is complete. | No | 0 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|----------------------------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|------------------------|
| 28 | Slot Clock Configuration | RO | 0b: the Switch uses an independent clock irrespective of the presence of a reference on the connector 1b: the Switch uses the same reference clock that the platform provides on the connector | Yes | 1 for Up 0 for Down |
| 29 | Data Link Layer Link Active | RO | Indicates the status of the Data Link Control and Management State Machine. 1b: indicate the DL_Active state 0b: otherwise | No | 0 |
| 30 | Link Bandwidth Management Status | RW1C | Valid for downstream port only. | No/Yes | 0 |
| 31 | Link Autonomous Bandwidth Status | RW1C | Valid for downstream port only. | No/Yes | 0 |

8.2.46 SLOT CAPABILITIES REGISTER – OFFSET 7Ch (Downstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|------------------------------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|------------------------------------------------------------|
| 0 | Attention Button Present | RO | When set, it indicates that an Attention Button is implemented on the chassis for this slot. | Yes | 1 |
| 1 | Power Controller Present | RO | When set, it indicates that a Power Controller is implemented for this slot. | Yes | 1 |
| 2 | MRL Sensor Present | RO | When set, this bit indicates that an MRL Sensor is implemented on the chassis for this slot. | Yes | 1 |
| 3 | Attention Indicator Present | RO | When set, it indicates that an Attention Indicator is implemented on the chassis for this slot | Yes | 1 |
| 4 | Power Indicator Present | RO | When set, it indicates that a Power Indicator is implemented on the chassis for this slot. | Yes | 1 |
| 5 | Hot-Plug Surprise | RO | When set, it indicates that a device present in this slot might be removed from the system without any prior notification. | Yes | 0 |
| 6 | Hot-Plug Capable | HWInt RO | When set, it indicates that this slot is capable of supporting Hot-Plug operation. Without external I/O expander connected, the default value will be clear to 0. | Yes | 0 |
| 14:7 | Slot Power Limit Value | RO | In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. Writes to this register also cause the Port to send the Set Slot Power Limit message. | Yes | 19h |
| 16:15 | Slot Power Limit Scale | RO | Specifies the scale used for the Slot Power Limit Value. Writes to this register also cause the Port to send the Set Slot Power Limit message. | Yes | 00b |
| 17 | EM_INTRELOCK Present | RO | When set, it indicates that an Electromechanical Interlock Present is implemented on the chassis for this slot. | Yes | 0 |
| 18 | No Command Completed Support | RO | When set, it indicates that this slot does not generate software notification when an issued command is completed by the Hot-Plug Controller. | Yes | 0 |
| 31:19 | Physical Slot Number | RO | It indicates the physical slot number attached to this Port. | Yes | 01 h for Port 1 04h for Port 4 05h for Port 5 ... |

8.2.47 SLOT CONTROL REGISTER – OFFSET 80h (Downstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|---------------------------------|------|-----------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | Attention Button Pressed Enable | RW | When set, it enables the generation of Hot-Plug interrupt or wakeup event on an attention button pressed event. | No/Yes | 0 |
| 1 | Power Fault Detected Enable | RW | When set, it enables the generation of Hot-Plug interrupt or wakeup event on a power fault event. | No/Yes | 0 |
| 2 | MRL SENOR ENABLE | RW | When set, it enables the generation of Hot-Plug interrupt or wakeup event on a MRL sensor event. | No/Yes | 0 |
| 3 | Presence Detect Changed Enable | RW | When set, it enables the generation of Hot-Plug interrupt or wakeup event on a presence detect changed event. | No/Yes | 0 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------------------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|----------------------------------------|
| 4 | Command Completed Interrupt Enable | RW | When set, it enables the generation of Hot-Plug interrupt when the Hot-Plug Controller completes a command. It is valid when offset 7Ch[18]=0b. | No/Yes | 0 |
| 5 | Hot-Plug Interrupt Enable | RW | When set, it enables generation of Hot-Plug interrupt on enabled Hot-Plug events. | No/Yes | 0 |
| 7:6 | Attention Indicator Control | RW | Controls the display of Attention Indicator. 00b: Reserved 01b: On 10b: Blink 11b: Off Writes to this register also cause the Port to send the ATTENTION INDICATOR * Messages. | No/Yes | 11b |
| 9:8 | Power Indicator Control | RW | Controls the display of Power Indicator. 00b: Reserved 01b: On 10b: Blink 11b: Off Writes to this register also cause the Port to send the POWER INDICATOR * Messages. | No/Yes | 11b when bit[2]=1 01b when bit[2]=0 |
| 10 | Power Controller Control | RW | 0b: reset the power state of the slot (Power On) 1b: set the power state of the slot (Power Off) | No/Yes | 1 when bit[2]=1 0 when bit[2]=0 |
| 11 | EM_INTRELOCK Control | RW | When set, it enables the generation of Hot-Plug interrupt or wakeup event on an electromechanical interlock present event. | No/Yes | 0 |
| 12 | Data Link Layer State Changed Enable | RW | When set, it enables the generation of Hot-Plug interrupt or wakeup event on a data link layer state changed event. | No/Yes | 0 |
| 15:13 | Reserved | RsvdP | Not Support. | No | 000b |

8.2.48 SLOT STATUS REGISTER – OFFSET 80h (Downstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|--------------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 16 | Attention Button Pressed | RW1C | When set, it indicates the Attention Button is pressed. | No/Yes | 0 |
| 17 | Power Fault Detected | RW1C | When set, it indicates a Power Fault is detected. | No/Yes | 0 |
| 18 | MRL Sensor Changed | RW1C | When set, it indicates a MRL Sensor Changed is detected. | No/Yes | 0 |
| 19 | Presence Detect Changed | RW1C | When set, it indicates a Presence Detect Changed is detected. | No/Yes | 0 |
| 20 | Command Completed | RW1C | When set, it indicates the Hot-Plug Controller completes an issued command. | No/Yes | 0 |
| 21 | MRL Sensor State | RO | Reflects the status of MRL Sensor. 0b: MRL Closed 1b: MRL Opened | No | 0 |
| 22 | Presence Detect State | RO | Indicates the presence of a card in the slot. 0b: Slot Empty 1b: Card Present in slot This register is implemented on all downstream ports that implement slots. For downstream ports not connected to slots (where the Slot Implemented bit of the PCI Express Capabilities register is 0b), this bit returns 1b. | No | 0 |
| 23 | EM_INTRELOCK Status | RO | Indicates the Electromechanical Interlock's current status. 0b: Electromechanical Interlock is disengaged 1b: Electromechanical Interlock is engaged | No | 0 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-------------------------------|-------|--------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 24 | Data Link Layer State Changed | RW1C | This bit is set when the value reported in the Data Link Layer Link Active field of the Link Status register is changed. | No/Yes | 0 |
| 31:25 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.2.49 DEVICE CAPABILITIES REGISTER 2 – OFFSET 8Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|--------------------------|-------|----------------------------------------------------------------------------------------------------------------|----------------------|------------------------|
| 4:0 | Reserved | RsvdP | Not Support. | No | 0_0000b |
| 5 | ARI Forwarding Supported | RO | 0b: ARI forwarding is not supported 1b: ARI forwarding is supported Valid for downstream ports only. | No/Yes | 0 for Up 1 for Down |
| 31:6 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.2.50 DEVICE CONTROL REGISTER 2 – OFFSET 90h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-----------------------|-------|-------------------------------------------------------------------|----------------------|---------|
| 4:0 | Reserved | RsvdP | Not Support. | No | 0_0000b |
| 5 | ARI Forwarding Enable | RW | 0b: Disable 1b: Enable Valid for downstream ports only. | No/Yes | 0 |
| 31:6 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.2.51 DEVICE STATUS REGISTER 2 – OFFSET 90h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------------|------|--------------|----------------------|---------|
| 31:16 | Device Status 2 | RO | Not Support. | No | 0000h |

8.2.52 LINK CAPABILITIES REGISTER 2 – OFFSET 94h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-------------------|------|--------------|----------------------|------------|
| 31:0 | Link Capability 2 | RO | Not Support. | No | 0000_0000h |

8.2.53 LINK CONTROL REGISTER 2 – OFFSET 98h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|-------------------|------|----------------------------------------------------------------------------------------------------------|----------------------|------------------------|
| 3:0 | Target Link Speed | RW | 0001b: target link speed set to 2.5 Gb/s 0010b: target link speed set to 5.0 Gb/s Others: Reserved | No/Yes | 2h |
| 4 | Enter Compliance | RW | 1b: enter compliance mode | No/Yes | 0 |
| 5 | HW AutoSpeed Dis | RW | Reset to 0b. | No/Yes | 0 |
| 6 | Select_Deemp | RW | Valid for downstream ports only. 0b: Select -6.0db de-emphasis 1b: Select -3.5db de-emphasis | Yes | 0 for Up 1 for Down |
| 9:7 | Tran_Margin | RW | Reset to 000b. | No/Yes | 000b |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-------------------------|-------|-------------------------------|----------------------|---------|
| 10 | Enter Modify Compliance | RW | Valid for upstream port only. | No/Yes | 0 |
| 11 | Compliance SOS | RW | Valid for upstream port only. | No/Yes | 0 |
| 12 | Compliance_Deemp | RW | Valid for upstream port only. | No/Yes | 0 |
| 15:13 | Reserved | RsvdP | Not Support. | No | 000b |

8.2.54 LINK STATUS REGISTER 2 – OFFSET 98h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------------------|------|------------------------------------------------------------------------------------|----------------------|------------------------|
| 16 | Current De-emphasis level | RO | 0b: current de-emphasis level is -3.5db 1b: current de-emphasis level is -6.0db | No | 0 for Up 1 for Down |
| 31:17 | Reserved | RO | Not Support. | No | 0-0h |

8.2.55 SLOT CAPABILITIES REGISTER 2 – OFFSET 9Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-------------------|------|--------------|----------------------|------------|
| 31:0 | Slot Capability 2 | RO | Not Support. | No | 0000_0000h |

8.2.56 SLOT CONTROL REGISTER 2 – OFFSET A0h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|----------------|------|--------------|----------------------|---------|
| 15:0 | Slot Control 2 | RO | Not Support. | No | 0000h |

8.2.57 SLOT STATUS REGISTER 2 – OFFSET A0h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------|------|--------------|----------------------|---------|
| 31:16 | Slot Status 2 | RO | Not Support. | No | 0000h |

8.2.58 SSID/SSVID CAPATILITIES REGISTER – OFFSET A4h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------------------|-------|-------------------------------------------------------------------------|----------------------|---------|
| 7:0 | SSID/SSVID Capabilities ID | RO | Read as 0Dh to indicate that these are SSID/SSVID capability registers. | No | 0Dh |
| 15:8 | Next Item Pointer | RO | Read as 00h. No other ECP registers. | Yes | 00h |
| 31:16 | Reserved | RsvdP | Not Support. | No | 0000h |

8.2.59 SUBSYSTEM VENDOR ID REGISTER – OFFSET A8h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|----------|------|-------------------------------------|----------------------|---------|
| 15:0 | SSVID | RO | Indicates the sub-system vendor id. | Yes | 12D8h |

8.2.60 SUBSYSTEM ID REGISTER – OFFSET A8h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------|------|-------------------------------------|----------------------|---------|
| 31:16 | SSID | RO | Indicates the sub-system device id. | Yes | 1224h |

8.2.61 BAR 0-1 CONFIGURATION REGISTER – OFFSET E4h (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-------------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 1:0 | BAR0 Type | RW | Decides whether BAR0 is 32 or 64 bit addressing. 00b: Disable BAR0/1 01b: Reserved 10b: 32-bit addressing 11b: 64-bit addressing | Yes | 10b |
| 2 | BAR0 Prefetchable | RW | 0b: Non Prefetchable 1b: Prefetchable | Yes | 0 |
| 31:3 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.2.62 DEVICE SERIAL NUMBER ENHANCED CAPABILITY HEADER REGISTER – OFFSET 100h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------|------|-----------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 15:0 | Extended Capabilities ID | RO | Read as 0003h to indicate that these are PCI express extended capability registers for device serial number extend capability register. | No | 0003h |
| 19:16 | Capability Version | RO | Must be 1h for this version. | No | 1h |
| 31:20 | Next Capability Offset | RO | Indicates next capability pointer. | Yes | FB4h |

8.2.63 DEVICE SERIAL NUMBER LOWER DW REGISTER – OFFSET 104h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-----------------------------------------|------|---------------------------------------|----------------------|------------|
| 31:0 | Device serial number 1 st DW | RO | First dword for device serial number. | Yes | 0000_0000h |

8.2.64 DEVICE SERIAL NUMBER HIGHER DW REGISTER – OFFSET 108h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-----------------------------------------|------|----------------------------------------|----------------------|------------|
| 31:0 | Device serial number 2 nd DW | RO | Second dword for device serial number. | Yes | 0000_0000h |

8.2.65 PCI EXPRESS POWER BUDGETING ENHANCED CAPABILITY HEADER REGISTER – OFFSET 138h (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------|------|---------------------------------------------------------------------------------------------------------|----------------------|---------|
| 15:0 | Extended Capabilities ID | RO | Read as 0004h to indicate that these are PCI express extended capability registers for power budgeting. | No | 0004h |
| 19:16 | Capability Version | RO | Must be 1h for this version. | No | 01h |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|------------------------|------|------------------------------------|----------------------|---------|
| 31:20 | Next Capability Offset | RO | Indicates next capability pointer. | Yes | 148h |

8.2.66 DATA SELECT REGISTER – OFFSET 13Ch (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|----------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 7:0 | Data Selection | RW | It indexes the power budgeting data reported through the data register. When 00h, it selects D0 Max power budget When 01h, it selects D0 Sustained power budget Other values would return zero power budgets, which means not supported. | No/Yes | 00h |
| 31:8 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.2.67 POWER BUDGETING DATA REGISTER – OFFSET 140h (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------|----------------------|----------------------------------|
| 7:0 | Base Power | RO | It specifies the base power value in watts. This value represents the required power budget in the given operation condition. | Yes | 04h if 13Ch=0 03h if 13Ch=1 |
| 9:8 | Data Scale | RO | It specifies the scale to apply to the base power value. | Yes | 00b |
| 12:10 | PM Sub State | RO | It specifies the power management sub state of the given operation condition. It is initialized to the default sub state. | No | 000b |
| 14:13 | PM State | RO | It specifies the power management state of the given operation condition. It defaults to the D0 power state. | Yes | 00b |
| 17:15 | Type | RO | It specifies the type of the given operation condition which is controlled by offset 13Ch[7:0]. It defaults to the Maximum power state. | Yes | 111b if 13Ch=0 011b if 13Ch=1 |
| 20:18 | Power Rail | RO | It specifies the power rail of the given operation condition.. | No | 010b |
| 31:21 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.2.68 POWER BUDGET CAPABILITY REGISTER – OFFSET 144h (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|------------------|-------|---------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | System Allocated | RO | When set, it indicates that the power budget for the device is included within the system power budget. | Yes | 1 |
| 31:1 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.2.69 PCI EXPRESS VIRTUAL CHANNEL ENHANCED CAPABILITY HEADER REGISTER – OFFSET 148h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------|------|---------------------------------------------------------------------------------------------------------|----------------------|------------------------------|
| 15:0 | Extended Capabilities ID | RO | Read as 0002h to indicate that these are PCI express extended capability registers for virtual channel. | No | 02h |
| 19:16 | Capability Version | RO | Read as 1h. | No | 01h |
| 31:20 | Next Capability Offset | RO | Indicates next capability pointer. | Yes | 270h for Up 520h for Down |

8.2.70 PORT VC CAPABILITY REGISTER 1 – OFFSET 14Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------------------------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 2:0 | Extended VC Count | RO | Indicates the number of extended Virtual Channels in addition to the default VC supported by the Switch. | Yes | 000b |
| 3 | Reserved | RsvdP | Not Support. | No | 0 |
| 6:4 | Low Priority Extended VC Count | RO | Indicates the number of extended Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group. | Yes | 000b |
| 7 | Reserved | RO | Not Support. | No | 0 |
| 9:8 | Reference Clock | RO | Indicates the reference clock for Virtual Channels that support time-based WRR Port Arbitration. Defined encoding is 00b for 100 ns reference clock. | No | 00b |
| 11:10 | Port Arbitration Table Entry Size | RO | Read as 10b to indicate the size of Port Arbitration table entry in the device is 4 bits. | No | 10b |
| 31:12 | Reserved | RsvdP | Not Support. | No | 0000_0h |

8.2.71 PORT VC CAPABILITY REGISTER 2 – OFFSET 150h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|------------------------------|
| 7:0 | VC Arbitration Capability | RO | It indicates the types of VC Arbitration supported by the device for the LPVC group. This field is valid when LPVC is greater than 0. The Switch supports Hardware fixed arbitration scheme, e.g., Round Robin and Weight Round Robin arbitration with 32 phases in LPVC. | No | 00h |
| 23:8 | Reserved | RsvdP | Not Support. | No | 0000h |
| 31:24 | VC Arbitration Table Offset | RO | It indicates the location of the VC Arbitration Table as an offset from the base address of the Virtual Channel Capability register in the unit of DQWD (16 bytes). | No | 00h if VC1=0 04h if VC1=1 |

8.2.72 PORT VC CONTROL REGISTER – OFFSET 154h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|---------------------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | Load VC Arbitration Table | WO | When set, the programmed VC Arbitration Table is applied to the hardware. This bit always returns '0' when read. | Yes | 0 |
| 3:1 | VC Arbitration Select | RW | This field is used to configure the VC Arbitration by selecting one of the supported VC Arbitration schemes. The valid values for the schemes supported by Switch are 0b and 1b. Other value than these written into this register will be treated as default. | No/Yes | 000b |
| 15:4 | Reserved | RsvdP | Not Support. | No | 000h |

8.2.73 PORT VC STATUS REGISTER – OFFSET 154h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 16 | VC Arbitration Table Status | RO | When set, it indicates that any entry of the VC Arbitration Table is written by software. This bit is cleared when hardware finishes loading values stored in the VC Arbitration Table after the bit of "Load VC Arbitration Table" is set. | No | 0 |
| 31:17 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.2.74 VC RESOURCE CAPABILITY REGISTER (0) – OFFSET 158h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-------------------------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|----------|
| 7:0 | Port Arbitration Capability | RO | It indicates the types of Port Arbitration supported by the VC resource. The Switch supports Hardware fixed arbitration scheme, e.g., Round Robin, Weight Round Robin (WRR) arbitration with 128 phases (3~4 enabled ports) and Time-based WRR with 128 phases (3~4 enabled ports). Note that the Time-based WRR is only valid in VC1. | No | 03h |
| 13:8 | Reserved | RsvdP | Not Support. | No | 00 0000h |
| 14 | Advanced Packet Switching | RO | When set, it indicates the VC resource only supports transaction optimized for Advanced Packet Switching (AS). | No | 0 |
| 15 | Reject Snoop Transactions | RsvdP | Not Support. | No | 0 |
| 22:16 | Maximum Time Slots | RO | It indicates the maximum numbers of time slots (minus one) are allocated for Isochronous traffic. | No | 3Fh |
| 23 | Reserved | RsvdP | Not Support. | No | 0 |
| 31:24 | Port Arbitration Table Offset | RO | It indicates the location of the Port Arbitration Table (n) as an offset from the base address of the Virtual Channel Capability register in the unit of DQWD (16 bytes). | No | 05h |

8.2.75 VC RESOURCE CONTROL REGISTER (0) – OFFSET 15Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------------------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 7:0 | TC/VC Map | RW | This field indicates the TCs that are mapped to the VC resource. Bit locations within this field correspond to TC values. When the bits in this field are set, it means that the corresponding TCs are mapped to the VC resource. Bit 0 of this field is read-only and must be set to “1” for the VC0. | Yes | FFh |
| 15:8 | Reserved | RsvdP | Not Support. | No | 00h |
| 16 | Load Port Arbitration Table | RW | When set, the programmed Port Arbitration Table is applied to the hardware. This bit always returns ‘0’ when read. | No/Yes | 0 |
| 19:17 | Port Arbitration Select | RW | This field is used to configure the Port Arbitration by selecting one of the supported Port Arbitration schemes. The permissible values for the schemes supported by Switch are 000b and 011b at VC0, other value than these written into this register will be treated as default. | No/Yes | 000b |
| 23:20 | Reserved | RsvdP | Not Support. | No | 0h |
| 26:24 | VC ID | RO | This field assigns a VC ID to the VC resource. | No | 000b |
| 30:27 | Reserved | RsvdP | Not Support. | No | 0h |
| 31 | VC Enable | RW | 0b: it disables this Virtual Channel 1b: it enables this Virtual Channel | No | 1 |

8.2.76 VC RESOURCE STATUS REGISTER (0) – OFFSET 160h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-------------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 15:0 | Reserved | RsvdP | Not Support. | No | 0000h |
| 16 | Port Arbitration Table Status | RO | When set, it indicates that any entry of the Port Arbitration Table is written by software. This bit is cleared when hardware finishes loading values stored in the Port Arbitration Table after the bit of “Load Port Arbitration Table” is set. | No | 0 |
| 17 | VC Negotiation Pending | RO | When set, it indicates that the VC resource is still in the process of negotiation. This bit is cleared after the VC negotiation is complete. | No | 0 |
| 31:18 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.2.77 VC RESOURCE CAPABILITY REGISTER (1) – OFFSET 164h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-------------------------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|------------------------------|
| 7:0 | Port Arbitration Capability | RO | It indicates the types of Port Arbitration supported by the VC resource. The Switch supports Hardware fixed arbitration scheme, e.g., Round Robin, Weight Round Robin (WRR) arbitration with 128 phases (3~4 enabled ports) and Time-based WRR with 128 phases (3~4 enabled ports). Note that the Time-based WRR is only valid in VC1. | No | 00h if VC1=0 13h if VC1=1 |
| 13:8 | Reserved | RsvdP | Not Support. | No | 0-0h |
| 14 | Advanced Packet Switching | RO | When set, it indicates the VC resource only supports transaction optimized for Advanced Packet Switching (AS). | No | 0 |
| 15 | Reject Snoop Transactions | RO | This bit is not applied to PCIe Switch. | No | 0 |
| 22:16 | Maximum Time Slots | RO | It indicates the maximum numbers of time slots (minus one) are allocated for Isochronous traffic. | Yes | 00h if VC1=0 3Fh if VC1=1 |
| 23 | Reserved | RsvdP | Not Support. | No | 0 |
| 31:24 | Port Arbitration Table Offset | RO | It indicates the location of the Port Arbitration Table (n) as an offset from the base address of the Virtual Channel Capability register in the unit of DQWD (16 bytes). | No | 00h if VC1=0 06h if VC1=1 |

8.2.78 VC RESOURCE CONTROL REGISTER (1) – OFFSET 168h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------------------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|--------------------------------|
| 7:0 | TC/VC Map | RW | This field indicates the TCs that are mapped to the VC resource. Bit locations within this field correspond to TC values. When the bits in this field are set, it means that the corresponding TCs are mapped to the VC resource. Bit 0 of this field is read-only and must be set to “0” for the VC1. | Yes | 00h |
| 15:8 | Reserved | RsvdP | Not Support. | No | 00h |
| 16 | Load Port Arbitration Table | RW | When set, the programmed Port Arbitration Table is applied to the hardware. This bit always returns 0b when read. | No/Yes | 0 |
| 19:17 | Port Arbitration Select | RW | This field is used to configure the Port Arbitration by selecting one of the supported Port Arbitration schemes. The permissible values for the schemes supported by Switch are 000b, 011b and 100b at VC1, other value than these written into this register will be treated as default. | No/Yes | 000b |
| 23:20 | Reserved | RsvdP | Not Support. | No | 0h |
| 26:24 | VC ID | RW | This field assigns a VC ID to the VC resource. | No/Yes | 000b if VC1=0 001b if VC1=1 |
| 30:27 | Reserved | RsvdP | Not Support. | No | 0h |
| 31 | VC Enable | RW | 0b: it disables this Virtual Channel 1b: it enables this Virtual Channel | No/Yes | 0 |

8.2.79 VC RESOURCE STATUS REGISTER (1) – OFFSET 16Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-------------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 15:0 | Reserved | RsvdP | Not Support. | No | 0000h |
| 16 | Port Arbitration Table Status | RO | When set, it indicates that any entry of the Port Arbitration Table is written by software. This bit is cleared when hardware finishes loading values stored in the Port Arbitration Table after the bit of “Load Port Arbitration Table” is set. | No | 0 |
| 17 | VC Negotiation Pending | RO | When set, it indicates that the VC resource is still in the process of negotiation. This bit is cleared after the VC negotiation is complete. | No | 0 |
| 31:18 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.2.80 VC ARBITRATION TABLE REGISTER – OFFSET 188h

The VC arbitration table is a read-write register array that contains a table for VC arbitration. Each table entry allocates four bits, of which three bits are used to represent VC ID and one bit is reserved. A total of 32 entries are used to construct the VC arbitration table. The layout for this register array is shown below.

Table 8-2 Register Array Layout for VC Arbitration

| 31 - 28 | 27 - 24 | 23 - 20 | 19 - 16 | 15 - 12 | 11 - 8 | 7 - 4 | 3 - 0 | Byte Location | EEPROM/ I2C-SMBUS | DEFAULT |
|------------|------------|------------|------------|------------|------------|------------|------------|---------------|----------------------|------------|
| Phase [7] | Phase [6] | Phase [5] | Phase [4] | Phase [3] | Phase [2] | Phase [1] | Phase [0] | 00h | No/Yes | 0000_0000h |
| Phase [15] | Phase [14] | Phase [13] | Phase [12] | Phase [11] | Phase [10] | Phase [9] | Phase [8] | 04h | No/Yes | 0000_0000h |
| Phase [23] | Phase [22] | Phase [21] | Phase [20] | Phase [19] | Phase [18] | Phase [17] | Phase [16] | 08h | No/Yes | 0000_0000h |
| Phase [31] | Phase [30] | Phase [29] | Phase [28] | Phase [27] | Phase [26] | Phase [25] | Phase [24] | 0Ch | No/Yes | 0000_0000h |

8.2.81 PORT ARBITRATION TABLE REGISTER (0) and (1) – OFFSET 198h and 1A8h

The Port arbitration table is a read-write register array that contains a table for Port arbitration. Each table entry allocates two bits to represent Port Number. The table entry size is dependent on the number of enabled ports (refer to bit 10 and 11 of Port VC capability register 1). The arbitration table contains 32 entries if three or four ports are to be enabled. The following table shows the register array layout for the size of entry equal to two.

Table 8-3 Table Entry Size in 4 Bits

| 31 - 24 | 23 - 16 | 15 - 8 | 7 - 0 | Byte Location | EEPROM/ I2C-SMBUS | DEFAULT |
|---------------|---------------|---------------|---------------|---------------|----------------------|------------|
| Phase [7:6] | Phase [5:4] | Phase [3:2] | Phase [1:0] | 00h | No/Yes | 0000_0000h |
| Phase [15:14] | Phase [13:12] | Phase [11:10] | Phase [9:8] | 04h | No/Yes | 0000_0000h |
| Phase [23:22] | Phase [21:20] | Phase [19:18] | Phase [17:16] | 08h | No/Yes | 0000_0000h |
| Phase [31:30] | Phase [29:28] | Phase [27:26] | Phase [25:24] | 0Ch | No/Yes | 0000_0000h |

8.2.82 ECC ERROR CHECK DISABLE REGISTER – OFFSET 1C8h (Global)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|------------------------------------------------------------|-------|-------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 3:0 | Reserved | RW | Test used only. | No/Yes | 000 |
| 4 | Enable INTA_L for Hot Plug or Link State Event | RW | 0b: Send an INTx Message for Hot Plug or Link State Event 1b: Assert INTA_L for Hot Plug or Link State Event | No/Yes | 0 |
| 5 | Reserved | RW | Test used only. | No/Yes | 0 |
| 6 | Enable INTA_L for GPIO-Generated Interrupts | RW | 0b: Send an INTx Message for GPIO Interrupt Requests 1b: Assert INTA_L for GPIO Interrupt Requests | No/Yes | 0 |
| 7 | Enable INTA_L for NT Virtual Doorbell-Generated Interrupts | RW | 0b: Send an INTx Message for NT Virtual Doorbell Interrupt Requests 1b: Assert INTA_L for NT Virtual Doorbell Interrupt Requests | No/Yes | 0 |
| 31: 8 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.2.83 NT-UP PORT SELECTION REGISTER – OFFSET 1DCh (Global)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-------------------|-------------|-------------------------------------------------------------------------|----------------------|---------|
| 7:0 | Reserved | RsvdP | Not Support. | No | 00h |
| 10:8 | UP_PORT_SEL | HWInt RW | Used to select Upstream Port when Bit[15]=1. | No/Yes | 000b |
| 14:13 | Reserved | RsvdP | Not Support. | No | 00 |
| 15 | Software_CFG_Mode | RW | When set to 1, UP and NT Ports are decided by Bit[11:8] and Bit[27:24]. | No/Yes | 0 |
| 23:16 | Reserved | RsvdP | Not Support. | No | 00h |
| 26:24 | NT_PORT_SEL | HwInt RW | Used to select NT Port when Bit[15]=1. | No/Yes | 000b |
| 31:27 | Reserved | RsvdP | Not Support. | No | 0-0b |

8.2.84 HOT PLUG CONFIGURATION REGISTER – OFFSET 1E0h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 1:0 | Reserved | RsvdP | Not Support. | No | 00b |
| 2 | HPC_PME_TURN_OFF_En | RW | Valid for downstream ports only. 0b: disable to send out PME_TURN_OFF message. 1b: enable to send out PME_TURN_OFF message. | Yes | 0 |
| 4:3 | HPC_Timer | RW | Valid for downstream ports only. Used to set hot plug port timer. 00b: Reserved 01b: 128 ms 10b: 256 ms 11b: 512 ms | Yes | 01b |
| 5 | Reserved | RsvdP | Not Support. | No | 0 |
| 6 | HPC_PG_ActiveLow_En | RW | Valid for downstream ports only. 0b: PWR_GOODx pins are Active high. 1b: PWR_GOODx pins are Active low. | Yes | 0 |
| 11:7 | Reserved | RsvdP | Not Support. | No | 0-0h |
| 12 | NT_Serial_HotPlug_En | RW | Valid for NT port only. 0b: disable serial hot plug capability on NT port. 1b: enable serial hot plug capability on NT port. | No | 0 |
| 14:7 | Reserved | RsvdP | Not Support. | No | 0-0h |
| 15 | IOE_Cmd_In_Progress | RO | Indicates that the Write command to an IOE (I/O Expander) GPIOx Output Data register is still in progress. | No | 0 |
| 16 | HPC_Serial_HotPlug_Disable | RW | Valid for upstream port only. 0b: enable serial hot plug capability for all downstream ports. 1b: disable serial hot plug capability for all downstream ports. | Yes | 0 |
| 17 | IOE_40Bit_En | RW | Valid for upstream port only. 0b: enable 16-pin IOE for all downstream ports. 1b: enable 40-pin IOE for all downstream ports. | Yes | 0 |
| 18 | HPC_GPIO_Dir | RW | 0b: set GPIO direction to input pin 1b: set GPIO direction to output pin | Yes | 0 |
| 19 | HPC_GPIO_Value | RW | I/O Expander GPIO Value. | Yes | 0 |
| 20 | HPC_I/O_Reload | RW | 1b: the value of Hotplug Controller Output pin is reloaded. This bit is self clearing. | Yes | 0 |
| 26:21 | HPC_Output_Reload_Value | RW | When Bit [20] is set, values from this field are reloaded. | Yes | 000b |
| 31:27 | Reserved | RsvdP | Not Support. | No | 0000_0b |

8.2.85 SOFTWARE LANE STATUS REGISTER – OFFSET 1F4h (Global)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|----------------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|------------|
| 31:0 | Software Lane Status | RO | Indicates current lane status. 0b: link down 1b: link up Bit[7:0]: for Lane 7 to Lane 0 Bit[15:8]: for Lane 23 to Lane 16 Bit[23:16]: for Lane 15 to Lane 8 Others: Reserved | No | 0000_0000h |

8.2.86 DE-EMPHASIS AND RATE CONTROL REGISTER – OFFSET 208h (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|------------------|------|---------------------------------------------------------|----------------------|---------|
| 15:0 | Rate Ctrl | RW | Test used only. 0h: GEN1 speed 1h: GEN2 speed | No/Yes | 0000h |
| 31:16 | De-emphasis Ctrl | RW | Test used only. 0h: -6 dB 1h: -3.5 dB | No/Yes | 0000h |

8.2.87 COMPLIANCE MODE CONTROL REGISTER – OFFSET 20Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------------|-------|--------------------------------------------------|----------------------|---------|
| 11:0 | Compliance Mode | RW | Test used only. 1h: enter Compliance mode | No/Yes | 000h |
| 31:12 | Reserved | RsvdP | Not Support. | No | 0_0000h |

8.2.88 EVEN PORT PHYSICAL LAYER COMMAND AND STATUS REGISTER – OFFSET 220h (Global)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|----------------------------|-------|-----------------|----------------------|---------|
| 0 | PORT0_Loopback_CMD | RW | Test used only. | No/Yes | 0 |
| 1 | PORT0_Scramble_Disable_CMD | RW | Test used only. | No/Yes | 0 |
| 2 | PORT0_Compliance_Receive | RW | Test used only. | No/Yes | 0 |
| 3 | Reserved | RsvdP | Not Support. | No | 0 |
| 4 | PORT2_Loopback_CMD | RW | Test used only. | No/Yes | 0 |
| 5 | PORT2_Scramble_Disable_CMD | RW | Test used only. | No/Yes | 0 |
| 6 | PORT2_Compliance_Receive | RW | Test used only. | No/Yes | 0 |
| 7 | Reserved | RsvdP | Not Support. | No | 0 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------------------------|-------|-----------------|----------------------|---------|
| 8 | PORT4_Loopback_CMD | RW | Test used only. | No/Yes | 0 |
| 9 | PORT4_Scramble_Disable_CMD | RW | Test used only. | No/Yes | 0 |
| 10 | PORT4_Compliance_Receive | RW | Test used only. | No/Yes | 0 |
| 11 | Reserved | RsvdP | Not Support. | No | 0 |
| 12 | PORT6_Loopback_CMD | RW | Test used only. | No/Yes | 0 |
| 13 | PORT6_Scramble_Disable_CMD | RW | Test used only. | No/Yes | 0 |
| 14 | PORT6_Compliance_Receive | RW | Test used only. | No/Yes | 0 |
| 15 | Reserved | RsvdP | Not Support. | No | 0 |
| 16 | PORT8_Loopback_CMD | RW | Test used only. | No/Yes | 0 |
| 17 | PORT8_Scramble_Disable_CMD | RW | Test used only. | No/Yes | 0 |
| 18 | PORT8_Compliance_Receive | RW | Test used only. | No/Yes | 0 |
| 19 | Reserved | RsvdP | Not Support. | No | 0 |
| 20 | PORT10_Loopback_CMD | RW | Test used only. | No/Yes | 0 |
| 21 | PORT10_Scramble_Disable_CMD | RW | Test used only. | No/Yes | 0 |
| 22 | PORT10_Compliance_Receive | RW | Test used only. | No/Yes | 0 |
| 31:23 | Reserved | RsvdP | Not Support. | No | 00h |

8.2.89 ODD PORT PHYSICAL LAYER COMMAND AND STATUS REGISTER – OFFSET 224h (Global)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|----------------------------|-------|-----------------|----------------------|---------|
| 0 | PORT1_Loopback_CMD | RW | Test used only. | No/Yes | 0 |
| 1 | PORT1_Scramble_Disable_CMD | RW | Test used only. | No/Yes | 0 |
| 2 | PORT1_Compliance_Receive | RW | Test used only. | No/Yes | 0 |
| 3 | Reserved | RsvdP | Not Support. | No | 0 |
| 4 | PORT3_Loopback_CMD | RW | Test used only. | No/Yes | 0 |
| 5 | PORT3_Scramble_Disable_CMD | RW | Test used only. | No/Yes | 0 |
| 6 | PORT3_Compliance_Receive | RW | Test used only. | No/Yes | 0 |
| 7 | Reserved | RsvdP | Not Support. | No | 0 |
| 8 | PORT5_Loopback_CMD | RW | Test used only. | No/Yes | 0 |
| 9 | PORT5_Scramble_Disable_CMD | RW | Test used only. | No/Yes | 0 |
| 10 | PORT5_Compliance_Receive | RW | Test used only. | No/Yes | 0 |
| 11 | Reserved | RsvdP | Not Support. | No | 0 |
| 12 | PORT7_Loopback_CMD | RW | Test used only. | No/Yes | 0 |
| 13 | PORT7_Scramble_Disable_CMD | RW | Test used only. | No/Yes | 0 |
| 14 | PORT7_Compliance_Receive | RW | Test used only. | No/Yes | 0 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------------------------|-------|-----------------|----------------------|---------|
| 15 | Reserved | RsvdP | Not Support. | No | 0 |
| 16 | PORT9_Loopback_CMD | RW | Test used only. | No/Yes | 0 |
| 17 | PORT9_Scramble_Disable_CMD | RW | Test used only. | No/Yes | 0 |
| 18 | PORT9_Compliance_Receive | RW | Test used only. | No/Yes | 0 |
| 19 | Reserved | RsvdP | Not Support. | No | 0 |
| 20 | PORT11_Loopback_CMD | RW | Test used only. | No/Yes | 0 |
| 21 | PORT11_Scramble_Disable_CMD | RW | Test used only. | No/Yes | 0 |
| 22 | PORT11_Compliance_Receive | RW | Test used only. | No/Yes | 0 |
| 31:23 | Reserved | RsvdP | Not Support. | No | 00h |

8.2.90 EVEN PORT DISABLE/QUIET/TEST PATTERN RATE REGISTER – OFFSET 230h (Global)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------------------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 7:0 | Even Port Disable | RW | 0b: enable LTSSM operation. 1b: force LTSSM in the Detect.Quiet state. Bit[5:0]: for Port 0, 2, 4, 6, 8, 10 Others: Reserved | No/Yes | 00h |
| 15:8 | Even Port Quiet | RW | 0b: LTSSM is allowed to exit the Detect.Quiet state 1b: LTSSM remains in the Detect.Quiet state Bit[5:0]: for Port 0, 2, 4, 6, 8, 10 Others: Reserved | No/Yes | 00h |
| 23:16 | Even Port Test Pattern Rate | RW | Test used only. | No/Yes | 00h |
| 31:24 | Reserved | RsvdP | Not Support. | No | 00h |

8.2.91 ODD PORT DISABLE/QUIET/TEST PATTERN RATE REGISTER – OFFSET 234h (Global)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 7:0 | Odd Port Disable | RW | 0b: enable LTSSM operation 1b: force LTSSM in the Detect.Quiet state Bit[5:0]: for Port 1, 3, 5, 7, 9, 11 Others: Reserved | No/Yes | 00h |
| 15:8 | Odd Port Quiet | RW | 0b: LTSSM is allowed to exit the Detect.Quiet state 1b: LTSSM remains in the Detect.Quiet state Bit[5:0]: for Port 1, 3, 5, 7, 9, 11 Others: Reserved | No/Yes | 00h |
| 23:16 | Odd Port Test Pattern Rate | RW | Test used only. | No/Yes | 00h |
| 31:24 | Reserved | RsvdP | Not Support. | No | 00h |

8.2.92 L1 PM SUBSTATES ENHANCED CAPABILITY HEADER – OFFSET 270h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|------------------------------------|------|-------------------------------------------------------------------------------------------------------|----------------------|---------|
| 15:0 | PCI Express Extended Capability ID | RO | Read as 001Eh to indicate PCI Express Extended Capability ID for L1 PM Substates Extended Capability. | No | 001Eh |
| 19:16 | Capability Version | RO | Must be 1h for this version. | No | 1h |
| 31:20 | Next Capability Offset | RO | Indicates next capability pointer. | Yes | 900h |

8.2.93 L1 PM SUBSTATES CAPABILITY REGISTER – OFFSET 274h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|---------------------------|-------|----------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | Reserved | RsvdP | Not Support. | No | 0 |
| 1 | PCI-PM L1.1 Supported | RO | When set this bit indicates that PCI-PM L1.1 is supported and must be set by all ports implementing L1 PM Substates. | Yes | 1 |
| 2 | Reserved | RO | Not Support. | No | 0 |
| 3 | ASPM L1.1 Supported | RO | When set this bit indicates that ASPM L1.1 is supported. | Yes | 0 |
| 4 | L1 PM Substates Supported | RO | When set this bit indicates that this port supports L1 PM Substates. | Yes | 1 |
| 31:5 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.2.94 L1 PM SUBSTATES CONTROL 1 REGISTER – OFFSET 278h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|--------------------|-------|-----------------------------------------------------------------------------------------|----------------------|---------|
| 0 | Reserved | RsvdP | Not Support. | No | 0 |
| 1 | PCI-PM L1.1 Enable | RW | When set this bit enables PCI-PM L1.1. Required for both upstream and downstream ports. | No/Yes | 0 |
| 2 | Reserved | RsvdP | Not Support. | No | 0 |
| 3 | ASPM L1.1 Enable | RW | When set this bit enables ASPM L1.1. Required for both upstream and downstream ports. | No/Yes | 0 |
| 31:4 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.2.95 L1 PM SUBSTATES CONTROL 2 REGISTER – OFFSET 27Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|----------|-------|--------------|----------------------|------------|
| 31:0 | Reserved | RsvdP | Not Support. | No | 0000 0000h |

8.2.96 SMBUS CONTROL AND STATUS REGISTER – OFFSET 344h (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|-------------------|-------------|-----------------------------------------------------------------------------------------|----------------------|-----------|
| 0 | SMBus Enable | HWInt RW | 0b: disable SMBUS, enable I2C 1b: enable SMBUS | No/Yes | 0 |
| 7:1 | SMBUS Address | HwInt RW | Set SMBUS Address. Bit [3:1] are decided by the status of strapped pins (GPIO[7:5]). | No/Yes | 0111_000b |
| 8 | ARP Disable | RW | Test used only. | No/Yes | 1 |
| 9 | PEC Check Disable | RW | 0b: enable PEC check 1b: disable PEC check | No/Yes | 1 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------------------|-------|--------------------------------------------------------------|----------------------|---------|
| 10 | AV Flag | RW | Test used only. | No/Yes | 0 |
| 11 | AR Flag | RW | Test used only. | No/Yes | 0 |
| 13:12 | UDID Addr Type | RW | Test used only. | No/Yes | 00b |
| 14 | UDID PEC Support | RW | Test used only. | No/Yes | 1 |
| 15 | Reserved | RsvdP | Not Support. | No | 0 |
| 23:16 | UDID Vendor ID | RW | Test used only. | No/Yes | B0h |
| 26:24 | UDID Revision ID | RW | Test used only. | No/Yes | 001b |
| 27 | Fty Test 0 | RW | Test used only. | No/Yes | 0 |
| 28 | SMBUS In Progress | RO | 0b: SMBUS interface is idle. 1b: SMBUS interface is busy. | No | 0 |
| 29 | PEC Check Fail | RO | 0b: PEC check successfully 1b: PEC check failed | No | 0 |
| 30 | Unsupported SMBUS Command | RO | 0b: supported command. 1b: unsupported command. | No | 0 |
| 31 | Reserved | RO | Not Support. | No | 1 |

8.2.97 DISABLE DOWNSTREAM PORT HOT RESET REGISTER – OFFSET 34Ch (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|------------------|-------|------------------------------------|----------------------|---------|
| 0 | DN_Hot_Reset_Dis | RW | Disable downstream port hot reset. | Yes | 0 |
| 31:1 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.2.98 ACS ENHANCED CAPABILITY HEADER REGISTER – OFFSET 520h (Downstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|------------------------------------|------|-------------------------------------------------------------------------------------------|----------------------|---------|
| 15:0 | PCI Express Extended Capability ID | RO | Read as 000Dh to indicate PCI Express Extended Capability ID for ACS Extended Capability. | No | 0Dh |
| 19:16 | Capability Version | RO | Must be 1h for this version. | No | 1h |
| 31:20 | Next Capability Offset | RO | Indicates next capability pointer. | Yes | 270h |

8.2.99 ACS CAPABILITY REGISTER – OFFSET 524h (Downstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|-----------------------------|-------|---------------------------------------------------------|----------------------|---------|
| 0 | ACS Source Validation | RO | Indicates the implements of ACS Source Validation. | No | 1 |
| 1 | ACS Translation Blocking | RO | Indicates the implements of ACS Translation Blocking. | No | 1 |
| 2 | ACS P2P Request Redirect | RO | Indicates the implements of ACS P2P Request Redirect. | No | 1 |
| 3 | ACS P2P Completion Redirect | RO | Indicates the implements of ACS P2P Completion Redirect | No | 1 |
| 4 | ACS Upstream Forwarding | RO | Indicates the implements of ACS Upstream Forwarding. | No | 1 |
| 5 | ACS P2P Egress control | RO | Indicates the implements of ACS P2P Egress control. | No | 1 |
| 6 | ACS Direct Translated P2P | RO | Indicates the implements of ACS Direct Translated P2P. | No | 1 |
| 7 | Reserved | RsvdP | Not Support. | No | 0 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|------------------------------------|-------|---------------------------------------------------------------------------------------------------|----------------------|---------|
| 15:8 | Egress Control Vector Size | RO | Encodings 01h – FFh directly indicate the number of applicable bits in the Egress Control Vector. | No | 10h |
| 16 | ACS Source Validation Enable | RW | 0b: disable the source validation 1b: enable the source validation | No/Yes | 0 |
| 17 | ACS Translation Blocking Enable | RW | 0b: disable ACS translation blocking 1b: enable ACS translation blocking | No/Yes | 0 |
| 18 | ACS P2P Request Redirect | RW | 0b: disable ACS P2P request redirect 1b: enable ACS P2P request redirect | No/Yes | 0 |
| 19 | ACS P2P Completion Redirect Enable | RW | 0b: disable ACS P2P completion redirect 1b: enable ACS P2P completion redirect | No/Yes | 0 |
| 20 | ACS Upstream Forwarding Enable | RW | 0b: disable ACS upstream forwarding 1b: enables ACS upstream forwarding | No/Yes | 0 |
| 21 | ACS P2P Egress control Enable | RW | 0b: disable ACS P2P egress control 1b: enable ACS P2P egress control | No/Yes | 0 |
| 22 | ACS Direct Translated P2P Enable | RW | 0b: disable ACS direct translated P2P 1b: enable ACS Direct Translated P2P | No/Yes | 0 |
| 31:23 | Reserved | RsvdP | Not Support. | No | 00h |

8.2.100 EGRESS CONTROL VECTOR REGISTER – OFFSET 528h (Downstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------------------|-------|---------------------------------------------------------------------------------------------------------|----------------------|---------|
| 15:0 | Egress Control Vector | RW | When a given bit is set, peer-to-peer requests targeting the associated Port are blocked or redirected. | No/Yes | 0000h |
| 31:16 | Reserved | RsvdP | Not Support. | No | 0000h |

8.2.101 GPIO 0-15 DIRECTION CONTROL REGISTER – OFFSET 62Ch (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|----------------------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | GPIO[0] Source/Destination | RW | As Input: 0b: Input Data Register (offset 63Ch[0]) 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[0] Output Data register (offset 644h[0]) 1b: Serial Hot Plug PERST# output for Hot Plug Port 0 | No/Yes | 0 |
| 1 | GPIO[0] Direction Control | RW | 0b: Input 1b: Output | No/Yes | 0 |
| 2 | GPIO[1] Source/Destination | RW | As Input: 0b: Input Data Register (offset 63Ch[1]) 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[1] Output Data register (offset 644h[1]) 1b: Serial Hot Plug PERST# output for Hot Plug Port 1 | No/Yes | 0 |
| 3 | GPIO[1] Direction Control | RW | 0b: Input 1b: Output | No/Yes | 0 |
| 4 | GPIO[2] Source/Destination | RW | As Input: 0b: Input Data Register (offset 63Ch[2]) 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[2] Output Data register (offset 644h[2]) 1b: Serial Hot Plug PERST# output for Hot Plug Port 2 | No/Yes | 0 |
| 5 | GPIO[2] Direction Control | RW | 0b: Input 1b: Output | No/Yes | 0 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|--------------------------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 6 | GPIO[3] Source/Destination | RW | As Input: 0b: Input Data Register (offset 63Ch[3]) 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[3] Output Data register (offset 644h[3]) 1b: Serial Hot Plug PERST# output for Hot Plug Port 3 | No/Yes | 0 |
| 7 | GPIO[3] Direction Control | RW | 0b: Input 1b: Output | No/Yes | 0 |
| 8 | GPIO[4] Source/Destination | RW | As Input: 0b: Input Data Register (offset 63Ch[4]) 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[4] Output Data register (offset 644h[4]) 1b: Serial Hot Plug PERST# output for Hot Plug Port 4 | No/Yes | 0 |
| 9 | GPIO[4] Direction Control | RW | 0b: Input 1b: Output | No/Yes | 0 |
| 10 | GPIO[5] Source/Destination | RW | As Input: 0b: Input Data Register (offset 63Ch[5]) 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[5] Output Data register (offset 644h[5]) 1b: Serial Hot Plug PERST# output for Hot Plug Port 5 | No/Yes | 0 |
| 11 | GPIO[5] Direction Control | RW | 0b: Input 1b: Output | No/Yes | 0 |
| 12 | GPIO[6] Source/Destination | RW | As Input: 0b: Input Data Register (offset 63Ch[6]) 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[6] Output Data register (offset 644h[6]) 1b: Serial Hot Plug PERST# output for Hot Plug Port 6 | No/Yes | 0 |
| 13 | GPIO[6] Direction Control | RW | 0b: Input 1b: Output | No/Yes | 0 |
| 14 | GPIO[7] Source/Destination | RW | As Input: 0b: Input Data Register (offset 63Ch[7]) 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[7] Output Data register (offset 644h[7]) 1b: Serial Hot Plug PERST# output for Hot Plug Port 7 | No/Yes | 0 |
| 15 | GPIO[7] Direction Control | RW | 0b: Input 1b: Output | No/Yes | 0 |
| 16 | GPIO[8] Source/Destination | RW | As Input: 0b: Input Data Register (offset 63Ch[8]) 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[8] Output Data register (offset 644h[8]) 1b: Serial Hot Plug PERST# output for Hot Plug Port 8 | No/Yes | 0 |
| 17 | GPIO[8] Direction Control | RW | 0b: Input 1b: Output | No/Yes | 0 |
| 18 | GPIO[9] Source/Destination | RW | As Input: 0b: Input Data Register (offset 63Ch[9]) 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[9] Output Data register (offset 644h[9]) 1b: Serial Hot Plug PERST# output for Hot Plug Port 9 | No/Yes | 0 |
| 19 | GPIO[9] Direction Control | RW | 0b: Input 1b: Output | No/Yes | 0 |
| 20 | GPIO[10] Source/Destination | RW | As Input: 0b: Input Data Register (offset 63Ch[10]) 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[10] Output Data register (offset 644h[10]) 1b: Serial Hot Plug PERST# output for Hot Plug Port 10 | No/Yes | 0 |
| 21 | GPIO[10] Direction Control | RW | 0b: Input 1b: Output | No/Yes | 0 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|--------------------------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 22 | GPIO[11] Source/Destination | RW | As Input: 0b: Input Data Register (offset 63Ch[11]) 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[11] Output Data register (offset 644h[11]) 1b: Serial Hot Plug PERST# output for Hot Plug Port 11 | No/Yes | 0 |
| 23 | GPIO[11] Direction Control | RW | 0b: Input 1b: Output | No/Yes | 0 |
| 24 | GPIO[12] Source/Destination | RW | As Input: 0b: Input Data Register (offset 63Ch[12]) 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[12] Output Data register (offset 644h[12]) 1b: Serial Hot Plug PERST# output for Hot Plug Port 12 | No/Yes | 0 |
| 25 | GPIO[12] Direction Control | RW | 0b: Input 1b: Output | No/Yes | 0 |
| 26 | GPIO[13] Source/Destination | RW | As Input: 0b: Input Data Register (offset 63Ch[13]) 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[13] Output Data register (offset 644h[13]) 1b: Serial Hot Plug PERST# output for Hot Plug Port 13 | No/Yes | 0 |
| 27 | GPIO[13] Direction Control | RW | 0b: Input 1b: Output | No/Yes | 0 |
| 28 | GPIO[14] Source/Destination | RW | As Input: 0b: Input Data Register (offset 63Ch[14]) 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[14] Output Data register (offset 644h[14]) 1b: Serial Hot Plug PERST# output for Hot Plug Port 14 | No/Yes | 0 |
| 29 | GPIO[14] Direction Control | RW | 0b: Input 1b: Output | No/Yes | 0 |
| 30 | GPIO[15] Source/Destination | RW | As Input: 0b: Input Data Register (offset 63Ch[15]) 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[15] Output Data register (offset 644h[15]) 1b: Serial Hot Plug PERST# output for Hot Plug Port 15 | No/Yes | 0 |
| 31 | GPIO[15] Direction Control | RW | 0b: Input 1b: Output | No/Yes | 0 |

8.2.102 GPIO 16-31 DIRECTION CONTROL REGISTER – OFFSET 630h (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|--------------------------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | GPIO[16] Source/Destination | RW | As Input: 0b: Input Data Register (offset 640h[0]) 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[16] Output Data register (offset 648h[0]) 1b: Reserved | No/Yes | 0 |
| 1 | GPIO[16] Direction Control | RW | 0b: Input 1b: Output | No/Yes | 0 |
| 2 | GPIO[17] Source/Destination | RW | As Input: 0b: Input Data Register (offset 640h[1]) 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[17] Output Data register (offset 648h[1]) 1b: Reserved | No/Yes | 0 |
| 3 | GPIO[17] Direction Control | RW | 0b: Input 1b: Output | No/Yes | 0 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|--------------------------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 4 | GPIO[18] Source/Destination | RW | As Input: 0b: Input Data Register (offset 640h[2]) 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[18] Output Data register (offset 648h[2]) 1b: Reserved | No/Yes | 0 |
| 5 | GPIO[18] Direction Control | RW | 0b: Input 1b: Output | No/Yes | 0 |
| 6 | GPIO[19] Source/Destination | RW | As Input: 0b: Input Data Register (offset 640h[3]) 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[19] Output Data register (offset 648h[3]) 1b: Reserved | No/Yes | 0 |
| 7 | GPIO[19] Direction Control | RW | 0b: Input 1b: Output | No/Yes | 0 |
| 8 | GPIO[20] Source/Destination | RW | As Input: 0b: Input Data Register (offset 640h[4]) 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[20] Output Data register (offset 648h[4]) 1b: Reserved | No/Yes | 0 |
| 9 | GPIO[20] Direction Control | RW | 0b: Input 1b: Output | No/Yes | 0 |
| 10 | GPIO[21] Source/Destination | RW | As Input: 0b: Input Data Register (offset 640h[5]) 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[21] Output Data register (offset 648h[5]) 1b: Reserved | No/Yes | 0 |
| 11 | GPIO[21] Direction Control | RW | 0b: Input 1b: Output | No/Yes | 0 |
| 12 | GPIO[22] Source/Destination | RW | As Input: 0b: Input Data Register (offset 640h[6]) 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[22] Output Data register (offset 648h[6]) 1b: Reserved | No/Yes | 0 |
| 13 | GPIO[22] Direction Control | RW | 0b: Input 1b: Output | No/Yes | 0 |
| 14 | GPIO[23] Source/Destination | RW | As Input: 0b: Input Data Register (offset 640h[7]) 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[23] Output Data register (offset 648h[7]) 1b: Reserved | No/Yes | 0 |
| 15 | GPIO[23] Direction Control | RW | 0: Input 1: Output | No/Yes | 0 |
| 16 | GPIO[24] Source/Destination | RW | As Input: 0b: Input Data Register (offset 640h[8]) 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[24] Output Data register (offset 648h[8]) 1b: Reserved | No/Yes | 0 |
| 17 | GPIO[24] Direction Control | RW | 0b: Input 1b: Output | No/Yes | 0 |
| 18 | GPIO[25] Source/Destination | RW | As Input: 0b: Input Data Register (offset 640h[9]) 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[25] Output Data register (offset 648h[9]) 1b: Reserved | No/Yes | 0 |
| 19 | GPIO[25] Direction Control | RW | 0b: Input 1b: Output | No/Yes | 0 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|--------------------------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 20 | GPIO[26] Source/Destination | RW | As Input: 0b: Input Data Register (offset 640h[10]) 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[26] Output Data register (offset 648h[10]) 1b: Reserved | No/Yes | 0 |
| 21 | GPIO[26] Direction Control | RW | 0b: Input 1b: Output | No/Yes | 0 |
| 22 | GPIO[27] Source/Destination | RW | As Input: 0b: Input Data Register (offset 640h[11]) 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[27] Output Data register (offset 648h[11]) 1b: Reserved | No/Yes | 0 |
| 23 | GPIO[27] Direction Control | RW | 0b: Input 1b: Output | No/Yes | 0 |
| 24 | GPIO[28] Source/Destination | RW | As Input: 0b: Input Data Register (offset 640h[12]) 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[28] Output Data register (offset 648h[12]) 1b: Reserved | No/Yes | 0 |
| 25 | GPIO[28] Direction Control | RW | 0b: Input 1b: Output | No/Yes | 0 |
| 26 | GPIO[29] Source/Destination | RW | As Input: 0b: Input Data Register (offset 640h[13]) 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[29] Output Data register (offset 648h[13]) 1b: Reserved | No/Yes | 0 |
| 27 | GPIO[29] Direction Control | RW | 0b: Input 1b: Output | No/Yes | 0 |
| 28 | GPIO[30] Source/Destination | RW | As Input: 0b: Input Data Register (offset 640h[14]) 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[30] Output Data register (offset 648h[14]) 1b: Reserved | No/Yes | 0 |
| 29 | GPIO[30] Direction Control | RW | 0b: Input 1b: Output | No/Yes | 0 |
| 30 | GPIO[31] Source/Destination | RW | As Input: 0b: Input Data Register (offset 640h[15]) 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[31] Output Data register (offset 648h[15]) 1b: Reserved | No/Yes | 0 |
| 31 | GPIO[31] Direction Control | RW | 0b: Input 1b: Output | No/Yes | 0 |

8.2.103 GPIO INPUT DE-BOUNCE REGISTER – OFFSET 638h (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-----------------------------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|------------|
| 31:0 | GPIOx Input De- Bounce Control | RW | Controls de-bounce when the corresponding GPIOx signal is configured as an input. Bit[31:0] correspond to GPIO[31:0] respectively. 0b: GPIOx input is not de-bounced 1b: GPIOx input is de-bounced | No/Yes | 0000_0000h |

8.2.104 GPIO 0-15 INPUT DATA REGISTER – OFFSET 63Ch (Global)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|---------------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | GPIO[0] Input Data | RO | GPIO[0] Input Data Return 0 if GPIO[0] is configured as an output (offset 62Ch[1]=1) Return the state of GPIO[0] pin if GPIO[0] is configured as an input (offset 62Ch[1]=0) | No/Yes | 1 |
| 1 | GPIO[1] Input Data | RO | GPIO[1] Input Data Return 0 if GPIO[1] is configured as an output (offset 62Ch[3]=1) Return the state of GPIO[1] pin if GPIO[1] is configured as an input (offset 62Ch[3]=0) | No/Yes | 1 |
| 2 | GPIO[2] Input Data | RO | GPIO[2] Input Data Return 0 if GPIO[2] is configured as an output (offset 62Ch[5]=1) Return the state of GPIO[2] pin if GPIO[2] is configured as an input (offset 62Ch[5]=0) | No/Yes | 0 |
| 3 | GPIO[3] Input Data | RO | GPIO[3] Input Data Return 0 if GPIO[3] is configured as an output (offset 62Ch[7]=1) Return the state of GPIO[3] pin if GPIO[3] is configured as an input (offset 62Ch[7]=0) | No/Yes | 1 |
| 4 | GPIO[4] Input Data | RO | GPIO[4] Input Data Return 0 if GPIO[4] is configured as an output (offset 62Ch[9]=1) Return the state of GPIO[4] pin if GPIO[4] is configured as an input (offset 62Ch[9]=0) | No/Yes | 0 |
| 5 | GPIO[5] Input Data | RO | GPIO[5] Input Data Return 0 if GPIO[5] is configured as an output (offset 62Ch[11]=1) Return the state of GPIO[5] pin if GPIO[5] is configured as an input (offset 62Ch[11]=0) | No/Yes | 1 |
| 6 | GPIO[6] Input Data | RO | GPIO[6] Input Data Return 0 if GPIO[6] is configured as an output (offset 62Ch[13]=1) Return the state of GPIO[6] pin if GPIO[6] is configured as an input (offset 62Ch[13]=0) | No/Yes | 0 |
| 7 | GPIO[7] Input Data | RO | GPIO[7] Input Data Return 0 if GPIO[7] is configured as an output (offset 62Ch[15]=1) Return the state of GPIO[7] pin if GPIO[7] is configured as an input (offset 62Ch[15]=0) | No/Yes | 1 |
| 8 | GPIO[8] Input Data | RO | GPIO[8] Input Data Return 0 if GPIO[8] is configured as an output (offset 62Ch[17]=1) Return the state of GPIO[8] pin if GPIO[8] is configured as an input (offset 62Ch[17]=0) | No/Yes | 0 |
| 9 | GPIO[9] Input Data | RO | GPIO[9] Input Data Return 0 if GPIO[9] is configured as an output (offset 62Ch[19]=1) Return the state of GPIO[9] pin if GPIO[9] is configured as an input (offset 62Ch[19]=0) | No/Yes | 1 |
| 10 | GPIO[10] Input Data | RO | GPIO[10] Input Data Return 0 if GPIO[10] is configured as an output (offset 62Ch[21]=1) Return the state of GPIO[10] pin if GPIO[10] is configured as an input (offset 62Ch[21]=0) | No/Yes | 0 |
| 11 | GPIO[11] Input Data | RO | GPIO[11] Input Data Return 0 if GPIO[11] is configured as an output (offset 62Ch[23]=1) Return the state of GPIO[11] pin if GPIO[11] is configured as an input (offset 62Ch[23]=0) | No/Yes | 1 |
| 12 | GPIO[12] Input Data | RO | GPIO[12] Input Data Return 0 if GPIO[12] is configured as an output (offset 62Ch[25]=1) Return the state of GPIO[12] pin if GPIO[12] is configured as an input (offset 62Ch[25]=0) | No/Yes | 0 |
| 13 | GPIO[13] Input Data | RO | GPIO[13] Input Data Return 0 if GPIO[13] is configured as an output (offset 62Ch[27]=1) Return the state of GPIO[13] pin if GPIO[13] is configured as an input (offset 62Ch[27]=0) | No/Yes | 1 |
| 14 | GPIO[14] Input Data | RO | GPIO[14] Input Data Return 0 if GPIO[14] is configured as an output (offset 62Ch[29]=1) Return the state of GPIO[14] pin if GPIO[14] is configured as an input (offset 62Ch[29]=0) | No/Yes | 0 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 15 | GPIO[15] Input Data | RO | GPIO[15] Input Data Return 0 if GPIO[15] is configured as an output (offset 62Ch[31]=1) Return the state of GPIO[15] pin if GPIO[15] is configured as an input (offset 62Ch[31]=0) | No/Yes | 1 |
| 31:16 | Reserved | RsvdP | Not Support. | No | 0000h |

8.2.105 GPIO 16-31 INPUT DATA REGISTER – OFFSET 640h (Global)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|---------------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | GPIO[16] Input Data | RO | GPIO[16] Input Data Return 0 if GPIO[16] is configured as an output (offset 630h[1]=1) Return the state of GPIO[16] pin if GPIO[16] is configured as an input (offset 630h[1]=0) | No/Yes | 0 |
| 1 | GPIO[17] Input Data | RO | GPIO[17] Input Data Return 0 if GPIO[17] is configured as an output (offset 630h[3]=1) Return the state of GPIO[17] pin if GPIO[17] is configured as an input (offset 630h[3]=0) | No/Yes | 1 |
| 2 | GPIO[18] Input Data | RO | GPIO[18] Input Data Return 0 if GPIO[18] is configured as an output (offset 630h[5]=1) Return the state of GPIO[18] pin if GPIO[18] is configured as an input (offset 630h[5]=0) | No/Yes | 0 |
| 3 | GPIO[19] Input Data | RO | GPIO[19] Input Data Return 0 if GPIO[19] is configured as an output (offset 630h[7]=1) Return the state of GPIO[19] pin if GPIO[19] is configured as an input (offset 630h[7]=0) | No/Yes | 1 |
| 4 | GPIO[20] Input Data | RO | GPIO[20] Input Data Return 0 if GPIO[20] is configured as an output (offset 630h[9]=1) Return the state of GPIO[20] pin if GPIO[20] is configured as an input (offset 630h[9]=0) | No/Yes | 0 |
| 5 | GPIO[21] Input Data | RO | GPIO[21] Input Data Return 0 if GPIO[21] is configured as an output (offset 630h[11]=1) Return the state of GPIO[21] pin if GPIO[21] is configured as an input (offset 630h[11]=0) | No/Yes | 1 |
| 6 | GPIO[22] Input Data | RO | GPIO[22] Input Data Return 0 if GPIO[22] is configured as an output (offset 630h[13]=1) Return the state of GPIO[22] pin if GPIO[22] is configured as an input (offset 630h[13]=0) | No/Yes | 0 |
| 7 | GPIO[23] Input Data | RO | GPIO[23] Input Data Return 0 if GPIO[23] is configured as an output (offset 630h[15]=1) Return the state of GPIO[23] pin if GPIO[23] is configured as an input (offset 630h[15]=0) | No/Yes | 1 |
| 8 | GPIO[24] Input Data | RO | GPIO[24] Input Data Return 0 if GPIO[24] is configured as an output (offset 630h[17]=1) Return the state of GPIO[24] pin if GPIO[24] is configured as an input (offset 630h[17]=0) | No/Yes | 0 |
| 9 | GPIO[25] Input Data | RO | GPIO[25] Input Data Return 0 if GPIO[25] is configured as an output (offset 630h[19]=1) Return the state of GPIO[25] pin if GPIO[25] is configured as an input (offset 630h[19]=0) | No/Yes | 1 |
| 10 | GPIO[26] Input Data | RO | GPIO[26] Input Data Return 0 if GPIO[26] is configured as an output (offset 630h[21]=1) Return the state of GPIO[26] pin if GPIO[26] is configured as an input (offset 630h[21]=0) | No/Yes | 0 |
| 11 | GPIO[27] Input Data | RO | GPIO[27] Input Data Return 0 if GPIO[27] is configured as an output (offset 630h[23]=1) Return the state of GPIO[27] pin if GPIO[27] is configured as an input (offset 630h[23]=0) | No/Yes | 1 |
| 12 | GPIO[28] Input Data | RO | GPIO[28] Input Data Return 0 if GPIO[28] is configured as an output (offset 630h[25]=1) Return the state of GPIO[28] pin if GPIO[28] is configured as an input (offset 630h[25]=0) | No/Yes | 0 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 13 | GPIO[29] Input Data | RO | GPIO[29] Input Data Return 0 if GPIO[29] is configured as an output (offset 630h[27]=1) Return the state of GPIO[29] pin if GPIO[29] is configured as an input (offset 630h[27]=0) | No/Yes | 1 |
| 14 | GPIO[30] Input Data | RO | GPIO[30] Input Data Return 0 if GPIO[30] is configured as an output (offset 630h[29]=1) Return the state of GPIO[30] pin if GPIO[30] is configured as an input (offset 630h[29]=0) | No/Yes | 0 |
| 15 | GPIO[31] Input Data | RO | GPIO[31] Input Data Return 0 if GPIO[31] is configured as an output (offset 630h[31]=1) Return the state of GPIO[31] pin if GPIO[31] is configured as an input (offset 630h[31]=0) | No/Yes | 1 |
| 31:16 | Reserved | RsvdP | Not Support. | No/Yes | 0000h |

8.2.106 GPIO 0-15 OUTPUT DATA REGISTER – OFFSET 644h (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|----------------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | GPIO[0] Output Data | RW | GPIO[0] Output Data The value written to this bit is driven to GPIO[0] output if GPIO[0] is configured as an output (offset 62Ch[1]=1) | No/Yes | 0 |
| 1 | GPIO[1] Output Data | RW | GPIO[1] Output Data The value written to this bit is driven to GPIO[1] output if GPIO[1] is configured as an output (offset 62Ch[3]=1) | No/Yes | 0 |
| 2 | GPIO[2] Output Data | RW | GPIO[2] Output Data The value written to this bit is driven to GPIO[2] output if GPIO[2] is configured as an output (offset 62Ch[5]=1) | No/Yes | 0 |
| 3 | GPIO[3] Output Data | RW | GPIO[3] Output Data The value written to this bit is driven to GPIO[3] output if GPIO[3] is configured as an output (offset 62Ch[7]=1) | No/Yes | 0 |
| 4 | GPIO[4] Output Data | RW | GPIO[4] Output Data The value written to this bit is driven to GPIO[4] output if GPIO[4] is configured as an output (offset 62Ch[9]=1) | No/Yes | 0 |
| 5 | GPIO[5] Output Data | RW | GPIO[5] Output Data The value written to this bit is driven to GPIO[5] output if GPIO[5] is configured as an output (offset 62Ch[11]=1) | No/Yes | 0 |
| 6 | GPIO[6] Output Data | RW | GPIO[6] Output Data The value written to this bit is driven to GPIO[6] output if GPIO[6] is configured as an output (offset 62Ch[13]=1) | No/Yes | 0 |
| 7 | GPIO[7] Output Data | RW | GPIO[7] Output Data The value written to this bit is driven to GPIO[7] output if GPIO[7] is configured as an output (offset 62Ch[15]=1) | No/Yes | 0 |
| 8 | GPIO[8] Output Data | RW | GPIO[8] Output Data The value written to this bit is driven to GPIO[8] output if GPIO[8] is configured as an output (offset 62Ch[17]=1) | No/Yes | 0 |
| 9 | GPIO[9] Output Data | RW | GPIO[9] Output Data The value written to this bit is driven to GPIO[9] output if GPIO[9] is configured as an output (offset 62Ch[19]=1) | No/Yes | 0 |
| 10 | GPIO[10] Output Data | RW | GPIO[10] Output Data The value written to this bit is driven to GPIO[10] output if GPIO[10] is configured as an output (offset 62C[21]=1) | No/Yes | 0 |
| 11 | GPIO[11] Output Data | RW | GPIO[11] Output Data The value written to this bit is driven to GPIO[11] output if GPIO[11] is configured as an output (offset 62Ch[23]=1) | No/Yes | 0 |
| 12 | GPIO[12] Output Data | RW | GPIO[12] Output Data The value written to this bit is driven to GPIO[12] output if GPIO[12] is configured as an output (offset 62Ch[25]=1) | No/Yes | 0 |
| 13 | GPIO[13] Output Data | RW | GPIO[13] Output Data The value written to this bit is driven to GPIO[13] output if GPIO[13] is configured as an output (offset 62Ch[27]=1) | No/Yes | 0 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 14 | GPIO[14] Output Data | RW | GPIO[14] Output Data The value written to this bit is driven to GPIO[14] output if GPIO[14] is configured as an output (offset 62Ch[29]=1) | No/Yes | 0 |
| 15 | GPIO[15] Output Data | RW | GPIO[15] Output Data The value written to this bit is driven to GPIO[15] output if GPIO[15] is configured as an output (offset 62Ch[31]=1) | No/Yes | 0 |
| 31:16 | Reserved | RsvdP | Not Support. | No | 0000h |

8.2.107 GPIO 16-31 OUTPUT DATA REGISTER – OFFSET 648h (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | GPIO[16] Output Data | RW | GPIO[16] Output Data The value written to this bit is driven to GPIO[16] output if GPIO[16] is configured as an output (offset 630h[1]=1) | No/Yes | 0 |
| 1 | GPIO[17] Output Data | RW | GPIO[17] Output Data The value written to this bit is driven to GPIO[17] output if GPIO[17] is configured as an output (offset 630h[3]=1) | No/Yes | 0 |
| 2 | GPIO[18] Output Data | RW | GPIO[18] Output Data The value written to this bit is driven to GPIO[18] output if GPIO[18] is configured as an output (offset 630h[5]=1) | No/Yes | 0 |
| 3 | GPIO[19] Output Data | RW | GPIO[19] Output Data The value written to this bit is driven to GPIO[19] output if GPIO[19] is configured as an output (offset 630h[7]=1) | No/Yes | 0 |
| 4 | GPIO[20] Output Data | RW | GPIO[20] Output Data The value written to this bit is driven to GPIO[20] output if GPIO[20] is configured as an output (offset 630h[9]=1) | No/Yes | 0 |
| 5 | GPIO[21] Output Data | RW | GPIO[21] Output Data The value written to this bit is driven to GPIO[21] output if GPIO[21] is configured as an output (offset 630h[11]=1) | No/Yes | 0 |
| 6 | GPIO[22] Output Data | RW | GPIO[22] Output Data The value written to this bit is driven to GPIO[22] output if GPIO[22] is configured as an output (offset 630h[13]=1) | No/Yes | 0 |
| 7 | GPIO[23] Output Data | RW | GPIO[23] Output Data The value written to this bit is driven to GPIO[23] output if GPIO[23] is configured as an output (offset 630h[15]=1) | No/Yes | 0 |
| 8 | GPIO[24] Output Data | RW | GPIO[24] Output Data The value written to this bit is driven to GPIO[24] output if GPIO[24] is configured as an output (offset 630h[17]=1) | No/Yes | 0 |
| 9 | GPIO[25] Output Data | RW | GPIO[25] Output Data The value written to this bit is driven to GPIO[25] output if GPIO[25] is configured as an output (offset 630h[19]=1) | No/Yes | 0 |
| 10 | GPIO[26] Output Data | RW | GPIO[26] Output Data The value written to this bit is driven to GPIO[26] output if GPIO[26] is configured as an output (offset 630h[21]=1) | No/Yes | 0 |
| 11 | GPIO[27] Output Data | RW | GPIO[27] Output Data The value written to this bit is driven to GPIO[27] output if GPIO[27] is configured as an output (offset 630h[23]=1) | No/Yes | 0 |
| 12 | GPIO[28] Output Data | RW | GPIO[28] Output Data The value written to this bit is driven to GPIO[28] output if GPIO[28] is configured as an output (offset 630h[25]=1) | No/Yes | 0 |
| 13 | GPIO[29] Output Data | RW | GPIO[29] Output Data The value written to this bit is driven to GPIO[29] output if GPIO[29] is configured as an output (offset 630h[27]=1) | No/Yes | 0 |
| 14 | GPIO[30] Output Data | RW | GPIO[30] Output Data The value written to this bit is driven to GPIO[30] output if GPIO[30] is configured as an output (offset 630h[29]=1) | No/Yes | 0 |
| 15 | GPIO[31] Output Data | RW | GPIO[31] Output Data The value written to this bit is driven to GPIO[31] output if GPIO[31] is configured as an output (offset 630h[31]=1) | No/Yes | 0 |
| 31:16 | Reserved | RsvdP | Not Support. | No | 0000h |

8.2.108 GPIO 0-31 INTERRUPT POLARITY REGISTER – OFFSET 64Ch (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-------------------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|------------|
| 31:0 | GPIO Interrupt Polarity | RW | Controls whether GPIO Interrupt input is Active-Low or Active-High for the corresponding GPIOx signal. Bit[31:0] correspond to GPIO[31:0] respectively. 0b: GPIO Interrupt input is Active-Low 1b: GPIO Interrupt input is Active-High | No/Yes | 0000_0000h |

8.2.109 GPIO 0-31 INTERRUPT STATUS REGISTER – OFFSET 650h (Global)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-----------------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|------------|
| 31:0 | GPIO Interrupt Status | RO | Indicates whether GPIO interrupt are inactive or active for the corresponding GPIOx signal. Bit[31:0] correspond to GPIO[31:0] respectively. 0b: GPIO interrupt is inactive 1b: GPIO interrupt is active | No | 5555_5554h |

8.2.110 GPIO 0-31 INTERRUPT MASK REGISTER – OFFSET 654h (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|---------------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|------------|
| 31:0 | GPIO Interrupt Mask | RW | Indicates whether GPIO interrupts are masked or not masked for the corresponding GPIOx signal. Bit[31:0] correspond to GPIO[31:0] respectively. 0b: GPIO interrupt is unmasked 1b: GPIO interrupt is masked | No/Yes | 0000_0000h |

8.2.111 XPIP_CSR 0 REGISTER – OFFSET 844h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-----------|------|------------------------------------------------|----------------------|------------|
| 31:0 | XPIP_CSR0 | RW | XPIP_CSR 0 value. Bit[2]: Cross_Link_En | Yes | 0400_1060h |

8.2.112 XPIP_CSR 1 REGISTER – OFFSET 848h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-----------|------|-------------------|----------------------|------------|
| 31:0 | XPIP_CSR1 | RW | XPIP_CSR 1 value. | Yes | 0400_0800h |

8.2.113 DECODE VGA REGISTER – OFFSET 84Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-------------------|-------|-------------------------------------------------|----------------------|---------|
| 30:0 | Reserved | RsvdP | Not Support. | No | 0-0h |
| 31 | Decode VGA Enable | RO | 0b: Disable VGA decode 1b: Enable VGA decode | Yes | 1 |

8.2.114 SWITCH OPERATION MODE REGISTER – OFFSET 850h (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|----------------------------------------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|----------|
| 0 | Store-Forward | RW | When set, a store-forward mode is used. Otherwise, the chip is working under cut-through mode. | Yes | 0 |
| 2:1 | Cut-through Threshold | RW | Cut-through Threshold. When forwarding a packet from low-speed port to high-speed mode, the chip provides the capability to adjust the forwarding threshold. 00b: the threshold is set at the middle of forwarding packet 01b: the threshold is set ahead 1-cycle of middle point 10b: the threshold is set ahead 2-cycle of middle point. 11b: the threshold is set ahead 3-cycle of middle point. | Yes | 01b |
| 3 | Port Arbitration Mode | RW | When set, the round-robin arbitration will stay in the arbitrated port even if the credit is not enough but request is pending. When clear, the round-robin arbitration will always go to the requesting port, which the outgoing credit is enough for the packet queued in the port. | Yes | 0 |
| 4 | Credit Update Mode | RW | When set, the frequency of releasing new credit to the link partner will be one credit per update. When clear, the frequency of releasing new credit to the link partner will be two credits per update. | Yes | 0 |
| 5 | Ordering on Different Egress Port Mode | RW | When set, there has ordering rule on packets for different egress port. | Yes | 0 |
| 6 | Ordering on Different Tag of Completion Mode | RW | When set, there has ordering rule between completion packet with different tag. | Yes | 1 |
| 7 | NonPost TLP Store-Forward | RW | When set, for Non-port TLP store-forward mode is used. Otherwise, Non-post TLP is working under cut-through mode. When write '1', this bit is changed to '0'. When write '0', this bit is changed to '1'. | Yes | 1 |
| 31:8 | Reserved | RsvdP | Not Support. | No | 0000_00h |

8.2.115 XPIP_CSR 2 REGISTER – OFFSET 854h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------------|-------|-----------------------|----------------------|---------|
| 7:0 | FTS Number | RW | Indicates FTS number. | Yes | 80h |
| 9:8 | Scrambler Control | RW | Reset to 00b. | Yes | 00b |
| 10 | L0s | RW | Reset to 0b. | Yes | 0 |
| 11 | Compliance to Detect | RW | Reset to 0b. | Yes | 0 |
| 13:12 | Change Speed Sel | RW | Reset to 00b. | Yes | 00b |
| 14 | Change Speed En | RW | Reset to 0b. | Yes | 0 |
| 15 | Reserved | RsvdP | Not Support. | No | 0 |

8.2.116 PHY PARAMETER 1 REGISTER – OFFSET 854h (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------------------------------------|------|--------------------------------------------------------------------------------------------------------|----------------------|---------|
| 20:16 | C_EMP_POST_GE N1_3P5_NOM (Global) | RW | Set the de-emphasis level for GEN1, -3.5db. Please refer to Section 6.1.7 for more detail information. | Yes | 1_0101b |
| 25:21 | C_EMP_POST_GE N2_3P5_NOM (Global) | RW | Set the de-emphasis level for GEN2, -3.5db. Please refer to Section 6.1.7 for more detail information. | Yes | 10_101b |
| 30:26 | C_EMP_POST_GE N2_6P0_NOM (Global) | RW | Set the de-emphasis level for GEN2, -6.0db. Please refer to Section 6.1.7 for more detail information. | Yes | 111_01b |
| 31 | Reserved | RO | Not Support. | No | 0 |

8.2.117 PHY PARAMETER 2 REGISTER – OFFSET 858h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------------------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 3:0 | C_TX_PHY_ LATENCY (Global) | RW | Set the transmitter electrical idle latency. Please refer to Section 6.1.8 for more detail information. It is set by Upstream Port Only. | Yes | 7h |
| 6:4 | C_REC_DETEC_ USEC (Global) | RW | Set the receiver detection threshold. Please refer to Section 6.1.1 for more detail information. It is set by Upstream Port Only. | Yes | 010b |
| 7 | Reserved | RsvdP | Not Support. | No | 0 |
| 8 | P_CDR_FREQLOO P_EN | RW | Reset to 0b. | Yes | 1 |
| 10:9 | P_CDR_ THRESHOLD | RW | Reset to 01b. | Yes | 10b |
| 12:11 | P_CDR_FREQLOO P_GAIN | RW | Reset to 01b. | Yes | 11b |
| 15:13 | Reserved | RsvdP | Not Support. | No | 000b |
| 16 | P_DRV_LVL_MGN DELATA_EN | RW | Reset to 0b. | Yes | 0 |
| 17 | P_DRV_LVL_NOM DELATA_EN | RW | Reset to 0b. | Yes | 0 |
| 18 | P_EMP_POST_MG N_DELATA_EN | RW | Reset to 0b. | Yes | 0 |
| 19 | P_EMP_POST_NO M_DELATA_EN | RW | Reset to 0b. | Yes | 0 |
| 21:20 | P_RX_SIGDET_ LVL | RW | Set the receiver signal detection threshold. Please refer to Section 6.1.2 for more detail information. | Yes | 01b |
| 25:22 | P_RX_EQ_1 | RW | Set the receiver equalization for GEN1 link. Please refer to Section 6.1.3 for more detail information. | Yes | 0h |
| 29:26 | P_RX_EQ_2 | RW | Set the receiver equalization for GEN2 link. Please refer to Section 6.1.3 for more detail information. | Yes | 0h |
| 30 | P_TXSWING | RW | Set the transmitter swing. Please refer to Section 6.1.4 for more detail information. 0b: full voltage swing with de-emphasis 1b: half voltage swing without de-emphasis | Yes | 0 |
| 31 | Reserved | RsvdP | Not Support. | No | 0 |

8.2.118 PHY PARAMETER 3 REGISTER – OFFSET 85Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-------------------------------|-------|------------------|----------------------|---------|
| 6:0 | PHY Parameter 3 (Per Port) | RW | PHY's Lane mode. | Yes | 00h |
| 14:7 | Reserved | RsvdP | Not Support. | No | 00h |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------|------|-------------------------------------------------------------|----------------------|---------|
| 31:15 | PHY Parameter 3 (Global) | RW | PHY's delta value setting. It is set by Upstream Port Only. | Yes | 0001h |

8.2.119 PHY PARAMETER 4 REGISTER - OFFSET 860h (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------------------------|-------|--------------------------|----------------------|---------|
| 14:0 | PHY TX Margin Parameter (Global) | RW | PHY Tx margin parameter. | Yes | 116Bh |
| 31:15 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.2.120 XPIP_CSR 3 REGISTER – OFFSET 864h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-----------|------|------------------|----------------------|------------|
| 31:0 | XPIP_CSR3 | RW | XPIP_CSR3 value. | Yes | 000F_0000h |

8.2.121 XPIP_CSR 4 REGISTER – OFFSET 868h (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|--------------------|------|-------------------|----------------------|------------|
| 31:0 | XPIP_CSR4 (Global) | RW | XPIP_CSR 4 value. | Yes | 0000_0000h |

8.2.122 XPIP_CSR 5 REGISTER – OFFSET 86Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-----------------------|------|----------------------------------------------------------------------------------------------------------------------------|----------------------|------------------------|
| 29:0 | XPIP_CSR5[29:0] | RW | Bit[10]: Default ACK Latency Timer Enable 0b: disable default ack latency timer 1b: enable default ack latency timer | Yes | 3308_0008h |
| 30 | DO_CHG_DATA_RATE_CTRL | RW | DO_CHG_DATA_RATE_CTRL. | Yes | 1 for Up 0 for Down |
| 31 | Gen1_Cap_Only | RW | 0b: report GEN2 capability 1b: report GEN1 capability | Yes | 0 |

8.2.123 NON TRANSFER MODE REGISTER – OFFSET 870h (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|--------------------------------------|------|-----------------|----------------------|---------|
| 0 | TX_SOF_FORM | RO | Test used only. | Yes | 0 |
| 1 | PM Data Select Register R/W Enable | RO | Test used only. | Yes | 0 |
| 2 | ARB_Abort_Sel | RO | Test used only. | Yes | 1 |
| 3 | 4K Boundary Check Enable | RO | Test used only. | Yes | 0 |
| 4 | FIFOERR_FIX_SEL | RO | Test used only. | No | 1 |
| 5 | ORDER_RULE5 Enable | RW | Test used only. | Yes | 0 |
| 6 | Ordering Frozen Disable for Post Pkt | RW | Test used only. | Yes | 0 |
| 7 | Ordering Frozen Disable for NP Pkt | RW | Test used only. | Yes | 0 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------|-------------|---------------------------------------------------------|----------------------|---------|
| 11:8 | Reserved | RsvdP | Not Support. | No | 0h |
| 12 | ARB_VCFLG_SEL | RO | Test used only. | Yes | 1 |
| 13 | DMA Capability | RO | 0b: disable DMA capability 1b: enable DMA capability | No/Yes | 1 |
| 14 | Non-Trans_Mode | HwInt RO | Indicates the status of strapping pin NT_EN_L. | Yes | 0 |
| 15 | GNT_FAIL2IDLE | RO | Test used only. | Yes | 1 |
| 31:16 | Reserved | RsvdP | Not Support. | No | 0000h |

8.2.124 OPERATION MODE REGISTER – OFFSET 874h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | Operation Mode | HwInt RO | Bit[0]: Memory Bist Bit[1]: IDDRB Bit[2]: FAST_MODE Bit[3]: DEBUG_MODE Bit[4]: PHY_MODE Bit[8:5]: WORK_MODE Bit[9]: PLCSEL Bit[10]: SCAN_MODE Bit[15:11]: Reserved | No | 0202h for 324 mode 0222h for 424 mode 0242h for 524 mode 0262h for 624 mode 0282h for 1124 mode 02A2h for 1224 mode |
| 23:16 | Reserved | RsvdP | Not Support. | No | 00h |
| 27:24 | L1PM Option | RW | Set L1PM option. | Yes | 0h |
| 31:28 | Reserved | RsvdP | Not Support. | No | 0h |

8.2.125 DEVICE SPECIFIC POWER MANAGEMENT EVENT– OFFSET 878h (Downstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | Device Specific PME Capability | RO | 0b: disable device specific PME. 1b: enable device specific PME. | Yes | 0 |
| 1 | PME Turnoff Message Request | RW | Request to send PME turnoff message. | No/Yes | 0 |
| 2 | Port Power | RW | Control GPIO[4:0] pins when Device Specific PME Capability is enabled. Downstream port 1 controls GPIO[0], Downstream port 2 controls GPIO[1], ... and so on. It is valid when Device Specific PME Capability is enabled. | No/Yes | 1 |
| 3 | Port Reset | RW | This bit when reset asserts an active low reset signal to the attached device. When set, the reset signal is de-asserted. It is valid when Device Specific PME Capability is enabled. | No/Yes | 1 |
| 15:4 | Reserved | RsvdP | Not Support. | No | 000h |
| 17:16 | Link Status | RO | These two bits represent the link status of device connected to the downstream port. 00b: L0 01b: L0s 10b: L1 11b: L2/L3 | No | 00b |
| 31:18 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.2.126 EEPROM CONTROL REGISTER – OFFSET 87Ch (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | EEPROM Start | RW | Starts the EEPROM read or write cycle. 1b: start read or write cycle | No/Yes | 0 |
| 3:1 | Reserved | RsvdP | Not Support. | No | 000b |
| 4 | EEPROM Autoload Status | RO | 0b: EEPROM autoload was unsuccessfully or is disabled 1b: EEPROM autoload occurred successfully after PERST_L. | No | 0 |
| 5 | EEPROM is Autoload Disabled | RW | 0b: EEPROM autoload is enabled 1b: EEPROM autoload is disabled | No/Yes | 0 |
| 7:6 | EEPROM Clock Rate | RW | Determines the frequency of the EEPROM clock which is derived from the primary clock. 01b: PEXCLK/4 (PEXCLK is 250 MHz) Others: Reserved | No/Yes | 01b |
| 15:8 | EEPROM Status | RO | Indicate the eeprom status. | No | 00h |
| 23:16 | EEPROM Command | RW | 01h: write STATUS register 02h: EEPROM write 03h: EEPROM read 04h: disable write operation 05h: read STATUS register 06h: enable write operation C7h: erase entire EEPROM | No/Yes | 00h |
| 30:24 | Reserved | RsvdP | Not Support. | No | 00h |
| 31 | Size 64K Mode | RW | 0b: EEPROM size is less or equal to 64K 1b: EEPROM size is larger 64K | No/Yes | 0 |

8.2.127 EEPROM ADDRESS AND DATA REGISTER – OFFSET 880h (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------|------|------------------------------|----------------------|---------|
| 15:0 | EEPROM Address | RW | Contains the EEPROM address. | No/Yes | 0000h |
| 31:16 | EEPROM Data | RW | Contains the EEPROM data. | No/Yes | 0000h |

8.2.128 DEBUGOUT CONTROL REGISTER – OFFSET 884h (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------------|-------|------------------------------------|----------------------|---------|
| 4:0 | Debug Mode Select | RW | Debug mode select. | No/Yes | 0 0000b |
| 7:5 | Debug Port Select S1 | RW | Debug port select s1. | No/Yes | 000b |
| 8 | DebugPort_ Select S2 | RW | Debugport select s2. | No/Yes | 0 |
| 9 | Debug Output Start | RW | Start to select debug output data. | No/Yes | 0 |
| 31:10 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.2.129 DEBUGOUT DATA REGISTER – OFFSET 888h (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-------------------|------|---------------------------------|----------------------|------------|
| 31:0 | Debug Output Data | RO | Contains the debug output data. | No | 0000 0000h |

8.2.130 LTSSM_CSR REGISTER – OFFSET 88Ch (Downstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-----------|-------|--------------------------------------------------------------------------------------------------------|----------------------|----------|
| 7:0 | LTSSM_CSR | RW | Bit[2]: Pseudo MRL_PDC_En 0b: disable pseudo MRL_PDC function 1b: enable pseudo MRL_PDC function | Yes | 00h |
| 31:8 | Reserved | RsvdP | Not Support. | No | 0000 00h |

8.2.131 MAC_CSR REGISTER – OFFSET 890h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------|-------|----------------|----------------------|---------|
| 15:0 | Reserved | RsvdP | Not Support. | No | 0000h |
| 31:16 | MAC_CSR | RW | MAC_CSR value. | Yes | 0004h |

8.2.132 POWER SAVING DISABLE REGISTER – OFFSET 8A4h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|----------------------|-------|------------------------------------------------------------------------------|----------------------|---------|
| 0 | Power Saving Disable | RW | Disable power saving. 0b: enable power saving 1b: disable power saving | Yes | 0 |
| 31:1 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.2.133 TRANSACTION LAYER CSR REGISTER – OFFSET 8A8h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-------------------------|-------|-----------------|----------------------|---------|
| 0 | Egress_Reqcredit_Starve | RW | Test used only. | Yes | 1 |
| 1 | MF_Credit_Update_Dis | RW | Test used only. | Yes | 0 |
| 2 | MC_Cap_Dis | RW | Test used only. | Yes | 0 |
| 3 | MEM_Sharing_Dis | RO | Test used only. | Yes | 0 |
| 31:4 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.2.134 REPLAY TIME-OUT COUNTER REGISTER – OFFSET 8ACh

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 11:0 | User Replay Timer | RW | A 12-bit register contains a user-defined value. | Yes | 000h |
| 12 | Enable User Replay Timer | RW | When asserted, the user-defined replay time-out value is be employed. 0b: use the default replay time-out value 1b: use the user-defined replay time-out value on bit[11:0] | Yes | 0 |
| 15:13 | Reserved | RsvdP | Not Support. | No | 000b |

8.2.135 ACKNOWLEDGE LATENCY TIMER REGISTER – OFFSET 8ACh

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-------------------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 29:16 | User ACK Latency Timer | RW | A 14-bit register contains a user-defined value. | Yes | 0-0h |
| 30 | Enable User ACK Latency | RW | When asserted, the user-defined ACK latency value is be employed. 0b: use the default ack latency value 1b: use the user-defined ack latency value on bit[29:16] | Yes | 0 |
| 31 | Reserved | RsvdP | Not Support. | No | 0 |

8.2.136 PORT MISC 0 REGISTER – OFFSET 8B0h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-------------------------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------|----------------------|----------|
| 7:0 | Reserved | RsvdP | Not Support. | No | 00h |
| 13:8 | Power Management Control Parameter | RW | Power Management Control parameter. | Yes | 00_0001b |
| 14 | RX Polarity Inversion Disable | RW | 0b: enable rx polarity inversion circuit 1b: disable rx polarity inversion circuit | Yes | 0 |
| 15 | Compliance Pattern Parity Control Disable | RW | 0b: enable compliance pattern parity control 1b: disable compliance pattern parity control It is set by Upstream Port Only. | Yes | 0 |

8.2.137 PHY PARAMETER 0 REGISTER – OFFSET 8B0h (Upstream Port Only)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------------------------|-------|---------------------------------------------------------------------------------------|----------------------|---------|
| 20:16 | C_DRV_LVL_3P5_NOM (Global) | RW | Set drive amplitude level. Please refer to Section 6.1.6 for more detail information. | Yes | 1_0011b |
| 25:21 | C_DRV_LVL_6P0_NOM (Global) | RW | Set drive amplitude level. Please refer to Section 6.1.6 for more detail information. | Yes | 10_011b |
| 30:26 | C_DRV_LVL_HALF_NOM (Global) | RW | Set drive amplitude level. Please refer to Section 6.1.6 for more detail information. | Yes | 000_10b |
| 31 | Reserved | RsvdP | Not Support. | No | 0 |

8.2.138 PORT MISC 1 REGISTER – OFFSET 8B4h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------------|-------|-----------------------------------------------------------|----------------------|------------------------|
| 7:0 | Reserved | RsvdP | Not Support. | No | 00h |
| 9:8 | DO_CHG_DATA_CNT_SEL | RW | The trying number for doing change data rate. | Yes | 00b |
| 10 | Port Disable | RW | Disable this port. 0b: enable port 1b: disable port | Yes | 0 |
| 11 | Reset Select | RW | Reset select. It is valid for upstream port only. | Yes | 1 for up 0 for down |
| 15:12 | Reserved | RsvdP | Not Support. | No | 000b |

8.2.139 XPIP_CSR 6 REGISTER – OFFSET 8B4h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------|------|-------------------|----------------------|---------|
| 23:16 | XPIP_CSR6 | RW | XPIP_CSR 6 value. | Yes | 78h |

8.2.140 XPIP_CSR 7 REGISTER – OFFSET 8B4h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|------------------------|------|-----------------|----------------------|---------|
| 25:24 | REV_TS_CTR | RW | Test used only. | Yes | 00 |
| 29:26 | MAC Control Parameter | RW | Test used only. | Yes | 0h |
| 30 | Line_Loopback | RW | Test used only. | Yes | 0 |
| 31 | P35_GEN2_MODE (Global) | RW | Test used only. | Yes | 0 |

8.2.141 PORT MISC 2 REGISTER – OFFSET 8B8h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|----------------|-------|-----------------|----------------------|---------|
| 0 | Change Role En | RW | Test used only. | Yes | 0 |
| 1 | IPCore Role | RW | Test used only. | Yes | 0 |
| 31:2 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.2.142 LED DISPLAY CSR REGISTER – OFFSET 8BCh (Global)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|----------|
| 5:0 | LED Display Mode Select | RW | Test used only. | Yes | 00_0000b |
| 7:6 | Reserved | RsvdP | Not Support. | No | 00b |
| 13:8 | Hotplug_Misc | RW | Bit[11:8] are used to control reset pulse for HotPlug function. Bit[8]: enable Bit[9]: issue reset pulse three times Bit[11:10]: control the width of the reset pulse 00b: 128 ms 01b: 256 ms 10b: 1 sec 11b: 2 sec Bit[12]: Reserved Bit[13]: enable the synchronize between IOE Interrupt and Hot-Plug state machine | Yes | 0h |
| 31:14 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.2.143 MULTI-CAST ENHANCED CAPABILITY HEADER REGISTER – OFFSET 900h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------|------|---------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 15:0 | Extended Capabilities ID | RO | Read as 0012h to indicate that these are PCI express extended capability registers for multi-cast capability. | No | 0012h |
| 19:16 | Capability Version | RO | Read as 1h. | No | 1h |
| 31:20 | Next Capability Offset | RO | Pointer points to 000h. | Yes | 000h |

8.2.144 MULTI-CAST CAPABILITY REGISTER – OFFSET 904h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|--------------------------------|------|----------------------------------------------------------------------------------|----------------------|----------|
| 5:0 | MC_Max_Group | RO | Value indicates the max. number of Multicast Groups that the component supports. | No | 00_0001b |
| 14:6 | Reserved | RO | Not Support. | No | 0 |
| 15 | MC_ECRC_Regeneration_Supported | RO | If set, indicates that ECRC regeneration is supported. | No | 0 |

8.2.145 MULTI-CAST CONTROL REGISTER – OFFSET 904h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------------|-------|--------------------------------------------------------------------|----------------------|---------|
| 16 | MC_Num_Group | RW | Value indicates the number of Multicast Groups configured for use. | No/Yes | 00h |
| 30:17 | Reserved | RsvdP | Not Support. | No | 0-0h |
| 31 | MC_ECRC_Regeneration_Supported | RW | When set, the Multicast mechanism is enabled for the component. | No/Yes | 0 |

8.2.146 MULTI-CAST BASE ADDRESS 0 REGISTER – OFFSET 908h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-------------------------|-------|---------------------------------------------------------------------------|----------------------|---------|
| 5:0 | MC_Index_Position | RW | The location of the LSB of the Multicast Group number within the address. | No/Yes | 00h |
| 11:6 | Reserved | RsvdP | Not Support. | No | 00h |
| 31:12 | MC_Base_Address [31:12] | RW | The base address of the Multicast address range. | No/Yes | 0-0h |

8.2.147 MULTI-CAST BASE ADDRESS 1 REGISTER – OFFSET 90Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-------------------------|------|--------------------------------------------------|----------------------|------------|
| 31:0 | MC_Base_Address [63:32] | RW | The base address of the Multicast address range. | No/Yes | 0000-0000h |

8.2.148 MULTI-CAST RECEIVER REGISTER – OFFSET 910h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|------------|-------|--------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 1:0 | MC_Receive | RW | For each bit that's Set, this Function gets a copy of any Multicast TLPs for the associated Multicast Group. | No/Yes | 00 |
| 31:2 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.2.149 MULTI-CAST BLOCK ALL REGISTER – OFFSET 918h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|--------------|-------|---------------------------------------------------------------------------------------------------------|----------------------|---------|
| 1:0 | MC_Block_All | RW | For each bit that is Set, this Function is blocked from sending TLPs to the associated Multicast Group. | No/Yes | 00 |
| 31:2 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.2.150 MULTI-CAST BLOCK UNTRANSLATED REGISTER – OFFSET 920h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-----------------------|-------|-------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 1:0 | MC_Block_Untranslated | RW | For each bit that is Set, this Function is blocked from sending TLPs containing Untranslated Addresses to the associated MCG. | No/Yes | 00 |
| 31:2 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.2.151 EEPROM_SCRATCHPAD REGISTER - OFFSET FB0h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-------------------|------|-----------------|----------------------|------------|
| 31:0 | EEPROM_Scratchpad | RO | Test used only. | Yes | 0000_0000h |

8.2.152 PCI EXPRESS ADVANCED ERROR REPORTING ENHANCED CAPABILITY HEADER REGISTER – OFFSET FB4h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|------------------------------|
| 15:0 | Extended Capabilities ID | RO | Read as 0001h to indicate that these are PCI express extended capability registers for advance error reporting. | No | 0001h |
| 19:16 | Capability Version | RO | Read as 1h. | No | 1h |
| 31:20 | Next Capability Offset | RO | Pointer points to the Power Budgeting Extended Capability structure for upstream port / the Port VC Extended Capability structure for downstream ports. | Yes | 138h for Up 148h for Down |

8.2.153 UNCORRECTABLE ERROR STATUS REGISTER – OFFSET FB8h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|------------------------------------|-------|------------------------------------------------------------------------------|----------------------|---------|
| 0 | Training Error Status | RW1C | When set, indicates that the Training Error event has occurred. | No/Yes | 0 |
| 3:1 | Reserved | RsvdP | Not Support. | No | 000 |
| 4 | Data Link Protocol Error Status | RW1C | When set, indicates that the Data Link Protocol Error event has occurred. | No/Yes | 0 |
| 11:5 | Reserved | RsvdP | Not Support. | No | 0-0b |
| 12 | Poisoned TLP Status | RW1C | When set, indicates that a Poisoned TLP has been received or generated. | No/Yes | 0 |
| 13 | Flow Control Protocol Error Status | RW1C | When set, indicates that the Flow Control Protocol Error event has occurred. | No/Yes | 0 |
| 14 | Completion Timeout Status | RW1C | When set, indicates that the Completion Timeout event has occurred. | No/Yes | 0 |
| 15 | Completer Abort Status | RW1C | When set, indicates that the Completer Abort event has occurred. | No/Yes | 0 |
| 16 | Unexpected Completion Status | RW1C | When set, indicates that the Unexpected Completion event has occurred. | No/Yes | 0 |
| 17 | Receiver Overflow Status | RW1C | When set, indicates that the Receiver Overflow event has occurred. | No/Yes | 0 |
| 18 | Malformed TLP Status | RW1C | When set, indicates that a Malformed TLP has been received. | No/Yes | 0 |
| 19 | ECRC Error Status | RW1C | When set, indicates that an ECRC Error has been detected. | No/Yes | 0 |
| 20 | Unsupported Request Error Status | RW1C | When set, indicates that an Unsupported Request event has occurred. | No/Yes | 0 |
| 21 | ACS Violation Status | RW1C | When set, indicates that an ACS Violation event has occurred. | No/Yes | 0 |
| 22 | Reserved | RsvdP | Not Support. | No | 0 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------------------|-------|----------------------------------------------------------------|----------------------|---------|
| 23 | MC Blocked TLP Status | RW1C | When set, indicates that an MC Blocked TLP event has occurred. | No/Yes | 0 |
| 31:24 | Reserved | RsvdP | Not Support. | No | 00h |

8.2.154 UNCORRECTABLE ERROR MASK REGISTER – OFFSET FBCh

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------------------------|-------|-------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | Training Error Mask | RW | When set, the Training Error event is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 3:1 | Reserved | RsvdP | Not Support. | No | 000b |
| 4 | Data Link Protocol Error Mask | RW | When set, the Data Link Protocol Error event is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 11:5 | Reserved | RsvdP | Not Support. | No | 0-0b |
| 12 | Poisoned TLP Mask | RW | When set, an event of Poisoned TLP is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 13 | Flow Control Protocol Error Mask | RW | When set, the Flow Control Protocol Error event is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 14 | Completion Timeout Mask | RW | When set, the Completion Timeout event is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 15 | Completer Abort Mask | RW | When set, the Completer Abort event is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 16 | Unexpected Completion Mask | RW | When set, the Unexpected Completion event is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 17 | Receiver Overflow Mask | RW | When set, the Receiver Overflow event is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 18 | Malformed TLP Mask | RW | When set, an event of Malformed TLP is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 19 | ECRC Error Mask | RW | When set, an event of ECRC Error is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 20 | Unsupported Request Error Mask | RW | When set, the Unsupported Request event is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 21 | ACS Violation Mask | RW | When set, the ACS Violation event is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 22 | Reserved | RsvdP | Not Support. | No | 0 |
| 23 | MC Blocked TLP Mask | RW | When set, the MC Blocked TLP event is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 31:24 | Reserved | RsvdP | Not Support. | No | 00h |

8.2.155 UNCORRECTABLE ERROR SEVERITY REGISTER – OFFSET FC0h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|--------------------------------------|-------|----------------------------|----------------------|---------|
| 0 | Training Error Severity | RW | 0b: Non-Fatal 1b: Fatal | No/Yes | 1 |
| 3:1 | Reserved | RsvdP | Not Support. | No | 000b |
| 4 | Data Link Protocol Error Severity | RW | 0b: Non-Fatal 1b: Fatal | No/Yes | 1 |
| 11:5 | Reserved | RsvdP | Not Support. | No | 0-0b |
| 12 | Poisoned TLP Severity | RW | 0b: Non-Fatal 1b: Fatal | No/Yes | 0 |
| 13 | Flow Control Protocol Error Severity | RW | 0b: Non-Fatal 1b: Fatal | No/Yes | 1 |
| 14 | Completion Timeout Error Severity | RW | 0b: Non-Fatal 1b: Fatal | No/Yes | 0 |
| 15 | Completer Abort Severity | RW | 0b: Non-Fatal 1b: Fatal | No/Yes | 0 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|------------------------------------|-------|----------------------------|----------------------|---------|
| 16 | Unexpected Completion Severity | RW | 0b: Non-Fatal 1b: Fatal | No/Yes | 0 |
| 17 | Receiver Overflow Severity | RW | 0b: Non-Fatal 1b: Fatal | No/Yes | 1 |
| 18 | Malformed TLP Severity | RW | 0b: Non-Fatal 1b: Fatal | No/Yes | 1 |
| 19 | ECRC Error Severity | RW | 0b: Non-Fatal 1b: Fatal | No/Yes | 0 |
| 20 | Unsupported Request Error Severity | RW | 0b: Non-Fatal 1b: Fatal | No/Yes | 0 |
| 21 | ACS Violation Severity | RW | 0b: Non-Fatal 1b: Fatal | No/Yes | 0 |
| 22 | Reserved | RsvdP | Not Support. | No | 0 |
| 23 | MC Blocked TLP Severity | RW | 0b: Not-Fatal 1b: Fatal | No/Yes | 0 |
| 31:24 | Reserved | RsvdP | Not Support. | No | 00h |

8.2.156 CORRECTABLE ERROR STATUS REGISTER – OFFSET FC4h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------------------------|-------|----------------------------------------------------------------|----------------------|---------|
| 0 | Receiver Error Status | RW1C | When set, the Receiver Error event is detected. | No/Yes | 0 |
| 5:1 | Reserved | RsvdP | Not Support. | No | 0 000b |
| 6 | Bad TLP Status | RW1C | When set, the event of Bad TLP has been received is detected. | No/Yes | 0 |
| 7 | Bad DLLP Status | RW1C | When set, the event of Bad DLLP has been received is detected. | No/Yes | 0 |
| 8 | REPLAY_NUM Rollover status | RW1C | When set, the REPLAY_NUM Rollover event is detected. | No/Yes | 0 |
| 11:9 | Reserved | RsvdP | Not Support. | No | 000b |
| 12 | Replay Timer Timeout status | RW1C | When set, the Replay Timer Timeout event is detected. | No/Yes | 0 |
| 13 | Advisory Non-Fatal Error status | RW1C | When set, the Advisory Non-Fatal Error event is detected. | No/Yes | 0 |
| 31:14 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.2.157 CORRECTABLE ERROR MASK REGISTER – OFFSET FC8h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-------------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | Receiver Error Mask | RW | When set, the Receiver Error event is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 5:1 | Reserved | RsvdP | Not Support. | No | 0 000b |
| 6 | Bad TLP Mask | RW | When set, the event of Bad TLP has been received is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 7 | Bad DLLP Mask | RW | When set, the event of Bad DLLP has been received is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 8 | REPLAY_NUM Rollover Mask | RW | When set, the REPLAY_NUM Rollover event is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 11:9 | Reserved | RsvdP | Not Support. | No | 000b |
| 12 | Replay Timer Timeout Mask | RW | When set, the Replay Timer Timeout event is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 13 | Advisory Non-Fatal Error Mask | RW | When set, the Advisory Non-Fatal Error event is not logged in the Header Long register and not issued as an Error Message to RC either. | No/Yes | 1 |
| 31:14 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.2.158 ADVANCE ERROR CAPABILITIES AND CONTROL REGISTER – OFFSET FCCh

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-------------------------|-------|-------------------------------------------------------------------------------------------------------|----------------------|---------|
| 4:0 | First Error Pointer | RO | It indicates the bit position of the first error reported in the Uncorrectable Error Status register. | No | 0_0000b |
| 5 | ECRC Generation Capable | RO | When set, it indicates the Switch has the capability to generate ECRC. | No | 1 |
| 6 | ECRC Generation Enable | RW | When set, it enables the generation of ECRC when needed. | No/Yes | 0 |
| 7 | ECRC Check Capable | RO | When set, it indicates the Switch has the capability to check ECRC. | No | 1 |
| 8 | ECRC Check Enable | RW | When set, the function of checking ECRC is enabled.. | No/Yes | 0 |
| 31:9 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.2.159 HEADER LOG REGISTER – OFFSET From FD0h to FDCh

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|--------|-----------------------|------|-------------------------------------------------------------------|----------------------|------------|
| 31:0 | 1 st DWORD | RO | Hold the 1st DWORD of TLP Header. The Head byte is in big endian. | No | 0000 0000h |
| 63:32 | 2 nd DWORD | RO | Hold the 2nd DWORD of TLP Header. The Head byte is in big endian. | No | 0000 0000h |
| 95:64 | 3 rd DWORD | RO | Hold the 3rd DWORD of TLP Header. The Head byte is in big endian. | No | 0000 0000h |
| 127:96 | 4 th DWORD | RO | Hold the 4th DWORD of TLP Header. The Head byte is in big endian. | No | 0000 0000h |

8.2.160 DIAGNOSTIC DATA 4 REGISTER – OFFSET FE0h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------|------|----------------------------------------------------------------------------------------|----------------------|---------|
| 3:0 | Lane4_Err_Cnt | RO | Test used only. Indicates the quality of errors detected by the PRBS data checkers. | No | 0h |
| 7:4 | Lane5_Err_Cnt | RO | Test used only. Indicates the quality of errors detected by the PRBS data checkers. | No | 0h |
| 11:8 | Lane6_Err_Cnt | RO | Test used only. Indicates the quality of errors detected by the PRBS data checkers. | No | 0h |
| 15:12 | Lane7_Err_Cnt | RO | Test used only. Indicates the quality of errors detected by the PRBS data checkers. | No | 0h |
| 19:16 | Lane12_Err_Cnt | RO | Test used only. Indicates the quality of errors detected by the PRBS data checkers. | No | 0h |
| 23:20 | Lane13_Err_Cnt | RO | Test used only. Indicates the quality of errors detected by the PRBS data checkers. | No | 0h |
| 27:24 | Lane14_Err_Cnt | RO | Test used only. Indicates the quality of errors detected by the PRBS data checkers. | No | 0h |
| 31:28 | Lane15_Err_Cnt | RO | Test used only. Indicates the quality of errors detected by the PRBS data checkers. | No | 0h |

8.2.161 CLOCK BUFFER CONTROL REGISTER – OFFSET FF8h (Global)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|-----|-------------|------|------------------------------------------------|----------------|---------|
| 8:0 | Buffer_Ctrl | RW | Used to control internal clock buffer outputs. | Yes | 000h |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|-------|------------------|-------|------------------------------------------------------------------------------------------------|----------------|---------|
| | | | Bit[8]: clkbuf_pd 0b: internal clock buffer power on 1b: internal clock buffer power off | | |
| 15:9 | Reserved | RsvdP | Not Support. | No | 0-0b |
| 23:16 | Clkreq_Buffer_En | RW | Used for L1PM function. | Yes | FFh |
| 31:24 | Reserved | RsvdP | Not Support | No | 00h |

8.2.162 CLOCK BUFFER PORT SELECT REGISTER – OFFSET FFCh (Global)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|------|--------------------|------|-----------------|----------------|------------|
| 31:0 | Buffer_Port_Select | RW | Test used only. | Yes | 0000_0000h |

8.3 NON TRANSPARENT PORT LINK INTERFACE CONFIGURATION REGISTERS – NT Mode Only

When the port of the Switch is set to operate at the non-transparent mode, it is represented by an Other Bridge that implements type 0 configuration space header. The following table details the allocation of the register fields of the PCI 2.3 compatible type 0 configuration space header.

| 31 – 24 | 23 – 16 | 15 – 8 | 7 – 0 | BYTE OFFSET |
|----------------------------------------------|------------------------|-----------------------|--------------------------------------|-------------|
| Device ID | | Vendor ID | | 00h |
| Primary Status | | Command | | 04h |
| Class Code | | | Revision ID | 08h |
| Reserved | Header Type | Reserved | Cache Line Size | 0Ch |
| BAR 0 | | | | 10h |
| BAR 1 | | | | 14h |
| BAR 2 | | | | 18h |
| BAR 3 | | | | 1Ch |
| BAR 4 | | | | 20h |
| BAR 5 | | | | 24h |
| Reserved | | | | 28h |
| SSID | | SSVID | | 2Ch |
| Reserved | | | | 30h |
| Reserved | | | Capability Pointer to 40h | 34h |
| Reserved | | | | 38h |
| Reserved | | Interrupt Pin | Interrupt Line | 3Ch |
| Power Management Capabilities | | Next Item Pointer=48h | Capability ID=01h | 40h |
| PM Data | PPB Support Extensions | Power Management Data | | 44h |
| Message Control | | Next Item Pointer=68h | Capability ID=05h | 48h |
| Message Address | | | | 4Ch |
| Message Upper Address | | | | 50h |
| Reserved | | Message Data | | 54h |
| Reserved | | | | 58h – 64h |
| PCI Express Capabilities Register | | Next Item Pointer=A4h | Capability ID=10h | 68h |
| Device Capabilities | | | | 6Ch |
| Device Status | | Device Control | | 70h |
| Link Capabilities | | | | 74h |
| Link Status | | Link Control | | 78h |
| Reserved | | | | 7Ch - 90h |
| Link Capabilities 2 | | | | 94h |
| Link Status 2 | | Link Control 2 | | 98h |
| Reserved | | | | 9Ch – A0h |
| Reserved | | Next Item Pointer=C8h | SSID/SSVID Capability ID=0Dh | A4h |
| SSID | | SSVID | | A8h |
| Reserved | | | | ACh – C4h |
| Length | | Next Item Pointer=00h | Vendor Specific Capability ID=09h | C8h |
| Vendor Specific Header Register | | | | CCh |
| Reserved | | | | D0h – E0h |
| NT Port Link Interface BAR 0-1 Configuration | | | | E4h |
| NT Port Link Interface BAR 2 Configuration | | | | E8h |
| NT Port Link Interface BAR 2-3 Configuration | | | | ECh |
| NT Port Link Interface BAR 4 Configuration | | | | F0h |
| NT Port Link Interface BAR 4-5 Configuration | | | | F4h |
| Reserved | | | | F8h - FCh |

Other than the PCI 2.3 compatible configuration space header, the Switch also implements PCI express extended configuration space header, which includes advanced error reporting, virtual channel, and power budgeting capability registers. The following table details the allocation of the register fields of PCI express extended capability space header. The first extended capability always begins at offset 100h with a PCI Express Enhanced Capability header and the rest of capabilities are located at an offset greater than 0FFh relative to the beginning of PCI compatible configuration space.

| 31 - 24 | 23 - 16 | 15 - 8 | 7 - 0 | BYTE OFFSET |
|--------------------------------------|-------------------------------------|------------------------------------------|----------------------------------|-------------|
| Next Capability Offset=FB4h | Cap. Version | PCI Express Extended Capability ID=0003h | | 100h |
| Serial Number Lower DW | | | | 104h |
| Serial Number Upper DW | | | | 108h |
| Reserved | | | | 10Ch - 134h |
| Next Capability Offset=148h | Cap. Version | PCI Express Extended Capability ID=0004h | | 138h |
| Reserved | | | Data Select Register | 13Ch |
| Data Register | | | | 140h |
| Reserved | | | Power Budget Capability Register | 144h |
| Next Capability Offset=000h | Cap. Version | PCI Express Extended Capability ID=0002h | | 148h |
| Port VC Capability Register 1 | | | | 14Ch |
| VC Arbitration Table Offset=4h | Port VC Capability Register 2 | | | 150h |
| Port VC Status | | Port VC Control | | 154h |
| Port Arbitration Table Offset=5h | VC Resource Capability Register (0) | | | 158h |
| VC Resource Control Register (0) | | | | 15Ch |
| VC Resource Status Register (0) | | Reserved | | 160h |
| Port Arbitration Table Offset=6h | VC Resource Capability Register (1) | | | 164h |
| VC Resource Control Register (1) | | | | 168h |
| VC Resource Status Register (1) | | Reserved | | 16Ch |
| Reserved | | | | 170h - 184h |
| VC Arbitration Table 0 | | | | 188h |
| VC Arbitration Table 1 | | | | 18Ch |
| VC Arbitration Table 2 | | | | 190h |
| VC Arbitration Table 3 | | | | 194h |
| Port VC0 Arbitration Table 0 (Low) | | | | 198h |
| Port VC0 Arbitration Table 0 (Upper) | | | | 19Ch |
| Port VC0 Arbitration Table 1 (Low) | | | | 1A0h |
| Port VC0 Arbitration Table 1 (Upper) | | | | 1A4h |
| Port VC1 Arbitration Table 0 (Low) | | | | 1A8h |
| Port VC1 Arbitration Table 0 (Upper) | | | | 1ACh |
| Port VC1 Arbitration Table 1 (Low) | | | | 1B0h |
| Port VC1 Arbitration Table 1 (Upper) | | | | 1B4h |
| Reserved | | | | 1B8h - 840h |
| XPIP_CSR 0 | | | | 844h |
| XPIP_CSR 1 | | | | 848h |
| Decode VGA | Reserved | | | 84Ch |
| Reserved | | | | 850h |
| Reserved | | XPIP_CSR 2 | | 854h |
| PHY Parameter 2 | | | | 858h |
| PHY Parameter 3 | | | | 85Ch |
| Reserved | | | | 860h |
| XPIP_CSR 3 | | | | 864h |
| Reserved | | | | 868h |
| XPIP_CSR 5 | | | | 86Ch |
| Reserved | | | | 870h |
| Operation Mode | | | | 874h |
| Reserved | | | | 878h - 88Ch |
| MAC_CSR 1 | | | | 890h |
| Reserved | | | | 894h - 8A0h |
| Power Saving Disable | | | | 8A4h |
| Transaction Layer_CSR | | | | 8A8h |
| ACK Latency Timer | | Replay Time-out Counter | | 8ACh |
| Reserved | | Port Misc 0 | | 8B0h |
| XPIP_CSR 7 | XPIP_CSR 6 | | Port Misc 1 | 8B4h |
| Reserved | | Port Misc 2 | | 8B8h |
| Reserved | | | | 8BCh - C30h |

PI7C9X2G1224GP

| 31 -24 | 23 - 16 | 15 - 8 | 7 -0 | BYTE OFFSET |
|--------------------------------------------------|--------------|------------------------------------------|------|-------------|
| Next Capability Offset=000h | Cap. Version | PCI Express Extended Capability ID=000Bh | | C34h |
| Vendor Specific Header | | | | C38h |
| Translation BAR 2 | | | | C3Ch |
| Translation BAR 3 | | | | C40h |
| Translation BAR 4 | | | | C44h |
| Translation BAR 5 | | | | C48h |
| Reserved | | Virtual IF IRQ Set | | C4Ch |
| Reserved | | Virtual IF IRQ Clear | | C50h |
| Reserved | | Virtual IF IRQ Mask Set | | C54h |
| Reserved | | Virtual IF IRQ Mask Clear | | C58h |
| Reserved | | Link IF IRQ Set | | C5Ch |
| Reserved | | Link IF IRQ Clear | | C60h |
| Reserved | | Link IF IRQ Mask Set | | C64h |
| Reserved | | Link IF IRQ Mask Clear | | C68h |
| Scratchpad 0 | | | | C6Ch |
| Scratchpad 1 | | | | C70h |
| Scratchpad 2 | | | | C74h |
| Scratchpad 3 | | | | C78h |
| Scratchpad 4 | | | | C7Ch |
| Scratchpad 5 | | | | C80h |
| Scratchpad 6 | | | | C84h |
| Scratchpad 7 | | | | C88h |
| Reserved | | | | C8Ch - D90h |
| Virtual Port 32-Bits LTT Entry 0 | | | | D94h |
| Virtual Port 32-Bits LTT Entry 1 | | | | D98h |
| Virtual Port 32-Bits LTT Entry 2 | | | | D9Ch |
| Virtual Port 32-Bits LTT Entry 3 | | | | DA0h |
| Virtual Port 32-Bits LTT Entry 4 | | | | DA4h |
| Virtual Port 32-Bits LTT Entry 5 | | | | DA8h |
| Virtual Port 32-Bits LTT Entry 6 | | | | DACh |
| Virtual Port 32-Bits LTT Entry 7 | | | | DB0h |
| Link Port 16-Bits LTT Entry 0-1 | | | | DB4h |
| Link Port 16-Bits LTT Entry 2-3 | | | | DB8h |
| Link Port 16-Bits LTT Entry 4-5 | | | | DBCh |
| Link Port 16-Bits LTT Entry 6-7 | | | | DC0h |
| Link Port 16-Bits LTT Entry 8-9 | | | | DC4h |
| Link Port 16-Bits LTT Entry 10-11 | | | | DC8h |
| Link Port 16-Bits LTT Entry 12-13 | | | | DCCh |
| Link Port 16-Bits LTT Entry 14-15 | | | | DD0h |
| Link Port 16-Bits LTT Entry 16-17 | | | | DD4h |
| Link Port 16-Bits LTT Entry 18-19 | | | | DD8h |
| Link Port 16-Bits LTT Entry 20-21 | | | | DDCh |
| Link Port 16-Bits LTT Entry 22-23 | | | | DE0h |
| Link Port 16-Bits LTT Entry 24-25 | | | | DE4h |
| Link Port 16-Bits LTT Entry 26-27 | | | | DE8h |
| Link Port 16-Bits LTT Entry 28-29 | | | | DECh |
| Link Port 16-Bits LTT Entry 30-31 | | | | DF0h |
| Fail-Over CSR | | | | DF4h |
| Reserved | | | | DF8h - FACH |
| EEPROM Scratchpad | | | | FB0h |
| Next Capability Offset=138h | Cap. Version | PCI Express Extended Capability ID=0001h | | FB4h |
| Uncorrectable Error Status Register | | | | FB8h |
| Uncorrectable Error Mask Register | | | | FBCh |
| Uncorrectable Error Severity Register | | | | FC0h |
| Correctable Error Status Register | | | | FC4h |
| Correctable Error Mask Register | | | | FC8h |
| Advanced Error Capabilities and Control Register | | | | FCCh |
| Header Log Register 0 | | | | FD0h |
| Header Log Register 1 | | | | FD4h |
| Header Log Register 2 | | | | FD8h |
| Header Log Register 3 | | | | FDCh |
| Reserved | | | | FE0h - FFCh |

8.3.1 VENDOR ID REGISTER – OFFSET 00h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-----------|------|--------------------------------------------------|----------------------|---------|
| 15:0 | Vendor ID | RO | Identifies Pericom as the vendor of this device. | Yes | 12D8h |

8.3.2 DEVICE ID REGISTER – OFFSET 00h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------|------|-----------------------------------------------|----------------------|---------|
| 31:16 | Device ID | RO | Identifies this device as the PI7C9X2G1224GP. | Yes | 1224h |

8.3.3 COMMAND REGISTER – OFFSET 04h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|------------------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | I/O Space Enable | RW | 0b: Ignores I/O transactions on the primary interface 1b: Enables responses to I/O transactions on the primary interface | No/Yes | 0 |
| 1 | Memory Space Enable | RW | 0b: Ignores memory transactions on the primary interface 1b: Enables responses to memory transactions on the primary interface | No/Yes | 0 |
| 2 | Bus Master Enable | RW | 0b: Does not initiate memory or I/O transactions on the upstream port and handles as an Unsupported Request (UR) to memory and I/O transactions on the downstream port. For Non-Posted Requests, a completion with UR completion status must be returned 1b: Enables the Switch Port to forward memory and I/O Read/Write transactions in the upstream direction | No/Yes | 0 |
| 3 | Special Cycle Enable | RsvdP | Not Support. | No | 0 |
| 4 | Memory Write And Invalidate Enable | RsvdP | Not Support. | No | 0 |
| 5 | VGA Palette Snoop Enable | RsvdP | Not Support. | No | 0 |
| 6 | Parity Error Response Enable | RW | 0b: Switch may ignore any parity errors that it detects and continue normal operation 1b: Switch must take its normal action when a parity error is detected | No/Yes | 0 |
| 7 | Wait Cycle Control | RsvdP | Not Support. | No | 0 |
| 8 | SERR# enable | RW | 0b: Disables the reporting of Non-fatal and Fatal errors detected by the Switch to the Root Complex 1b: Enables the Non-fatal and Fatal error reporting to Root Complex | No/Yes | 0 |
| 9 | Fast Back-to-Back Enable | RsvdP | Not Support. | No | 0 |
| 10 | Interrupt Disable | RW | 0b: Enable to generate INTx Interrupt Messages 1b: Disable to generate INTx Interrupt Messages | No/Yes | 0 |
| 15:11 | Reserved | RsvdP | Reset to 5'b0. | No | 0000 0b |

8.3.4 PRIMARY STATUS REGISTER – OFFSET 04h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-------------------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 18:16 | Reserved | RsvdP | Not Support. | No | 000b |
| 19 | Interrupt Status | RO | Indicates that an INTx Interrupt Message is pending internally to the device. In the Switch, the forwarding of INTx messages from the downstream device of the Switch port is not reflected in this bit. Must be hardwired to 1'b0. | No | 0 |
| 20 | Capabilities List | RO | Set to 1b to enable support for the capability list (offset 34h is the pointer to the data structure). | No | 1 |
| 21 | 66MHz Capable | RsvdP | Not Support. | No | 0 |
| 22 | Reserved | RsvdP | Not Support. | No | 0 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 23 | Fast Back-to-Back Capable | RsvdP | Not Support. | No | 0 |
| 24 | Master Data Parity Error | RW1C | Set to 1b (by a requester) whenever a Parity error is detected or forwarded on the primary side of the port in a Switch. If the Parity Error Response Enable bit is cleared, this bit is never set. | No/Yes | |
| 26:25 | DEVSEL# timing | RsvdP | Not Support. | No | 00b |
| 27 | Signaled Target Abort | RsvdP | Not Support. | No | 0 |
| 28 | Received Target Abort | RsvdP | Not Support. | No | 0 |
| 29 | Received Master Abort | RsvdP | Not Support. | No | 0 |
| 30 | Signaled System Error | RW1C | Set to 1b when the Switch sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR Enable bit in the Command register is 1. | No/Yes | 0 |
| 31 | Detected Parity Error | RW1C | Set to 1b whenever the primary side of the port in a Switch receives a Poisoned TLP. | No/Yes | 0 |

8.3.5 REVISION ID REGISTER – OFFSET 08h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|----------|------|--------------------------------------|----------------------|---------|
| 7:0 | Revision | RO | Indicates revision number of device. | No/Yes | 00h |

8.3.6 CLASS CODE REGISTER – OFFSET 08h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------------------|------|---------------------------------------------------------------------------------------------|----------------------|---------|
| 15:8 | Programming Interface | RO | Read as 00h to indicate no programming interfaces have been defined for PCI-to-PCI Bridges. | No | 00h |
| 23:16 | Sub-Class Code | RO | Read as 80h to indicate device is an Other Bridge. | No | 80h |
| 31:24 | Base Class Code | RO | Read as 06h to indicate device is a Bridge device. | No | 06h |

8.3.7 CACHE LINE REGISTER – OFFSET 0Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|-----------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 7:0 | Cache Line Size | RW | The cache line size register is set by the system firmware and the operating system cache line size. This field is implemented by PCI Express devices as a RW field for legacy compatibility, but it has no impact on any PCI Express device functionality. | No/Yes | 00h |

8.3.8 PRIMARY LATENCY TIMER REGISTER – OFFSET 0Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-----------------------|-------|--------------|----------------------|---------|
| 15:8 | Primary Latency Timer | RsvdP | Not Support. | No | 00h |

8.3.9 HEADER TYPE REGISTER – OFFSET 0Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-------------|------|-----------------------------------------------------------------------------------------------------------|----------------------|---------|
| 23:16 | Header Type | RO | Read as 00h to indicate that the register layout conforms to Type 0 Configuration Header for the NT Port. | No | 00h |

8.3.10 BAR 0 REGISTER – OFFSET 10h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|------------------------|-------|-----------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | Memory Space Indicator | RO | Reset to 0b to indicate the Base Address register maps NT Port Configuration registers into Memory Space. | No | 0 |
| 2:1 | Memory Map Type | RO | 00b: support 32-bit Memory Space. 10b: support 64-bit Memory Space. | No | 00b |
| 3 | Prefetchable | RO | Reset to 0b to indicate NT Port Configuration registers maps to Non-Prefetchable Memory Space. | No | 0 |
| 16:4 | Reserved | RsvdP | Not Support. | No | 0-0h |
| 31:17 | Base Address 0 | RW | Use this Memory base address to map the NT-Port Configuration registers. | No/Yes | 0-0h |

8.3.11 BAR 1 REGISTER – OFFSET 14h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|----------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|------------|
| 31:0 | Base Address 1 | RW | RO when the Base Address 0 register is not 64-bit addressing (offset 10h[2:1] is not 10b). RW when the Base Address 0 register is 64-bit addressing. Base Address 1 is used to provide the upper 32 Address bits when offset 10h[2:1] is set to 10b. | No/Yes | 0000_0000h |

8.3.12 BAR 2 REGISTER – OFFSET 18h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|------------------------|-------|------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | Memory Space Indicator | RO | Reset to 0b to indicate it is a Memory BAR. | No | 0 |
| 2:1 | Memory Map Type | RO | 00b: support 32-bit Memory Space 10b: support 64-bit Memory Space | No | 00b |
| 3 | Prefetchable | RO | Reset to 0b to indicate NT Port Configuration registers maps to Non-Prefetchable Memory Space. | No | 0 |
| 19:4 | Reserved | RsvdP | Not Support. | No | 0-0h |
| 31:20 | Base Address 2 | RW | Base Address 2. | No/Yes | 000h |

8.3.13 BAR 3 REGISTER – OFFSET 1Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|------------------------|------|--------------------------------------------------------------------------|----------------------|---------|
| 0 | Memory Space Indicator | RO | When 18h[2:1]=00b, BAR 3 is used as an independent 32-bit BAR. | No | 0 |
| | | RW | When 18h[2:1]=10b, BAR 3 is used as the upper 32 bits of 64-bit BAR 2/3. | No/Yes | 0 |
| 2:1 | Memory Map Type | RO | When 18h[2:1]=00b, BAR 3 is used as an independent 32-bit BAR. | No | 00b |
| | | RW | When 18h[2:1]=10b, BAR 3 is used as the upper 32 bits of 64-bit BAR 2/3. | No/Yes | 00b |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|----------------|-------|--------------------------------------------------------------------------|----------------------|-----------|
| 3 | Prefetchable | RO | When 18h[2:1]=00b, BAR 3 is used as an independent 32-bit BAR. | No | 0 |
| | | RW | When 18h[2:1]=10b, BAR 3 is used as the upper 32 bits of 64-bit BAR 2/3. | No/Yes | 0 |
| 31:4 | Base Address 3 | RsvdP | When 18h[2:1]=00b, BAR 3 is used as an independent 32-bit BAR. | No | 0000_000h |
| | | RW | When 18h[2:1]=10b, BAR 3 is used as the upper 32 bits of 64-bit BAR 2/3. | No/Yes | 0000_000h |

8.3.14 BAR 4 REGISTER – OFFSET 20h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|------------------------|-------|------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | Memory Space Indicator | RO | Reset to 0b to indicate it is a Memory BAR. | No | 0 |
| 2:1 | Memory Map Type | RO | 00b: support 32-bit Memory Space 10b: support 64-bit Memory Space | No | 00b |
| 3 | Prefetchable | RO | Reset to 0b to indicate NT Port Configuration registers maps to Non-Prefetchable Memory Space. | No | 0 |
| 19:4 | Reserved | RsvdP | Not Support. | No | 0-0h |
| 31:20 | Base Address 4 | RW | Base Address 4. | No/Yes | 000h |

8.3.15 BAR 5 REGISTER – OFFSET 24h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|------------------------|-------|--------------------------------------------------------------------------|----------------------|-----------|
| 0 | Memory Space Indicator | RO | When 20h[2:1]=00b, BAR 5 is used as an independent 32-bit BAR. | No | 0 |
| | | RW | When 20h[2:1]=10b, BAR 5 is used as the upper 32 bits of 64-bit BAR 4/5. | No/Yes | 0 |
| 1 | Memory Space Enable | RO | When 20h[2:1]=00b, BAR 5 is used as an independent 32-bit BAR. | No | 00b |
| | | RW | When 20h[2:1]=10b, BAR 5 is used as the upper 32 bits of 64-bit BAR 4/5. | No/Yes | 00b |
| 2:1 | Memory Map Type | RO | When 20h[2:1]=00b, BAR 5 is used as an independent 32-bit BAR. | No | 0 |
| 3 | Prefetchable | RW | When 20h[2:1]=10b, BAR 5 is used as the upper 32 bits of 64-bit BAR 4/5. | No/Yes | 0 |
| 31:4 | Base Address 3 | RsvdP | When 20h[2:1]=00b, BAR 5 is used as an independent 32-bit BAR. | No | 0000_000h |
| | | RW | When 20h[2:1]=10b, BAR 5 is used as the upper 32 bits of 64-bit BAR 4/5. | No/Yes | 0000_000h |

8.3.16 SUBSYSTEM VENDOR ID REGISTER – OFFSET 2Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|----------|------|----------------------------------------|----------------------|---------|
| 15:0 | SSVID | RO | It indicates the sub-system vendor id. | No/Yes | 12D8h |

8.3.17 SUBSYSTEM ID REGISTER – OFFSET 2Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------|------|----------------------------------------|----------------------|---------|
| 31:16 | SSID | RO | It indicates the sub-system device id. | No/Yes | 1224h |

8.3.18 CAPABILITY POINTER REGISTER – OFFSET 34h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|--------------------|------|------------------------------------|----------------------|---------|
| 7:0 | Capability Pointer | RO | Indicates next capability pointer. | Yes | 40h |

8.3.19 INTERRUPT LINE REGISTER – OFFSET 3Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|----------------|------|---------------------------|----------------------|---------|
| 7:0 | Interrupt Line | RW | Indicates Interrupt Line. | No/Yes | 00h |

8.3.20 INTERRUPT PIN REGISTER – OFFSET 3Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|---------------|------|-------------------------------------------------------------------------------------|----------------------|---------|
| 15:8 | Interrupt Pin | RO | The Switch implements INTA virtual wire interrupt signal. Only 00h or 01h is valid. | Yes | 01h |

8.3.21 POWER MANAGEMENT CAPABILITIES REGISTER – OFFSET 40h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------------|-------|----------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 7:0 | Enhanced Capabilities ID | RO | Read as 01h to indicate that these are power management enhanced capability registers. | No | 01h |
| 15:8 | Next Item Pointer | RO | The pointer points to the MSI capability Structure. | Yes | 48h |
| 18:16 | Power Management Revision | RO | Read as 011b to indicate the device is compliant to Revision 1.2 of <i>PCI Power Management Interface Specifications</i> . | No | 011b |
| 19 | PME# Clock | RsvdP | Not Support. | No | 0 |
| 20 | Reserved | RsvdP | Not Support. | No | 0 |
| 21 | Device Specific Initialization | RO | Read as 0b to indicate Switch does not have device specific initialization requirements. | Yes | 0 |
| 24:22 | AUX Current | RO | Reset to 000b. | Yes | 000b |
| 25 | D1 Power State Support | RO | Read as 0b to indicate Switch does not support the D1 power management state. | Yes | 0 |
| 26 | D2 Power State Support | RO | Read as 0b to indicate Switch does not support the D2 power management state. | Yes | 0 |
| 31:27 | PME# Support | RO | Read as 19h to indicate Switch supports the forwarding of PME# message in D0, D3 and D4 states. | Yes | 19h |

8.3.22 POWER MANAGEMENT DATA REGISTER – OFFSET 44h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|-------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 1:0 | Power State | RW | Indicates the current power state of the Switch. Writing a value of D0 when the previous state was D3 cause a hot reset without asserting DWRN_RST_L. 00b: D0 state 01b: D1 state 10b: D2 state 11b: D3 hot state | No/Yes | 00b |
| 2 | Reserved | RsvdP | Not Support. | No | 0 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 3 | No_Soft_Reset | RO | When set, this bit indicates that device transitioning from D3hot to D0 does not perform an internal reset. When clear, an internal reset is performed when power state transits from D3hot to D0. | Yes | 1 |
| 7:4 | Reserved | RsvdP | Not Support. | No | 0h |
| 8 | PME# Enable | RW | When asserted, the Switch will generate the PME# message. | No/Yes | 0 |
| 12:9 | Data Select | RW | Select data registers RW if offset 870h[1]=1 and RO if offset 870h[1]=0. | No/Yes | 0h |
| 14:13 | Data Scale | RO | Reset to 00b. | No | 00b |
| 15 | PME Status | RO | Read as 0b as the PME# message is not implemented. | No | 0 |

8.3.23 PPB SUPPORT EXTENSIONS – OFFSET 44h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------------------------|-------|--------------------------------------------------------|----------------------|----------|
| 21:16 | Reserved | RsvdP | Not Support. | No | 00_0000b |
| 22 | B2_B3 Support for D3HOT | RO | Does not apply to PCI Express. Must be hardwired to 0. | No | 0 |
| 23 | Bus Power / Clock Control Enable | RO | Does not apply to PCI Express. Must be hardwired to 0. | No | 0 |

8.3.24 DATA REGISTER – OFFSET 44h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------|------|----------------|----------------------|---------|
| 31:24 | Data Register | RO | Data Register. | Yes | 00h |

8.3.25 MSI CAPABILITIES REGISTER – OFFSET 48h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 7:0 | Enhanced Capabilities ID | RO | Read as 05h to indicate that this is message signal interrupt capability register. | No | 05h |
| 15:8 | Next Item Pointer | RO | Indicates next capability pointer. | Yes | 68h |
| 16 | MSI Enable | RW | 0b: The function is prohibited from using MSI to request service 1b: The function is permitted to use MSI to request service and is prohibited from using its INTx # pin | No/Yes | 0 |
| 19:17 | Multiple Message Capable | RO | Do not support multiple messages. | No | 000b |
| 22:20 | Multiple Message Enable | RW | Reset to 000b. | No/Yes | 000b |
| 23 | 64-bit address capable | RO | 0b: The function is not capable of generating a 64-bit message address 1b: The function is capable of generating a 64-bit message address | No | 1b |
| 31:24 | Reserved | RsvdP | Not Support. | No | 00h |

8.3.26 MESSAGE ADDRESS REGISTER – OFFSET 4Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-----------------|-------|-------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 1:0 | Reserved | RsvdP | Not Support. | No | 00b |
| 31:2 | Message Address | RW | If the message enable bit is set, the contents of this register specify the DWORD aligned address for MSI memory write transaction. | No/Yes | 0-0h |

8.3.27 MESSAGE UPPER ADDRESS REGISTER – OFFSET 50h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-----------------------|------|-----------------------------------------------------------------------------------------|----------------------|------------|
| 31:0 | Message Upper Address | RW | This register is only effective if the device supports a 64-bit message address is set. | No/Yes | 0000_0000h |

8.3.28 MESSAGE DATA REGISTER – OFFSET 54h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|--------------|------|---------------|----------------------|---------|
| 15:0 | Message Data | RW | Message data. | No/Yes | 0000h |

8.3.29 PCI EXPRESS CAPABILITIES REGISTER – OFFSET 68h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------|-------|-------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 7:0 | Enhanced Capabilities ID | RO | Read as 10h to indicate that these are PCI express enhanced capability registers. | No | 10h |
| 15:8 | Next Item Pointer | RO | Pointer points to the SSID/SSVID Extended Capability Structure. | Yes | A4h |
| 19:16 | Capability Version | RO | Read as 2h to indicate the device is compliant to Revision .2.0 of <i>PCI Express Base Specifications</i> . | No | 2h |
| 23:20 | Device/Port Type | RO | Indicates the type of PCI Express logical device. | No | 0h |
| 24 | Slot Implemented | RO | Reset to 0b. | No | 0 |
| 29:25 | Interrupt Message Number | RO | Read as 0. No MSI messages are generated in the transparent mode. | No | 00_000b |
| 31:30 | Reserved | RsvdP | Not Support. | No | 00b |

8.3.30 DEVICE CAPABILITIES REGISTER – OFFSET 6Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------------------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 2:0 | Max_Payload_Size Supported | RO | Indicates the maximum payload size that the device can support for TLPs. 000b: 128 payload size 001b: 256 payload size 010b: 512 payload size | Yes | 001b |
| 4:3 | Phantom Functions Supported | RO | Indicates the support for use of unclaimed function numbers as Phantom functions. Read as 00b, since the Switch does not act as a requester. | No | 00b |
| 5 | Extended Tag Field Supported | RO | Indicates the maximum supported size of Tag field as a Requester. Read as 0, since the Switch does not act as a requester. | No | 0 |
| 8:6 | Endpoint L0s Acceptable Latency | RO | Acceptable total latency that an Endpoint can withstand due to the transition from L0s state to the L0 state. For Switch, the ASPM software would not check this value. | No | 111b |
| 11:9 | Endpoint L1 Acceptable Latency | RO | Acceptable total latency that an Endpoint can withstand due to the transition from L1 state to the L0 state. For Switch, the ASPM software would not check this value. | No | 111b |
| 14:12 | Reserved | RsvdP | Not Support. | No | 000b |
| 15 | Role_Based Error Reporting | RO | When set, indicates that the device implements the functionality originally defined in the Error Reporting ECN. | Yes | 1 |
| 17:16 | Reserved | RsvdP | Not Support. | No | 00b |
| 25:18 | Captured Slot Power Limit Value | RO | In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. This value is set by the Set_Slot_Power_Limit message. | No | 00h |
| 27:26 | Captured Slot Power Limit Scale | RO | Specifies the scale used for the Slot Power Limit Value. | No | 00b |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------|-------|------------------------------------------------------------------------|----------------------|---------|
| 31:28 | Reserved | RsvdP | This value is set by the Set_Slot_Power_Limit message. Not Support. | No | 0h |

8.3.31 DEVICE CONTROL REGISTER – OFFSET 70h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | Correctable Error Reporting Enable | RW | 0b: Disable Correctable Error Reporting 1b: Enable Correctable Error Reporting | No/Yes | 0 |
| 1 | Non-Fatal Error Reporting Enable | RW | 0b: Disable Non-Fatal Error Reporting 1b: Enable Non-Fatal Error Reporting | No/Yes | 0 |
| 2 | Fatal Error Reporting Enable | RW | 0b: Disable Fatal Error Reporting 1b: Enable Fatal Error Reporting | No/Yes | 0 |
| 3 | Unsupported Request Reporting Enable | RW | 0b: Disable Unsupported Request Reporting 1b: Enable Unsupported Request Reporting | No/Yes | 0 |
| 4 | Enable Relaxed Ordering | RO | When set, it permits the device to set the Relaxed Ordering bit in the attribute field of transaction. Since the Switch can not either act as a requester or alter the content of packet it forwards, this bit always returns '0' when read. | No | 0 |
| 7:5 | Max_Payload_Size | RW | This field sets maximum TLP payload size for the device. Permissible values that can be programmed are indicated by the Max_Payload_Size Supported in the Device Capabilities register. Any value exceeding the Max_Payload_Size Supported written to this register results into clamping to the Max_Payload_Size Supported value. | No/Yes | 000b |
| 8 | Extended Tag Field Enable | RsvdP | Not Support. | No | 0 |
| 9 | Phantom Function Enable | RsvdP | Not Support. | No | 0 |
| 10 | Auxiliary (AUX) Power PM Enable | RsvdP | Not Support. | No | 0 |
| 11 | Enable No Snoop | RsvdP | Not Support. | No | 0 |
| 14:12 | Max_Read_Request_Size | RO | This field sets the maximum Read Request size for the device as a Requester. Since the Switch does not generate read request by itself, these bits are hardwired to 0. | No | 000b |
| 15 | Reserved | RsvdP | Not Support. | No | 0 |

8.3.32 DEVICE STATUS REGISTER – OFFSET 70h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|------------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 16 | Correctable Error Detected | RW1C | Asserted when correctable error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. | No/Yes | 0 |
| 17 | Non-Fatal Error Detected | RW1C | Asserted when non-fatal error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. | No/Yes | 0 |
| 18 | Fatal Error Detected | RW1C | Asserted when fatal error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. | No/Yes | 0 |
| 19 | Unsupported Request Detected | RW1C | Asserted when unsupported request is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. | No/Yes | 0 |
| 20 | AUX Power Detected | RO | Asserted when the AUX power is detected by the Switch | No | 0 |
| 21 | Transactions Pending | RO | Each port of Switch does not issue Non-posted Requests on its own behalf, so this bit is hardwired to 0. | No | 0 |
| 31:22 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.3.33 LINK CAPABILITIES REGISTER – OFFSET 74h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------------------------------------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------------------------------------|
| 3:0 | Maximum Link Speed | RO | Indicates the maximum speed of the Express link. 0001b: 2.5 Gb/s 0010b: 5.0Gb/s Others: Reserved | No | 1h |
| 9:4 | Maximum Link Width | HWInt RO | Indicates the maximum width of the given PCIe Link. 00_0001b: x1 link 00_0010b: x2 link 00_0100b: x4 link 00_1000b: x8 link Others: Reserved | No | 08h, 04h, 02h or 01h |
| 11:10 | Active State Power Management (ASPM) Support | RO | Indicates the level of ASPM supported on the given PCIe Link. Each port of Switch supports L0s and L1 entry. | Yes | 01b |
| 14:12 | L0s Exit Latency | RO | Indicates the L0s exit latency for the given PCIe Link. The length of time this port requires to complete transition from L0s to L0 is in the range of 256ns to less than 512ns. | Yes | 011b |
| 17:15 | L1 Exit Latency | RO | Indicates the L1 exit latency for the given PCIe Link. The length of time this port requires to complete transition from L1 to L0 is less than 1us. | Yes | 000b |
| 18 | Clock Power Management | RO | A value of 1b indicates that component tolerates the removal of any reference clock via CLKREQ#. | Yes | 1 |
| 19 | Surprise Down Capability Enable | RsvdP | Not Support. | No | 0 |
| 20 | Data Link Layer Active Reporting Capable | RsvdP | Not Support. | No | 0 |
| 21 | Link BW Notify Capability | RsvdP | Not Support. | No | 0 |
| 23:20 | Reserved | RsvdP | Not Support. | No | 0-0h |
| 31:24 | Port Number | RO | Indicates the NT-Port Number. | Yes | 00h... port 0 01h... port 1 ... |

8.3.34 LINK CONTROL REGISTER – OFFSET 78h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|----------------------------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 1:0 | Active State Power Management (ASPM) Control | RW | 00b: ASPM is Disabled 01b: L0s Entry Enabled 10b: L1 Entry Enabled 11b: L0s and L1 Entry Enabled Note that the receiver must be capable of entering L0s even when the field is disabled | No/Yes | 00b |
| 2 | Reserved | RsvdP | Not Support. | No | 0 |
| 3 | Read Completion Boundary (RCB) | RO | Does not apply to PCI Express Switch. Returns '0' when read. | No | 0 |
| 4 | Link Disable | RsvdP | Not Support. | No | 0 |
| 5 | Retrain Link | RsvdP | Not Support. | No | 0 |
| 6 | Common Clock Configuration | RW | 0b: The components at both ends of a link are operating with synchronous reference clock. 1b: The components at both ends of a link are operating with a distributed common reference clock | No/Yes | 0 |
| 7 | Extended Synch | RW | When set, it transmits 4096 FTS ordered sets in the L0s state for entering L0 state and transmits 1024 TS1 ordered sets in the L1 state for entering L0 state. | No/Yes | 0 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------------------------|-------|----------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 8 | Enable Clock Power Management | RW | 0b: clock power management is disable and must hold CLKREQ# low. 1b: device is permitted to use CLKREQ# to power manage link clock. | No/Yes | 0 |
| 9 | HW Autonomous Width Disable | RW | Reset to 0b. | No/Yes | 0 |
| 10 | Link Bandwidth Management Interrupt Enable | RW | Reset to 0b. | No/Yes | 0 |
| 11 | Link Autonomous Bandwidth Interrupt Enable | RW | Reset to 0b.. | No/Yes | 0 |
| 15:12 | Reserved | RsvdP | Not Support. | No | 00h |

8.3.35 LINK STATUS REGISTER – OFFSET 78h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------------------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 19:16 | Link Speed | RO | Indicate the negotiated speed of the Express link. 1h: link to 2.5 Gb/s 2h: link to 5.0 Gb/s | No | 1h |
| 25:20 | Negotiated Link Width | RO | Indicates the negotiated width of the given PCIe link. 01h: x1 link 02h: x2 link 04h: x4 link | No | 01h |
| 26 | Training Error | RsvdP | Not Support. | No | 0 |
| 27 | Link Training | RsvdP | Not Support. | No | 0 |
| 28 | Slot Clock Configuration | RO | 0b: the Switch uses an independent clock corresponsive of the presence of a reference on the connector 1b: the Switch uses the same reference clock that the platform provides on the connector | Yes | 1 |
| 29 | Data Link Layer Link Active | RsvdP | Not Support. | No | 0 |
| 30 | Link Bandwidth Management Status | RO | Reset to 0b. | No | 0 |
| 31 | Link Autonomous Bandwidth Status | RO | Reset to 0b. | No | 0 |

8.3.36 LINK CONTROL REGISTER 2 – OFFSET 94h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|----------|-------|--------------|----------------------|---------|
| 31:0 | Reserved | RsvdP | Not Support. | No | 000b |

8.3.37 LINK CONTROL REGISTER 2 – OFFSET 98h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|-----------------------------------|------|----------------------------------------------------------------------------------------------------------|----------------------|---------|
| 3:0 | Target Link Speed | RW | 0001b: target link speed set to 2.5 Gb/s 0010b: target link speed set to 5.0 Gb/s Others: Reserved | No/Yes | 2h |
| 4 | Enter Compliance | RW | 1b: enter compliance mode | No/Yes | 0 |
| 5 | Hardware Autonomous Speed Disable | RW | Not Support. | No | 0 |
| 6 | Selectable De-Emphasis | RO | Not Support. | No | 0 |
| 9:7 | Tran_Margin | RW | Test used only. | No/Yes | 000b |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-------------------------|-------|--------------|----------------------|---------|
| 10 | Enter Modify Compliance | RW | Not Support. | No | 0 |
| 11 | Compliance SOS | RW | Not Support. | No | 0 |
| 12 | Compliance_Deemp | RW | Not Support. | No | 0 |
| 15:13 | Reserved | RsvdP | Not Support. | No | 000b |

8.3.38 LINK STATUS REGISTER 2 – OFFSET 98h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------------------|------|------------------------|----------------------|---------|
| 16 | Current De-emphasis level | RO | 0b: -6dB 1b: -3.5dB | No | 0 |
| 31:17 | Link status 2 | RO | Not Support. | No | 0-0h |

8.3.39 SSID/SSVID CAPABILITIES REGISTER – OFFSET A4h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------------------|-------|-------------------------------------------------------------------------|----------------------|---------|
| 7:0 | SSID/SSVID Capabilities ID | RO | Read as 0Dh to indicate that these are SSID/SSVID capability registers. | No | 0Dh |
| 15:8 | Next Item Pointer | RO | Indicates next capability pointer. | Yes | C8h |
| 31:16 | Reserved | RsvdP | Not Support. | No | 0000h |

8.3.40 SUBSYSTEM VENDOR ID REGISTER – OFFSET A8h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|----------|------|----------------------------------------|----------------------|---------|
| 15:0 | SSVID | RO | It indicates the sub-system vendor id. | Yes | 12D8h |

8.3.41 SUBSYSTEM ID REGISTER – OFFSET A8h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------|------|----------------------------------------|----------------------|---------|
| 31:16 | SSID | RO | It indicates the sub-system device id. | Yes | 8619h |

8.3.42 VENDOR SPECIFIC CAPABILITIES REGISTER – OFFSET C8h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------|------|--------------------------------------------------------------------------------------------|----------------------|---------|
| 7:0 | Enhanced Capabilities ID | RO | Read as 09h to indicate that these are vendor specific capability registers. | No | 09h |
| 15:8 | Next Item Pointer | RO | Read as 00h. No other ECP registers. | No | 00h |
| 31:16 | Length Information | RO | The length field provides the information for number of bytes in the capability structure. | No | 0038h |

8.3.43 VENDOR SPECIFIC HEADER REGISTER – OFFSET CCh

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|----------|-------|----------------------|----------------------|------------|
| 31:0 | Reserved | RsvdP | Reset to 0380_0002h. | No | 0380_0002h |

8.3.44 NT PORT LINK INTERFACE BAR 0-1 CONFIGURATION REGISTER – OFFSET E4h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-------------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 1:0 | BAR0 Type | RW | 00b: Disable BAR0/1 01b: Reserved 10b: BAR0 is implemented as a 32-bit Memory BAR 11b: BAR0/1 is implemented as a 64-bit Memory BAR | Yes | 10b |
| 2 | BAR0 Prefetchable | RW | 0b: Non Prefetchable 1b: Prefetchable | Yes | 0 |
| 31:3 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.3.45 NT PORT LINK INTERFACE BAR 2 CONFIGURATION REGISTER – OFFSET E8h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------|-------|----------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | Type Selector | RsvdP | Not Support. | No | 0 |
| 2:1 | BAR2 Type | RW | 00b: BAR2 is implemented as a 32 bit Memory BAR 10b: BAR2/3 is implemented as a 64-bit Memory BAR | Yes | 00b |
| 3 | Prefetchable | RW | 0b: Non Prefetchable 1b: Prefetchable | Yes | 0 |
| 19:4 | Reserved | RsvdP | Not Support. | No | 0_000h |
| 30:20 | BAR2 Size | RW | To specify BAR2 size. 0b: Corresponding BAR2 bits are RO bits that always return 0 1b: Corresponding BAR2 bits are RW bits | Yes | 0-0h |
| 31 | BAR 2 Enable | RW | Valid when bits[2:1]=00b. 0b: Disable BAR2 1b: Enable BAR2 | Yes | 0 |
| | BAR 2 Size | RW | Includes with bits[30:20] when tis BAR is used as a 64-bit BAR (bits[2:1]=10b). | | |

8.3.46 NT PORT LINK INTERFACE BAR 2-3 CONFIGURATION REGISTER – OFFSET Ech

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------|-------|----------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | Type Selector | RsvdP | Not Support. | No | 0 |
| 2:1 | BAR3 Type | RO | 00b: BAR3 is implemented as a 32-bit Memory BAR. | No | 00b |
| 3 | Prefetchable | RW | 0b: Non Prefetchable 1b: Prefetchable | Yes | 0 |
| 19:4 | Upper 32 Bits | RsvdP | Not Support when E8h[2:1]=00b. | No | 0_000h |
| | | RW | When E8h[2:1]=10b, BAR2/3 are used as a 64-bit BAR, bit[31:0] (including bit[19:4]) are used as the upper 32-bits. | Yes | 0_000h |
| 30:20 | BAR3 Size | RW | To specify BAR3 size. 0b: Corresponding BAR3 bits are RO bits that always return 0 1b: Corresponding BAR3 bits are RW bits | Yes | 000h |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|--------------|------|-----------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 31 | BAR 3 Enable | RW | Valid when E8h[2:1]=00b. 0b: Disable BAR3 1b: Enable BAR3 | Yes | 0 |
| | 64-Bit BAR | RW | Valid when E8h[2:1]=10b. 0b: BAR2/3 is disabled, all BAR2/3 bits read 0. 1b: BAR2/3 is enabled as a 64-bit BAR. | | |

8.3.47 NT PORT LINK INTERFACE BAR 4 CONFIGURATION REGISTER – OFFSET F0h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------|-------|----------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | Type Selector | RsvdP | Not Support. | No | 0 |
| 2:1 | BAR4 Type | RW | 00b: BAR4 is implemented as a 32 bit Memory BAR 10b: BAR4/5 is implemented as a 64-bit Memory BAR | Yes | 00b |
| 3 | Prefetchable | RW | 0b: Non Prefetchable 1b: Prefetchable | Yes | 0 |
| 19:4 | Reserved | RsvdP | Not Support. | No | 0_000h |
| 30:20 | BAR4 Size | RW | To specify BAR4 size. 0b: Corresponding BAR4 bits are RO bits that always return 0 1b: Corresponding BAR4 bits are RW bits | Yes | 0-0h |
| 31 | BAR4 Enable | RW | Valid when bis[2:1]=00b. 0b: Disable BAR4 1b: Enable BAR4 | Yes | 0 |
| | BAR 4 Size | RW | Includes with bits[30:20] when tis BAR is used as a 64-bit BAR (bits[2:1]=10b). | | |

8.3.48 NT PORT LINK INTERFACE BAR 4-5 CONFIGURATION REGISTER – OFFSET F4h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------|-------|----------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | Type Selector | RsvdP | Not Support. | No | 0 |
| 2:1 | BAR5 Type | RO | 00b: BAR5 is implemented as a 32-bit Memory BAR. | No | 00b |
| 3 | Prefetchable | RW | 0b: Non Prefetchable 1b: Prefetchable | Yes | 0 |
| 19:4 | Upper 32 Bits | RsvdP | Not Support when F0h[2:1]=00b. | No | 0_000h |
| | | RW | When F0h[2:1]=10b, BAR4/5 are used as a 64-bit BAR, bit[31:0] (including bit[19:4]) are used as the upper 32-bits. | Yes | 0_000h |
| 30:20 | BAR5 Size | RW | To specify BAR5 size. 0b: Corresponding BAR5 bits are RO bits that always return 0 1b: Corresponding BAR5 bits are RW bits | Yes | 000h |
| 31 | BAR 5 Enable | RW | Valid when F0h[2:1]=00b. 0b: Disable BAR5. 1b: Enable BAR5. | Yes | 0 |
| | 64-Bit BAR | RW | Valid when F0h[2:1]=10b. 0b: BAR4/5 is disabled, all BAR4/5 bits read 0. 1b: BAR4/5 is enabled as a 64-bit BAR. | | |

8.3.49 DEVICE SERIAL NUMBER ENHANCED CAPABILITY HEADER REGISTER – OFFSET 100h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------|------|-----------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 15:0 | Extended Capabilities ID | RO | Read as 0003h to indicate that these are PCI express extended capability registers for device serial number extend capability register. | No | 0003h |
| 19:16 | Capability Version | RO | Must be 1h for this version. | No | 1h |
| 31:20 | Next Capability Offset | RO | Indicates next capability pointer. | Yes | FB4h |

8.3.50 DEVICE SERIAL NUMBER LOWER DW REGISTER – OFFSET 104h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-----------------------------------------|------|---------------------------------------|----------------------|------------|
| 31:0 | Device serial number 1 st DW | RO | First dword for device serial number. | Yes | 0000_0000h |

8.3.51 DEVICE SERIAL NUMBER HIGHTER DW REGISTER – OFFSET 108h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-----------------------------------------|------|----------------------------------------|----------------------|------------|
| 31:0 | Device serial number 2 nd DW | RO | Second dword for device serial number. | Yes | 0000_0000h |

8.3.52 PCI EXPRESS POWER BUDGETING ENHANCED CAPABILITY HEADER REGISTER – OFFSET 138h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------|------|---------------------------------------------------------------------------------------------------------|----------------------|---------|
| 15:0 | Extended Capabilities ID | RO | Read as 0004h to indicate that these are PCI express extended capability registers for power budgeting. | No | 0004h |
| 19:16 | Capability Version | RO | Must be 1h for this version. | No | 01h |
| 31:20 | Next Capability Offset | RO | Indicates next capability pointer. | Yes | 148h |

8.3.53 DATA SELECT REGISTER – OFFSET 13Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|----------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 7:0 | Data Selection | RW | It indexes the power budgeting data reported through the data register. When 00h, it selects D0 Max power budget When 01h, it selects D0 Sustained power budget Other values would return zero power budgets, which means not supported. | No/Yes | 00h |
| 31:8 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.3.54 POWER BUDGETING DATA REGISTER – OFFSET 140h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------|-------|-------------------------------------------------------------------------------------------------------------------------------|----------------------|----------------------------------------|
| 7:0 | Base Power | RO | It specifies the base power value in watts. This value represents the required power budget in the given operation condition. | Yes | 04h if 13Ch[0]=0 03h if 13Ch[0]=1 |
| 9:8 | Data Scale | RO | It specifies the scale to apply to the base power value. | Yes | 00b |
| 12:10 | PM Sub State | RO | It specifies the power management sub state of the given operation condition. It is initialized to the default sub state. | No | 000b |
| 14:13 | PM State | RO | It specifies the power management state of the given operation condition. It defaults to the D0 power state. | Yes | 00b |
| 17:15 | Type | RO | It specifies the type of the given operation condition. It defaults to the Maximum power state. | No/Yes | 111b if 13Ch[0]=0 011b if 13Ch[0]=1 |
| 20:18 | Power Rail | RO | It specifies the power rail of the given operation condition.. | No | 010b |
| 31:21 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.3.55 POWER BUDGET CAPABILITY REGISTER – OFFSET 144h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|------------------|-------|---------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | System Allocated | RO | When set, it indicates that the power budget for the device is included within the system power budget. | Yes | 1 |
| 31:1 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.3.56 PCI EXPRESS VIRTUAL CHANNEL ENHANCED CAPABILITY HEADER REGISTER – OFFSET 148h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------|------|---------------------------------------------------------------------------------------------------------|----------------------|---------|
| 15:0 | Extended Capabilities ID | RO | Read as 0002h to indicate that these are PCI express extended capability registers for virtual channel. | No | 02h |
| 19:16 | Capability Version | RO | Read as 1h. | No | 01h |
| 31:20 | Next Capability Offset | RO | Read as 000h. No other ECP registers. | No | 000h |

8.3.57 PORT VC CAPABILITY REGISTER 1 – OFFSET 14Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 2:0 | Extended VC Count | RO | It indicates the number of extended Virtual Channels in addition to the default VC supported by the Switch. | Yes | 000b |
| 3 | Reserved | RsvdP | Not Support. | No | 0 |
| 6:4 | Low Priority Extended VC Count | RO | It indicates the number of extended Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group. | Yes | 000b |
| 7 | Reserved | RsvdP | Not Support. | No | 0 |
| 9:8 | Reference Clock | RO | It indicates the reference clock for Virtual Channels that support time-based WRR Port Arbitration. Defined encoding is 00b for 100 ns reference clock. | No | 00b |
| 11:10 | Port Arbitration Table Entry Size | RO | Read as 10b to indicate the size of Port Arbitration table entry in the device is 4 bits. | No | 10b |
| 31:12 | Reserved | RsvdP | Not Support. | No | 0000_0h |

8.3.58 PORT VC CAPABILITY REGISTER 2 – OFFSET 150h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|------------------------------|
| 7:0 | VC Arbitration Capability | RO | It indicates the types of VC Arbitration supported by the device for the LPVC group. This field is valid when LPVC is greater than 0. The Switch supports Hardware fixed arbitration scheme, e.g., Round Robin and Weight Round Robin arbitration with 32 phases in LPVC. | No | 03h |
| 23:8 | Reserved | RsvdP | Not Support. | No | 0000h |
| 31:24 | VC Arbitration Table Offset | RO | It indicates the location of the VC Arbitration Table as an offset from the base address of the Virtual Channel Capability register in the unit of DQWD (16 bytes). | No | 00h if VC1=0 04h if VC1=1 |

8.3.59 PORT VC CONTROL REGISTER – OFFSET 154h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|---------------------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | Load VC Arbitration Table | RW | When set, the programmed VC Arbitration Table is applied to the hardware. This bit always returns '0' when read. | Yes | 0 |
| 3:1 | VC Arbitration Select | RW | This field is used to configure the VC Arbitration by selecting one of the supported VC Arbitration schemes. The valid values for the schemes supported by Switch are 0b and 1b. Other value than these written into this register will be treated as default. | No/Yes | 000b |
| 15:4 | Reserved | RsvdP | Not Support. | No | 000h |

8.3.60 VC STATUS REGISTER – OFFSET 154h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 16 | VC Arbitration Table Status | RO | When set, it indicates that any entry of the VC Arbitration Table is written by software. This bit is cleared when hardware finishes loading values stored in the VC Arbitration Table after the bit of "Load VC Arbitration Table" is set. | No | 0 |
| 31:17 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.3.61 VC RESOURCE CAPABILITY REGISTER (0) – OFFSET 158h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-------------------------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|----------|
| 7:0 | Port Arbitration Capability | RO | It indicates the types of Port Arbitration supported by the VC resource. The Switch supports Hardware fixed arbitration scheme, e.g., Round Robin, Weight Round Robin (WRR) arbitration with 128 phases (3~4 enabled ports) and Time-based WRR with 128 phases (3~4 enabled ports). Note that the Time-based WRR is only valid in VC1. | No | 03h |
| 13:8 | Reserved | RsvdP | Not Support. | No | 00_0000h |
| 14 | Advanced Packet Switching | RO | When set, it indicates the VC resource only supports transaction optimized for Advanced Packet Switching (AS). | No | 0 |
| 15 | Reject Snoop Transactions | RO | This bit is not applied to PCIe Switch. | No | 0 |
| 22:16 | Maximum Time Slots | RO | It indicates the maximum numbers of time slots (minus one) are allocated for Isochronous traffic. | No | 3Fh |
| 23 | Reserved | RsvdP | Not Support. | No | 0 |
| 31:24 | Port Arbitration Table Offset | RO | It indicates the location of the Port Arbitration Table (n) as an offset from the base address of the Virtual Channel Capability register in the unit of DQWD (16 bytes). | No | 05h |

8.3.62 VC RESOURCE CONTROL REGISTER (0) – OFFSET 15Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------------------------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 7:0 | TC/VC Map | RW | This field indicates the TCs that are mapped to the VC resource. Bit locations within this field correspond to TC values. When the bits in this field are set, it means that the corresponding TCs are mapped to the VC resource. | Yes | FFh |
| 15:8 | Reserved | RsvdP | Not Support. | No | 00h |
| 16 | Load Port Arbitration Table | RW | When set, the programmed Port Arbitration Table is applied to the hardware. This bit always returns 0b when read. | No/Yes | 0 |
| 19:17 | Port Arbitration Select | RW | This field is used to configure the Port Arbitration by selecting one of the supported Port Arbitration schemes. The permissible values for the schemes supported by Switch are 000b and 011b at VC0, other value than these written into this register will be treated as default. | No/Yes | 000b |
| 23:20 | Reserved | RsvdP | Not Support. | No | 0h |
| 26:24 | VC ID | RO | This field assigns a VC ID to the VC resource. | No | 000b |
| 30:27 | Reserved | RsvdP | Not Support. | No | 0h |
| 31 | VC Enable | RO | 0b: it disables this Virtual Channel 1b: it enables this Virtual Channel | No | 1 |

8.3.63 VC RESOURCE STATUS REGISTER (0) – OFFSET 160h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-------------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 15:0 | Reserved | RsvdP | Not Support. | No | 0000h |
| 16 | Port Arbitration Table Status | RO | When set, it indicates that any entry of the Port Arbitration Table is written by software. This bit is cleared when hardware finishes loading values stored in the Port Arbitration Table after the bit of “Load Port Arbitration Table” is set. | No | 0 |
| 17 | VC Negotiation Pending | RO | When set, it indicates that the VC resource is still in the process of negotiation. This bit is cleared after the VC negotiation is complete. | No | 0 |
| 31:18 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.3.64 VC RESOURCE CAPABILITY REGISTER (1) – OFFSET 164h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-------------------------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|------------------------------|
| 7:0 | Port Arbitration Capability | RO | It indicates the types of Port Arbitration supported by the VC resource. The Switch supports Hardware fixed arbitration scheme, e.g., Round Robin, Weight Round Robin (WRR) arbitration with 128 phases (3~4 enabled ports) and Time-based WRR with 128 phases (3~4 enabled ports). Note that the Time-based WRR is only valid in VC1. | No | 00h if VC1=0 13h if VC1=1 |
| 13:8 | Reserved | RsvdP | Not Support. | No | 0-0h |
| 14 | Advanced Packet Switching | RO | When set, it indicates the VC resource only supports transaction optimized for Advanced Packet Switching (AS). | No | 0 |
| 15 | Reject Snoop Transactions | RO | This bit is not applied to PCIe Switch. | No | 0 |
| 22:16 | Maximum Time Slots | RO | It indicates the maximum numbers of time slots (minus one) are allocated for Isochronous traffic. | Yes | 00h if VC1=0 3Fh if VC1=1 |
| 23 | Reserved | RsvdP | Not Support. | No | 0 |
| 31:24 | Port Arbitration Table Offset | RO | It indicates the location of the Port Arbitration Table (n) as an offset from the base address of the Virtual Channel Capability register in the unit of DQWD (16 bytes). | No | 00h if VC1=0 06h if VC1=1 |

8.3.65 VC RESOURCE CONTROL REGISTER (1) – OFFSET 168h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------------------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|--------------------------------|
| 7:0 | TC/VC Map | RW | This field indicates the TCs that are mapped to the VC resource. Bit locations within this field correspond to TC values. When the bits in this field are set, it means that the corresponding TCs are mapped to the VC resource. Bit 0 of this field is read-only and must be set to “0” for the VC1. | Yes | 00h |
| 15:8 | Reserved | RsvdP | Not Support. | No | 0-0h |
| 16 | Load Port Arbitration Table | RW | When set, the programmed Port Arbitration Table is applied to the hardware. This bit always returns 0b when read. | No/Yes | 0 |
| 19:17 | Port Arbitration Select | RW | This field is used to configure the Port Arbitration by selecting one of the supported Port Arbitration schemes. The permissible values for the schemes supported by Switch are 000b, 011b and 100b at VC1, other value than these written into this register will be treated as default. | No/Yes | 000b |
| 23:20 | Reserved | RsvdP | Not Support. | No | 0h |
| 26:24 | VC ID | RW | This field assigns a VC ID to the VC resource. | No/Yes | 000b if VC1=0 001b if VC1=1 |
| 30:27 | Reserved | RsvdP | Not Support. | No | 0h |
| 31 | VC Enable | RW | 0b: it disables this Virtual Channel 1b: it enables this Virtual Channel | No/Yes | 0 |

8.3.66 VC RESOURCE STATUS REGISTER (1) – OFFSET 16Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-------------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 15:0 | Reserved | RsvdP | Not Support. | No | 0000h |
| 16 | Port Arbitration Table Status | RO | When set, it indicates that any entry of the Port Arbitration Table is written by software. This bit is cleared when hardware finishes loading values stored in the Port Arbitration Table after the bit of “Load Port Arbitration Table” is set. | No | 0 |
| 17 | VC Negotiation Pending | RO | When set, it indicates that the VC resource is still in the process of negotiation. This bit is cleared after the VC negotiation is complete. | No | 0 |
| 31:18 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.3.67 VC ARBITRATION TABLE REGISTER – OFFSET 188h

The VC arbitration table is a read-write register array that contains a table for VC arbitration. Each table entry allocates four bits, of which three bits are used to represent VC ID and one bit is reserved. A total of 32 entries are used to construct the VC arbitration table. The layout for this register array is shown below.

Table 8-4 Register Array Layout for VC Arbitration

| 31 - 28 | 27 - 24 | 23 - 20 | 19 - 16 | 15 - 12 | 11 - 8 | 7 - 4 | 3 - 0 | Byte Location | EEPROM/ I2C-SMBUS | DEFAULT |
|------------|------------|------------|------------|------------|------------|------------|------------|---------------|----------------------|------------|
| Phase [7] | Phase [6] | Phase [5] | Phase [4] | Phase [3] | Phase [2] | Phase [1] | Phase [0] | 00h | No/Yes | 0000_0000h |
| Phase [15] | Phase [14] | Phase [13] | Phase [12] | Phase [11] | Phase [10] | Phase [9] | Phase [8] | 04h | No/Yes | 0000_0000h |
| Phase [23] | Phase [22] | Phase [21] | Phase [20] | Phase [19] | Phase [18] | Phase [17] | Phase [16] | 08h | No/Yes | 0000_0000h |
| Phase [31] | Phase [30] | Phase [29] | Phase [28] | Phase [27] | Phase [26] | Phase [25] | Phase [24] | 0Ch | No/Yes | 0000_0000h |

8.3.68 PORT ARBITRATION TABLE REGISTER (0) and (1) – OFFSET 198h and 1A8h

The Port arbitration table is a read-write register array that contains a table for Port arbitration. Each table entry allocates two bits to represent Port Number. The table entry size is dependent on the number of enabled ports (refer to bit 10 and 11 of Port VC capability register 1). The arbitration table contains 32 entries if three or four ports are to be enabled. The following table shows the register array layout for the size of entry equal to two.

Table 8-5 Table Entry Size in 4 Bits

| 31 - 24 | 23 - 16 | 15 - 8 | 7 - 0 | Byte Location | EEPROM/I2C-SMBUS | DEFAULT |
|---------------|---------------|---------------|---------------|---------------|------------------|------------|
| Phase [7:6] | Phase [5:4] | Phase [3:2] | Phase [1:0] | 00h | No/Yes | 0000_0000h |
| Phase [15:14] | Phase [13:12] | Phase [11:10] | Phase [9:8] | 04h | No/Yes | 0000_0000h |
| Phase [23:22] | Phase [21:20] | Phase [19:18] | Phase [17:16] | 08h | No/Yes | 0000_0000h |
| Phase [31:30] | Phase [29:28] | Phase [27:26] | Phase [25:24] | 0Ch | No/Yes | 0000_0000h |

8.3.69 XPIP_CSR 0 REGISTER – OFFSET 844h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/I2C-SMBUS | DEFAULT |
|------|-----------|------|--------------------------------------------------------------------------------------------|------------------|------------|
| 31:0 | XPIP_CSR0 | RW | XPIP CSR 0 value. Bit[2]: Cross_Link_En. These bits always return '0' when read. | Yes | 0400_1060h |

8.3.70 XPIP_CSR 1 REGISTER – OFFSET 848h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/I2C-SMBUS | DEFAULT |
|------|-----------|------|------------------------------------------------------------------|------------------|------------|
| 31:0 | XPIP_CSR1 | RW | XPIP CSR 1 value. These bits always return '0' when read. | Yes | 0400_0800h |

8.3.71 DECODE VGA REGISTER – OFFSET 84Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/I2C-SMBUS | DEFAULT |
|------|-------------------|-------|-----------------------------------------------------------------------------------------------|------------------|---------|
| 30:0 | Reserved | RsvdP | Not Support. | No | 0-0h |
| 31 | Decode VGA Enable | RO | 0b: Disable VGA decode 1b: Enable VGA decode This bit always returns '0' when read. | Yes | 1 |

8.3.72 XPIP_CSR 2 REGISTER – OFFSET 854h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/I2C-SMBUS | DEFAULT |
|-----|-------------------|------|-----------------------------------------|------------------|---------|
| 7:0 | FTS Number | RW | These bits always return '0' when read. | Yes | 80h |
| 9:8 | Scrambler Control | RW | These bits always return '0' when read. | Yes | 00b |
| 10 | L0s | RW | This bit always returns '0' when read. | Yes | 0 |
| 11 | Compliance to | RW | This bit always returns '0' when read. | Yes | 0 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|------------------|-------|-----------------------------------------|----------------------|---------|
| | Detect | | | | |
| 13:12 | Change Speed Sel | RW | These bits always return '0' when read. | Yes | 00b |
| 14 | Change Speed En | RW | This bit always returns '0' when read. | Yes | 0 |
| 31:15 | Reserved | RsvdP | Not Support. | No | 0 0000h |

8.3.73 PHY PARAMETER 2 REGISTER – OFFSET 858h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|------------------------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 7:0 | Reserved | RsvdP | Not Support. | No | 27h |
| 8 | P_CDR_FREQLOO P_EN | RW | This bit always returns '0' when read. | Yes | 1 |
| 10:9 | P_CDR_ THRESHOLD | RW | These bits always return '0' when read. | Yes | 10b |
| 12:11 | P_CDR_FREQLOO P_GAIN | RW | These bits always return '0' when read. | Yes | 11b |
| 15:13 | Reserved | RsvdP | Not Support. | No | 000b |
| 16 | P_DRV_LVL_MGN DELATA EN | RW | This bit always returns '0' when read. | Yes | 0 |
| 17 | P_DRV_LVL_NOM DELATA EN | RW | This bit always returns '0' when read. | Yes | 0 |
| 18 | P_EMP_POST_MG N_DELATA EN | RW | This bit always returns '0' when read. | Yes | 0 |
| 19 | P_EMP_POST_NO M_DELATA EN | RW | This bit always returns '0' when read. | Yes | 0 |
| 21:20 | P_RX_SIGDET_ LVL | RW | Set the receiver signal detection threshold. Please refer to Section 6.1.2 for more detail information. These bits always return '0' when read. | Yes | 01b |
| 25:22 | P_RX_EQ_1 | RW | Set the receiver equalization for GEN1 link. Please refer to Section 6.1.3 for more detail information. These bits always return '0' when read. | Yes | 0h |
| 29:26 | P_RX_EQ_2 | RW | Set the receiver equalization for GEN2 link. Please refer to Section 6.1.3 for more detail information. These bits always return '0' when read. | Yes | 0h |
| 30 | P_TXSWING | RW | Set the transmitter swing. Please refer to Section 6.1.4 for more detail information. 0b: full voltage swing with de-emphasis 1b: half voltage swing without de-emphasis This bit always returns '0' when read. | Yes | 0 |
| 31 | Reserved | RsvdP | Not Support. | No | 0 |

8.3.74 PHY PARAMETER 3 REGISTER – OFFSET 85Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-------------------------------|-------|---------------------------------------------------------------------------|----------------------|---------|
| 6:0 | PHY Parameter 3 (Per Lane) | RW | PHY's Lane mode. These bits always return '0' when read. | Yes | 00h |
| 14:7 | Reserved | RsvdP | Not Support. | No | 00h |
| 31:15 | PHY Parameter 3 (Per Port) | RW | PHY's delta value setting. These bits always return '0' when read. | Yes | 0001h |

8.3.75 XPIP_CSR 3 REGISTER – OFFSET 864h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-----------|------|------------------------------------------------------------------|----------------------|------------|
| 31:0 | XPIP_CSR3 | RW | XPIP CSR 3 value. These bits always return '0' when read. | Yes | 000F_0000h |

8.3.76 XPIP_CSR 5 REGISTER – OFFSET 86Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-----------------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|------------|
| 29:0 | XPIP_CSR5[29:0] | RW | Bit[10]: Default ACK Latency Timer Enable 0b: disable default ack latency timer 1b: enable default ack latency timer These bits always return '0' when read. | Yes | 3308_0008h |
| 30 | DO_CHG_DATA_RATE_CTRL | RW | DO_CHG_DATA_RATE_CTRL. This bit always returns '0' when read. | Yes | 0 |
| 31 | Gen1_Cap_Only | RW | 0b: report GEN2 capability 1b: report GEN1 capability This bit always returns '0' when read. | Yes | 0 |

8.3.77 OPERATION MODE REGISTER – OFFSET 874h (Global)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | Operation Mode | HwInt RO | Bit[0]: Memory Bist Bit[1]: IDDRB Bit[2]: FAST_MODE Bit[3]: DEBUG_MODE Bit[4]: PHY_MODE Bit[8:5]: WORK_MODE Bit[9]: PLCSEL Bit[10]: SCAN_MODE Bit[15:11]: Reserved These bits always return '0' when read. | No | 0202h for 324 mode 0222h for 424 mode 0242h for 524 mode 0262h for 624 mode 0282h for 1124 mode 02A2h for 1224 mode |
| 31:16 | Reserved | RsvdP | Not Support. | No | 0000h |

8.3.78 MAC_CSR REGISTER – OFFSET 890h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------|-------|-----------------------------------------|----------------------|---------|
| 15:0 | Reserved | RsvdP | Not Support. | No | 0000h |
| 31:16 | MAC_CSR | RW | These bits always return '0' when read. | Yes | 0004h |

8.3.79 POWER SAVING DISABLE REGISTER – OFFSET 8A4h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|----------------------|------|---------------------------------------------------------------------|----------------------|---------|
| 0 | Power Saving Disable | RW | Disable power saving. This bit always returns '0' when read. | Yes | 0 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|----------|-------|--------------|----------------------|---------|
| 31:1 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.3.80 TRANSACTION LAYER CSR REGISTER – OFFSET 8A8h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-------------------------|-------|-----------------|----------------------|---------|
| 0 | Egress_Reqcredit_Starve | RW | Test used only. | Yes | 1 |
| 1 | MF_Credit_Update_Dis | RW | Test used only. | Yes | 0 |
| 2 | MC_Cap_Dis | RW | Test used only. | Yes | 0 |
| 3 | MEM_Sharing_Dis | RO | Test used only. | Yes | 0 |
| 31:4 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.3.81 REPLAY TIME-OUT COUNTER REGISTER – OFFSET 8ACh

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------|-------|-----------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 11:0 | User Replay Timer | RW | A 12-bit register contains a user-defined value. These bits always return '0' when read. | Yes | 000h |
| 12 | Enable User Replay Timer | RW | When asserted, the user-defined replay time-out value is be employed. This bit always returns '0' when read. | Yes | 0 |
| 15:13 | Reserved | RsvdP | Not Support. | No | 000b |

8.3.82 ACKNOWLEDGE LATENCY TIMER REGISTER – OFFSET 8ACh

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-------------------------|-------|-------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 29:16 | User ACK Latency Timer | RW | A 14-bit register contains a user-defined value. These bits always return '0' when read. | Yes | 0-0h |
| 30 | Enable User ACK Latency | RW | When asserted, the user-defined ACK latency value is be employed. This bit always returns '0' when read. | Yes | 0 |
| 31 | Reserved | RsvdP | Not Support. | No | 0 |

8.3.83 PORT MISC 0 REGISTER – OFFSET 8B0h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-------------------------------------------|-------|-----------------------------------------------------------------------------------------------|----------------------|----------|
| 7:0 | Reserved | RsvdP | Not Support. | No | 00h |
| 13:8 | Power Management Control Parameter | RW | Power Management Control parameter. | Yes | 00_0001b |
| 14 | RX Polarity Inversion Disable | RW | 0b: enable rx polarity inversion circuit 1b: disable rx polarity inversion circuit | Yes | 0 |
| 15 | Compliance Pattern Parity Control Disable | RW | 0b: enable compliance pattern parity control 1b: disable compliance pattern parity control | Yes | 0 |
| 31:16 | Reserved | RsvdP | Not Support | No | 0000h |

8.3.84 PORT MISC 1 REGISTER – OFFSET 8B4h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------------|-------|------------------------------------------------------------------------------------------|----------------------|---------|
| 7:0 | Reserved | RsvdP | Not Support. | No | 00h |
| 8:9 | DO_CHG_DATA_CNT_SEL | RW | The trying number for doing change data rate. These bits always return '0' when read. | Yes | 00b |
| 10 | Port Disable | RW | Disable this port. This bit always returns '0' when read. | Yes | 0 |
| 15:11 | Reserved | RsvdP | Not Support. | No | 0_0000b |

8.3.85 XPIP_CSR 6 REGISTER – OFFSET 8B4h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------|------|--------------------------------------------------------------|----------------------|---------|
| 23:16 | XPIP_CSR6 | RW | XPIP_CSR 6 Value. These bits always return '0' when read. | Yes | 78h |

8.3.86 XPIP_CSR 7 REGISTER – OFFSET 8B4h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------------------|------|------------------------------------------------------------|----------------------|---------|
| 25:24 | REV_TS_CTR | RW | Test used only. These bits always return '0' when read. | Yes | 00 |
| 29:26 | MAC Control Parameter | RW | Test used only. These bits always return '0' when read. | Yes | 0h |
| 30 | Line_Loopback | RW | Test used only. This bit always returns '0' when read. | No | 0 |
| 31 | P35_GEN2_MODE | RW | Test used only. This bit always returns '0' when read. | Yes | 0 |

8.3.87 PORT MISC 2 REGISTER – OFFSET 8B8h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|----------------|-------|-----------------------------------------------------------|----------------------|---------|
| 0 | Change_Role_En | RW | Test used only. This bit always returns '0' when read. | Yes | 0 |
| 1 | IPCore_Role | RW | Test used only. This bit always returns '0' when read. | Yes | 0 |
| 31:2 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.3.88 VENDOR SPECIFIC CAPABILITIES HEADER REGISTER – OFFSET C34h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------|------|-------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 15:0 | Extended Capabilities ID | RO | Read as 000Bh to indicate that these are PCI express extended capability registers for vendor specific registers. | No | 000Bh |
| 19:16 | Capability Version | RO | Read as 1h. | No | 1h |
| 31:20 | Next Capability Offset | RO | Read as 000h. No other ECP registers. | No | 000h |

8.3.89 VENDOR SPECIFIC HEADER REGISTER – OFFSET C38h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|------------------------|------|----------------------|----------------------|------------|
| 31:0 | Vendor Specific Header | RO | Reset to 0780_0003h. | No | 0780_0003h |

8.3.90 MEMORY BAR 2 ADDRESS TRANSLATION REGISTER – OFFSET C3Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------------------------|-------|-------------------------------------------------|----------------------|---------|
| 19:0 | Reserved | RsvdP | Not Support. | No | 0_0000h |
| 31:20 | Memory BAR 2 Address Translation | RW | Valid when BAR 2 is enabled (offset E8h[31]=1). | Yes | 000h |

8.3.91 MEMORY BAR 3 ADDRESS TRANSLATION REGISTER – OFFSET C40h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------------------------|-------|------------------------------------------|----------------------|---------|
| 19:0 | Reserved | RsvdP | Not Support. | No | 000h |
| 31:20 | Memory BAR 3 Address Translation | RW | Valid when BAR 3 is enabled (ECh[31]=1). | Yes | 000h |

8.3.92 MEMORY BAR4 ADDRESS TRANSLATION REGISTER – OFFSET C44h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------------------------|-------|-------------------------------------------------|----------------------|---------|
| 19:0 | Reserved | RsvdP | Not Support. | No | 0_0000h |
| 31:20 | Memory BAR 4 Address Translation | RW | Valid when BAR 4 is enabled (offset F0h[31]=1). | Yes | 000h |

8.3.93 MEMORY BAR 5 ADDRESS TRANSLATION REGISTER – OFFSET C48h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|----------------------------------|-------|------------------------------------------|----------------------|---------|
| 19:0 | Reserved | RsvdP | Not Support. | No | 000h |
| 31:0 | Memory BAR 5 Address Translation | RW | Valid when BAR 5 is enabled (F4h[31]=1). | Yes | 000h |

8.3.94 VIRTUAL IF IRQ SET REGISTER – OFFSET C4Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------|-------|----------------------------|----------------------|---------|
| 15:0 | Set IRQ | RW | Set virtual interface IRQ. | No/Yes | 0000h |
| 31:16 | Reserved | RsvdP | Not Support. | No | 0000h |

8.3.95 VIRTUAL IF IRQ CLEAR REGISTER – OFFSET C50h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------|-------|------------------------------|----------------------|---------|
| 15:0 | Clear IRQ | RW1C | Clear virtual interface IRQ. | No/Yes | 0000h |
| 31:16 | Reserved | RsvdP | Not Support. | No | 0000h |

8.3.96 VIRTUAL IF IRQ MASK SET REGISTER – OFFSET C54h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------|-------|-------------------------------------------|----------------------|---------|
| 15:0 | Set IRQ Mask | RW | Set virtual interface interrupt IRQ mask. | No/Yes | FFFFh |
| 31:16 | Reserved | RsvdP | Not Support. | No | 0000h |

8.3.97 VIRTUAL IF IRQ MASK CLEAR REGISTER – OFFSET C58h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------|-------|---------------------------------------------|----------------------|---------|
| 15:0 | Clear IRQ Mask | RW1C | Clear virtual interface interrupt IRQ mask. | No/Yes | 0000h |
| 31:16 | Reserved | RsvdP | Not Support. | No | 0000h |

8.3.98 LINK IF IRQ SET REGISTER – OFFSET C5Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------|-------|-------------------------|----------------------|---------|
| 15:0 | Set IRQ | RW | Set link interface IRQ. | No/Yes | 0000h |
| 31:16 | Reserved | RsvdP | Not Support. | No | 0000h |

8.3.99 LINK IF IRQ CLEAR REGISTER – OFFSET C60h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------|-------|---------------------------|----------------------|---------|
| 15:0 | Clear IRQ | RW1C | Clear link interface IRQ. | No/Yes | 0000h |
| 31:16 | Reserved | RsvdP | Not Support. | No | 0000h |

8.3.100 LINK IF IRQ MASK SET REGISTER – OFFST C64h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------|-------|----------------------------------------|----------------------|---------|
| 15:0 | Set IRQ Mask | RW | Set link interface interrupt IRQ mask. | No/Yes | FFFFh |
| 31:16 | Reserved | RsvdP | Not Support. | No | 0000h |

8.3.101 LINK IF IRQ MASK CLEAR REGISTER – OFFSET C68h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------|-------|------------------------------------------|----------------------|---------|
| 15:0 | Clear IRQ Mask | RW1C | Clear link interface interrupt IRQ mask. | No/Yes | 0000h |
| 31:16 | Reserved | RsvdP | Not Support. | No | 0000h |

8.3.102 SCRATCHPAD 0 REGISTER – OFFSET C6Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|--------------|------|------------------------|----------------------|------------|
| 31:0 | Scratchpad 0 | RW | Scratchpad 0 register. | No/Yes | 0000_0000h |

8.3.103 SCRATCHPAD 1 REGISTER – OFFSET C70h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|--------------|------|------------------------|----------------------|------------|
| 31:0 | Scratchpad 1 | RW | Scratchpad 1 register. | No/Yes | 0000_0000h |

8.3.104 SCRATHPAD 2 REGISTER – OFFSET C74h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|--------------|------|------------------------|----------------------|------------|
| 31:0 | Scratchpad 2 | RW | Scratchpad 2 register. | No/Yes | 0000_0000h |

8.3.105 SCRATCHPAD 3 REGISTER – OFFSET C78h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|--------------|------|------------------------|----------------------|------------|
| 31:0 | Scratchpad 3 | RW | Scratchpad 3 register. | No/Yes | 0000_0000h |

8.3.106 SCRATHPAD 4 REGISTER – OFFSET C7Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|--------------|------|------------------------|----------------------|------------|
| 31:0 | Scratchpad 4 | RW | Scratchpad 4 register. | No/Yes | 0000_0000h |

8.3.107 SCRATCHPAD 5 REGISTER – OFFSET C80h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|--------------|------|------------------------|----------------------|------------|
| 31:0 | Scratchpad 5 | RW | Scratchpad 5 register. | No/Yes | 0000_0000h |

8.3.108 SCRATCHPAD 6 REGISTER – OFFSET C84h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|--------------|------|------------------------|----------------------|------------|
| 31:0 | Scratchpad 6 | RW | Scratchpad 6 register. | No/Yes | 0000_0000h |

8.3.109 SCRATCHPAD 7 REGISTER – OFFSTE C88h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|--------------|------|------------------------|----------------------|------------|
| 31:0 | Scratchpad 8 | RW | Scratchpad 8 register. | No/Yes | 0000_0000h |

8.3.110 VIRTUAL PORT 32-BITS LTT ENTRY 0-7 – OFFSET D94h to DB0h

Table 8-6 Virtual Port 32-Bits LTT Entry 0-7 Register Locations

| CFG OFFSET | LTT Entry_n | CFG OFFSET | LTT Entry_n |
|------------|-------------|------------|-------------|
| D94h | 0 | DA4h | 4 |
| D98h | 1 | DA8h | 5 |
| D9Ch | 2 | DAC h | 6 |
| DA0h | 3 | DB0h | 7 |

Table 8-7 Virtual Port 32-Bits LTT Entry_n (n=0 through 7)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------------------------|-------|-------------------------------------------------------------------------------|----------------------|---------|
| 15:0 | ReqID | RW | Bit[2:0]: function number Bit[7:3]: device number Bit[15:8]: bus number | No/Yes | 0000h |
| 29:16 | Reserved | RsvdP | Not Support. | No | 0-0h |
| 30 | LUT Entry_n_ No Snoop Enable | RsvdP | Not Support. | No | 0 |
| 31 | LUT Entry_n Enable | RW | 0b: disable 1b: enable | No/Yes | 0 |

8.3.111 LINK PORT 16-BITS LTT ENTRY 0-31 REGISTER – OFFSET DB4h – DF4h

Table 8-8 Link Port 16-Bits LTT Entry 0-31 Register Locations

| CFG OFFSET | LTT Entry_n | CFG OFFSET | LTT Entry_n |
|------------|-------------|------------|-------------|
| DB4h | 0-1 | DD4h | 16-17 |
| DB8h | 2-3 | DD8h | 18-19 |
| DBCh | 4-5 | DDCh | 20-21 |
| DC0h | 6-7 | DE0h | 22-23 |
| DC4h | 8-9 | DE4h | 24-25 |
| DC8h | 10-11 | DE8h | 26-27 |
| DCCh | 12-13 | DECh | 28-29 |
| DD0h | 14-15 | DF0h | 30-31 |

Table 8-9 Link Port 16-Bits LTT Entry_n_m (n_m 0-1 to 30-31)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------------------------|-------|-------------------------------------------------|----------------------|---------|
| 0 | LUT Entry_n Enable | RW | 0b: disable 1b: enable | No/Yes | 0 |
| 1 | LUT Entry_n No Snoop Enable | RsvdP | Not Support. | No | 0 |
| 2 | Reserved | RsvdP | Not Support. | No | 0 |
| 15:3 | ReqID | RW | Bit[7:3]: device number Bit[15:8]: device id | No/Yes | 00h |
| 16 | LUT Entry_m Enable | RW | 0b: disable 1b: enable | No/Yes | 0 |
| 17 | LUT Entry_m No Snoop Enable | RW | 0b: disable 1b: enable | No/Yes | 0 |
| 18 | Reserved | RsvdP | Not Support. | No | 0 |
| 31:19 | ReqID | RW | Bit[7:3]: device number Bit[15:8]: device id | No/Yes | 00h |

8.3.112 FAIL-OVER CSR REGISTER – OFFSET DF4h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|--------------------|-------|-----------------|----------------------|---------|
| 0 | Pri Linksdwn Force | RW | Test used only. | Yes | 0 |
| 1 | 2nd Linksdwn Force | RW | Test used only. | Yes | 0 |
| 2 | Failover Enable | RW | Test used only. | Yes | 0 |
| 3 | Disable Hot Reset | RW | Test used only. | Yes | 0 |
| 31:4 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.3.113 EEPROM_SCRATCHPAD REGISTER – OFFSET FB0h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-------------------|------|-----------------|----------------------|------------|
| 31:0 | EEPROM_Scratchpad | RO | Test used only. | Yes | 0000_0000h |

8.3.114 PCI EXPRESS ADVANCED ERROR REPORTING ENHANCED CAPABILITY HEADER REGISTER – OFFSET FB4h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------|------|-----------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 15:0 | Extended Capabilities ID | RO | Read as 0001h to indicate that these are PCI express extended capability registers for advance error reporting. | No | 0001h |
| 19:16 | Capability Version | RO | Read as 1h. | No | 1h |
| 31:20 | Next Capability Offset | RO | Indicates next capability pointer. | No/Yes | 138h |

8.3.115 UNCORRECTABLE ERROR STATUS REGISTER – OFFSET FB8h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|---------------------------------|-------|---------------------------------------------------------------------------|----------------------|---------|
| 0 | Training Error Status | RW1C | When set, indicates that the Training Error event has occurred. | No/Yes | 0 |
| 3:1 | Reserved | RsvdP | Not Support. | No | 000 |
| 4 | Data Link Protocol Error Status | RW1C | When set, indicates that the Data Link Protocol Error event has occurred. | No/Yes | 0 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|------------------------------------|-------|------------------------------------------------------------------------------|----------------------|---------|
| 11:5 | Reserved | RsvdP | Not Support. | No | 0-0b |
| 12 | Poisoned TLP Status | RW1C | When set, indicates that a Poisoned TLP has been received or generated. | No/Yes | 0 |
| 13 | Flow Control Protocol Error Status | RW1C | When set, indicates that the Flow Control Protocol Error event has occurred. | No/Yes | 0 |
| 14 | Completion Timeout Status | RW1C | When set, indicates that the Completion Timeout event has occurred. | No/Yes | 0 |
| 15 | Completer Abort Status | RW1C | When set, indicates that the Completer Abort event has occurred. | No/Yes | 0 |
| 16 | Unexpected Completion Status | RW1C | When set, indicates that the Unexpected Completion event has occurred. | No/Yes | 0 |
| 17 | Receiver Overflow Status | RW1C | When set, indicates that the Receiver Overflow event has occurred. | No/Yes | 0 |
| 18 | Malformed TLP Status | RW1C | When set, indicates that a Malformed TLP has been received. | No/Yes | 0 |
| 19 | ECRC Error Status | RW1C | When set, indicates that an ECRC Error has been detected. | No/Yes | 0 |
| 20 | Unsupported Request Error Status | RW1C | When set, indicates that an Unsupported Request event has occurred. | No/Yes | 0 |
| 21 | ACS Violation Status | RW1C | When set, indicates that an ACS Violation event has occurred | No/Yes | 0 |
| 22 | Reserved | RsvdP | Not Support. | No | 0 |
| 23 | MC Blocked TLP Status | RW1C | When set, indicates that an MC Blocked TLP event has occurred. | No/Yes | 0 |
| 31:24 | Reserved | RsvdP | Not Support. | No | 00h |

8.3.116 UNCORRECTABLE ERROR MASK REGISTER – OFFSET FBCh

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------------------------|-------|-------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | Training Error Mask | RW | When set, the Training Error event is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 3:1 | Reserved | RsvdP | Not Support. | No | 000b |
| 4 | Data Link Protocol Error Mask | RW | When set, the Data Link Protocol Error event is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 11:5 | Reserved | RsvdP | Not Support. | No | 0-0b |
| 12 | Poisoned TLP Mask | RW | When set, an event of Poisoned TLP is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 13 | Flow Control Protocol Error Mask | RW | When set, the Flow Control Protocol Error event is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 14 | Completion Timeout Mask | RW | When set, the Completion Timeout event is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 15 | Completer Abort Mask | RW | When set, the Completer Abort event is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 16 | Unexpected Completion Mask | RW | When set, the Unexpected Completion event is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 17 | Receiver Overflow Mask | RW | When set, the Receiver Overflow event is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 18 | Malformed TLP Mask | RW | When set, an event of Malformed TLP is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 19 | ECRC Error Mask | RW | When set, an event of ECRC Error is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 20 | Unsupported Request Error Mask | RW | When set, the Unsupported Request event is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 21 | ACS Violation Mask | RW | When set, the ACS Violation event is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 22 | Reserved | RsvdP | Not Support. | No | 0 |
| 23 | MC Blocked TLP Mask | RW1C | When set, the MC Blocked TLP event is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 31:24 | Reserved | RsvdP | Not Support. | No | 00h |

8.3.117 UNCORRECTABLE ERROR SEVERITY REGISTER – OFFSET FC0h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------------------|-------|----------------------------|----------------------|---------|
| 0 | Training Error Severity | RW | 0b: Non-Fatal 1b: Fatal | No/Yes | 1 |
| 3:1 | Reserved | RsvdP | Not Support. | No | 000b |
| 4 | Data Link Protocol Error Severity | RW | 0b: Non-Fatal 1b: Fatal | No/Yes | 1 |
| 11:5 | Reserved | RsvdP | Not Support. | No | 0-0b |
| 12 | Poisoned TLP Severity | RW | 0b: Non-Fatal 1b: Fatal | No/Yes | 0 |
| 13 | Flow Control Protocol Error Severity | RW | 0b: Non-Fatal 1b: Fatal | No/Yes | 1 |
| 14 | Completion Timeout Error Severity | RW | 0b: Non-Fatal 1b: Fatal | No/Yes | 0 |
| 15 | Completer Abort Severity | RW | 0b: Non-Fatal 1b: Fatal | No/Yes | 0 |
| 16 | Unexpected Completion Severity | RW | 0b: Non-Fatal 1b: Fatal | No/Yes | 0 |
| 17 | Receiver Overflow Severity | RW | 0b: Non-Fatal 1b: Fatal | No/Yes | 1 |
| 18 | Malformed TLP Severity | RW | 0b: Non-Fatal 1b: Fatal | No/Yes | 1 |
| 19 | ECRC Error Severity | RW | 0b: Non-Fatal 1b: Fatal | No/Yes | 0 |
| 20 | Unsupported Request Error Severity | RW | 0b: Non-Fatal 1b: Fatal | No/Yes | 0 |
| 21 | ACS Violation Severity | RW | 0b: Non-Fatal 1b: Fatal | No/Yes | 0 |
| 22 | Reserved | RsvdP | Not Support. | No | 0 |
| 23 | MC Blocked TLP Severity | RW | 0b: Not-Fatal 1b: Fatal | No/Yes | 0 |
| 31:24 | Reserved | RsvdP | Not Support. | No | 00h |

8.3.118 CORRECTABLE ERROR STATUS REGISTER – OFFSET FC4 h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------------------------|-------|----------------------------------------------------------------|----------------------|---------|
| 0 | Receiver Error Status | RW1C | When set, the Receiver Error event is detected. | No/Yes | 0 |
| 5:1 | Reserved | RsvdP | Not Support. | No | 0 000b |
| 6 | Bad TLP Status | RW1C | When set, the event of Bad TLP has been received is detected. | No/Yes | 0 |
| 7 | Bad DLLP Status | RW1C | When set, the event of Bad DLLP has been received is detected. | No/Yes | 0 |
| 8 | REPLAY_NUM Rollover status | RW1C | When set, the REPLAY_NUM Rollover event is detected. | No/Yes | 0 |
| 11:9 | Reserved | RsvdP | Not Support. | No | 000b |
| 12 | Replay Timer Timeout status | RW1C | When set, the Replay Timer Timeout event is detected. | No/Yes | 0 |
| 13 | Advisory Non-Fatal Error status | RW1C | When set, the Advisory Non-Fatal Error event is detected. | No/Yes | 0 |
| 31:14 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.3.119 CORRECTABLE ERROR MASK REGISTER – OFFSET FC8 h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-------------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | Receiver Error Mask | RW | When set, the Receiver Error event is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 5:1 | Reserved | RsvdP | Not Support. | No | 0_000b |
| 6 | Bad TLP Mask | RW | When set, the event of Bad TLP has been received is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 7 | Bad DLLP Mask | RW | When set, the event of Bad DLLP has been received is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 8 | REPLAY_NUM Rollover Mask | RW | When set, the REPLAY_NUM Rollover event is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 11:9 | Reserved | RsvdP | Not Support. | No | 000b |
| 12 | Replay Timer Timeout Mask | RW | When set, the Replay Timer Timeout event is not logged in the Header Log register and not issued as an Error Message to RC either. | No/Yes | 0 |
| 13 | Advisory Non-Fatal Error Mask | RW | When set, the Advisory Non-Fatal Error event is not logged in the Header Long register and not issued as an Error Message to RC either. | No/Yes | 1 |
| 31:14 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.3.120 ADVANCE ERROR CAPABILITIES AND CONTROL REGISTER – OFFSET FCCh

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-------------------------|-------|-----------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 4:0 | First Error Pointer | RO | It indicates the bit position of the first error reported in the Uncorrectable Error Status register. Reset to 5'd0. | No | 0_0000b |
| 5 | ECRC Generation Capable | RO | When set, it indicates the Switch has the capability to generate ECRC. | No | 1 |
| 6 | ECRC Generation Enable | RW | When set, it enables the generation of ECRC when needed. | No/Yes | 0 |
| 7 | ECRC Check Capable | RO | When set, it indicates the Switch has the capability to check ECRC. | No | 1 |
| 8 | ECRC Check Enable | RW | When set, the function of checking ECRC is enabled.. | No/Yes | 0 |
| 31:9 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.3.121 HEADER LOG REGISTER – OFFSET From FD0h to FDCh

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|--------|-----------------------|------|-------------------------------------------------------------------|----------------------|------------|
| 31:0 | 1 st DWORD | RO | Hold the 1st DWORD of TLP Header. The Head byte is in big endian. | No | 0000-0000h |
| 63:32 | 2 nd DWORD | RO | Hold the 2nd DWORD of TLP Header. The Head byte is in big endian. | No | 0000-0000h |
| 95:64 | 3 rd DWORD | RO | Hold the 3rd DWORD of TLP Header. The Head byte is in big endian. | No | 0000-0000h |
| 127:96 | 4 th DWORD | RO | Hold the 4th DWORD of TLP Header. The Head byte is in big endian. | No | 0000-0000h |

8.4 NON TRANSPARENT PORT VIRTUAL INTERFACE CONFIGURATION REGISTERS – NT Mode Only

When the port of the Switch is set to operate at the non-transparent mode, it is represented by an Other Bridge that implements type 0 configuration space header. The following table details the allocation of the register fields of the PCI 2.3 compatible type 0 configuration space header.

| 31 – 24 | 23 – 16 | 15 – 8 | 7 – 0 | BYTE OFFSET |
|-------------------------------------------------|------------------------|-----------------------|--------------------------------------|-------------|
| Device ID | | Vendor ID | | 00h |
| Primary Status | | Command | | 04h |
| Class Code | | | Revision ID | 08h |
| Reserved | Header Type | Reserved | Cache Line Size | 0Ch |
| BAR 0 | | | | 10h |
| BAR 1 | | | | 14h |
| BAR 2 | | | | 18h |
| BAR 3 | | | | 1Ch |
| BAR 4 | | | | 20h |
| BAR 5 | | | | 24h |
| Reserved | | | | 28h |
| SSID | | SSVID | | 2Ch |
| Reserved | | | | 30h |
| Reserved | | | Capability Pointer to 40h | 34h |
| Reserved | | | | 38h |
| Reserved | | Interrupt Pin | Interrupt Line | 3Ch |
| Power Management Capabilities | | Next Item Pointer=48h | Capability ID=01h | 40h |
| PM Data | PPB Support Extensions | Power Management Data | | 44h |
| Message Control | | Next Item Pointer=68h | Capability ID=05h | 48h |
| Message Address | | | | 4Ch |
| Message Upper Address | | | | 50h |
| Reserved | | Message Data | | 54h |
| Reserved | | | | 58h – 64h |
| PCI Express Capabilities Register | | Next Item Pointer=A4h | Capability ID=10h | 68h |
| Device Capabilities | | | | 6Ch |
| Device Status | | Device Control | | 70h |
| Link Capabilities | | | | 74h |
| Link Status | | Link Control | | 78h |
| Reserved | | | | 7Ch - 90h |
| Link Capabilities 2 | | | | 94h |
| Link Status 2 | | Link Control 2 | | 98h |
| Reserved | | | | 9Ch – A0h |
| Reserved | | Next Item Pointer=C8h | SSID/SSVID Capability ID=0Dh | A4h |
| SSID | | SSVID | | A8h |
| Reserved | | | | ACh – C4h |
| Length | | Next Item Pointer=00h | Vendor Specific Capability ID=09h | C8h |
| Reserved | | | | CCh |
| NT Port Virtual Interface BAR 0-1 Configuration | | | | D0h |
| NT Port Virtual Interface BAR 2 Configuration | | | | D4h |
| NT Port Virtual Interface BAR 2-3 Configuration | | | | D8h |
| NT Port Virtual Interface BAR 4 Configuration | | | | DCh |
| NT Port Virtual Interface BAR 4-5 Configuration | | | | E0h |
| Reserved | | | | E4h - FCh |

Other than the PCI 2.3 compatible configuration space header, the Switch also implements PCI express extended configuration space header, which includes advanced error reporting, virtual channel, and power budgeting capability registers. The following table details the allocation of the register fields of PCI express extended capability space header. The first extended capability always begins at offset 100h with a PCI Express Enhanced Capability header and the rest of capabilities are located at an offset greater than 0FFh relative to the beginning of PCI compatible configuration space.

PI7C9X2G1224GP

| 31 - 24 | 23 - 16 | 15 - 8 | 7 - 0 | BYTE OFFSET |
|-----------------------------------|--------------|------------------------------------------|-------|-------------|
| Next Capability Offset=C34h | Cap. Version | PCI Express Extended Capability ID=0003h | | 100h |
| Serial Number Lower DW | | | | 104h |
| Serial Number Upper DW | | | | 108h |
| Reserved | | | | 10Ch - C30h |
| Next Capability Offset=000h | Cap. Version | PCI Express Extended Capability ID=000Bh | | C34h |
| Vendor Specific Header | | | | C38h |
| Translation BAR 2 | | | | C3Ch |
| Translation BAR 3 | | | | C40h |
| Translation BAR 4 | | | | C44h |
| Translation BAR 5 | | | | C48h |
| Reserved | | Virtual IF IRQ Set | | C4Ch |
| Reserved | | Virtual IF IRQ Clear | | C50h |
| Reserved | | Virtual IF IRQ Mask Set | | C54h |
| Reserved | | Virtual IF IRQ Mask Clear | | C58h |
| Reserved | | Link IF IRQ Set | | C5Ch |
| Reserved | | Link IF IRQ Clear | | C60h |
| Reserved | | Link IF IRQ Mask Set | | C64h |
| Reserved | | Link IF IRQ Mask Clear | | C68h |
| Scratchpad 0 | | | | C6Ch |
| Scratchpad 1 | | | | C70h |
| Scratchpad 2 | | | | C74h |
| Scratchpad 3 | | | | C78h |
| Scratchpad 4 | | | | C7Ch |
| Scratchpad 5 | | | | C80h |
| Scratchpad 6 | | | | C84h |
| Scratchpad 7 | | | | C88h |
| Reserved | | | | C8Ch - D90h |
| Virtual Port 32-Bits LTT Entry 0 | | | | D94h |
| Virtual Port 32-Bits LTT Entry 1 | | | | D98h |
| Virtual Port 32-Bits LTT Entry 2 | | | | D9Ch |
| Virtual Port 32-Bits LTT Entry 3 | | | | DA0h |
| Virtual Port 32-Bits LTT Entry 4 | | | | DA4h |
| Virtual Port 32-Bits LTT Entry 5 | | | | DA8h |
| Virtual Port 32-Bits LTT Entry 6 | | | | DACH |
| Virtual Port 32-Bits LTT Entry 7 | | | | DB0h |
| Link Port 16-Bits LTT Entry 0-1 | | | | DB4h |
| Link Port 16-Bits LTT Entry 2-3 | | | | DB8h |
| Link Port 16-Bits LTT Entry 4-5 | | | | DBCh |
| Link Port 16-Bits LTT Entry 6-7 | | | | DC0h |
| Link Port 16-Bits LTT Entry 8-9 | | | | DC4h |
| Link Port 16-Bits LTT Entry 10-11 | | | | DC8h |
| Link Port 16-Bits LTT Entry 12-13 | | | | DCCh |
| Link Port 16-Bits LTT Entry 14-15 | | | | DD0h |
| Link Port 16-Bits LTT Entry 16-17 | | | | DD4h |
| Link Port 16-Bits LTT Entry 18-19 | | | | DD8h |
| Link Port 16-Bits LTT Entry 20-21 | | | | DDCh |
| Link Port 16-Bits LTT Entry 22-23 | | | | DE0h |
| Link Port 16-Bits LTT Entry 24-25 | | | | DE4h |
| Link Port 16-Bits LTT Entry 26-27 | | | | DE8h |
| Link Port 16-Bits LTT Entry 28-29 | | | | DECh |
| Link Port 16-Bits LTT Entry 30-31 | | | | DF0h |
| Fail-Over CSR | | | | DF4h |
| Reserved | | | | DF8 - FFCh |

8.4.1 VENDOR ID REGISTER – OFFSET 00h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-----------|------|--------------------------------------------------|----------------------|---------|
| 15:0 | Vendor ID | RO | Identifies Pericom as the vendor of this device. | Yes | 12D8h |

8.4.2 DEVICE ID REGISTER – OFFSET 00h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------|------|-----------------------------------------------|----------------------|---------|
| 31:16 | Device ID | RO | Identifies this device as the PI7C9X2G1224GP. | Yes | 1224h |

8.4.3 COMMAND REGISTER – OFFSET 04h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|------------------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | I/O Space Enable | RW | 0b: Ignores I/O transactions on the primary interface 1b: Enables responses to I/O transactions on the primary interface | No/Yes | 0 |
| 1 | Memory Space Enable | RW | 0b: Ignores memory transactions on the primary interface 1b: Enables responses to memory transactions on the primary interface | No/Yes | 0 |
| 2 | Bus Master Enable | RW | 0b: Does not initiate memory or I/O transactions on the upstream port and handles as an Unsupported Request (UR) to memory and I/O transactions on the downstream port. For Non-Posted Requests, a completion with UR completion status must be returned 1b: Enables the Switch Port to forward memory and I/O Read/Write transactions in the upstream direction | No/Yes | 0 |
| 3 | Special Cycle Enable | RsvdP | Not Support. | No | 0 |
| 4 | Memory Write And Invalidate Enable | RsvdP | Not Support. | No | 0 |
| 5 | VGA Palette Snoop Enable | RsvdP | Not Support. | No | 0 |
| 6 | Parity Error Response Enable | RW | 0b: Switch may ignore any parity errors that it detects and continue normal operation 1b: Switch must take its normal action when a parity error is detected | No/Yes | 0 |
| 7 | Wait Cycle Control | RsvdP | Not Support. | No | 0 |
| 8 | SERR# enable | RW | 0b: Disables the reporting of Non-fatal and Fatal errors detected by the Switch to the Root Complex 1b: Enables the Non-fatal and Fatal error reporting to Root Complex | No/Yes | 0 |
| 9 | Fast Back-to-Back Enable | RsvdP | Not Support. | No | 0 |
| 10 | Interrupt Disable | RW | 0b: Enable to generate INTx Interrupt Messages 1b: Disable to generate INTx Interrupt Messages | No/Yes | 0 |
| 15:11 | Reserved | RsvdP | Not Support. | No | 0000 0b |

8.4.4 PRIMARY STATUS REGISTER – OFFSET 04h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-------------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 18:16 | Reserved | RsvdP | Not Support. | No | 000b |
| 19 | Interrupt Status | RO | Indicates that an INTx Interrupt Message is pending internally to the device. In the Switch, the forwarding of INTx messages from the downstream device of the Switch port is not reflected in this bit. Must be hardwired to 0. | No | 0 |
| 20 | Capabilities List | RO | Set to 1b to enable support for the capability list (offset 34h is the pointer to the data structure). | No | 1 |
| 21 | 66MHz Capable | RsvdP | Not Support | No | 0 |
| 22 | Reserved | RsvdP | Not Support. | No | 0 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 23 | Fast Back-to-Back Capable | RsvdP | Not Support. | No | 0 |
| 24 | Master Data Parity Error | RW1C | Set to 1b (by a requester) whenever a Parity error is detected or forwarded on the primary side of the port in a Switch. If the Parity Error Response Enable bit is cleared, this bit is never set. | No/Yes | 0 |
| 26:25 | DEVSEL# timing | RsvdP | Not Support. | No | 00b |
| 27 | Signaled Target Abort | RW1C | Set to 1b (by a requester) whenever a Completer Abort is detected. | No/Yes | 0 |
| 28 | Received Target Abort | RsvdP | Not Support. | No | 0 |
| 29 | Received Master Abort | RsvdP | Not Support. | No | 0 |
| 30 | Signaled System Error | RW1C | Set to 1b when the Switch sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR Enable bit in the Command register is 1. | No | 0 |
| 31 | Detected Parity Error | RW1C | Set to 1b whenever the primary side of the port in a Switch receives a Poisoned TLP. | No/Yes | 0 |

8.4.5 REVISION ID REGISTER – OFFSET 08h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|----------|------|--------------------------------------|----------------------|---------|
| 7:0 | Revision | RO | Indicates revision number of device. | No/Yes | 00h |

8.4.6 CLASS CODE REGISTER – OFFSET 08h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------------------|------|---------------------------------------------------------------------------------------------|----------------------|---------|
| 15:8 | Programming Interface | RO | Read as 00h to indicate no programming interfaces have been defined for PCI-to-PCI Bridges. | No | 00h |
| 23:16 | Sub-Class Code | RO | Read as 80h to indicate device is an Other Bridge. | No | 80h |
| 31:24 | Base Class Code | RO | Read as 06h to indicate device is a Bridge device. | No | 06h |

8.4.7 CACHE LINE REGISTER – OFFSET 0Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|-----------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 7:0 | Cache Line Size | RW | The cache line size register is set by the system firmware and the operating system cache line size. This field is implemented by PCI Express devices as a RW field for legacy compatibility, but it has no impact on any PCI Express device functionality. | No/Yes | 00h |

8.4.8 PRIMARY LATENCY TIMER REGISTER – OFFSET 0Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-----------------------|-------|--------------|----------------------|---------|
| 15:8 | Primary Latency Timer | RsvdP | Not Support. | No | 00h |

8.4.9 HEADER TYPE REGISTER – OFFSET 0Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-------------|------|-----------------------------------------------------------------------------------------------------------|----------------------|---------|
| 23:16 | Header Type | RO | Read as 00h to indicate that the register layout conforms to Type 0 Configuration Header for the NT Port. | No | 00h |

8.4.10 BAR 0 REGISTER – OFFSET 10h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|------------------------|-------|-----------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | Memory Space Indicator | RO | Reset to 0b to indicate the Base Address register maps NT Port Configuration registers into Memory Space. | No | 0 |
| 2:1 | Memory Map Type | RO | 00b: support 32-bit Memory Space. 10b: support 64-bit Memory Space. | No | 00b |
| 3 | Prefetchable | RO | Reset to 0b to indicate NT Port Configuration registers maps to Non-Prefetchable Memory Space. | No | 0 |
| 16:4 | Reserved | RsvdP | Not Support. | No | 0-0h |
| 31:17 | Base Address 0 | RW | Use this Memory base address to map the NT-Port Configuration registers. | No/Yes | 0-0h |

8.4.11 BAR 1 REGISTER – OFFSET 14h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|----------------|------|---------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 31:0 | Base Address 1 | RO | When 10h[2:1]=00b, BAR 0 is not enabled as a 64-bit BAR. | No | 0 |
| | | RW | When 10h[2:1]=10b, for 64-bit addressing (BAR 0/1), BAR 1 extends BAR 0 to provide the upper 32 Address bits. | No/Yes | 0 |

8.4.12 BAR 2 REGISTER – OFFSET 18h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|------------------------|-------|------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | Memory Space Indicator | RO | Reset to 0b to indicate it is a Memory BAR. | No | 0 |
| 2:1 | Memory Map Type | RO | 00b: support 32-bit Memory Space. 10b: support 64-bit Memory Space. | No | 00b |
| 3 | Prefetchable | RO | Reset to 0b to indicate NT Port Configuration registers maps to Non-Prefetchable Memory Space. | No | 0 |
| 19:4 | Reserved | RsvdP | Not Support. | No | 0-0h |
| 31:20 | Base Address 2 | RW | Base Address 2. | No/Yes | 000h |

8.4.13 BAR 3 REGISTER – OFFSET 1Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|------------------------|------|--------------------------------------------------------------------------|----------------------|---------|
| 0 | Memory Space Indicator | RO | When 18h[2:1]=00b, BAR 3 is used as an independent 32-bit BAR. | No | 0 |
| | | RW | When 18h[2:1]=10b, BAR 3 is used as the upper 32 bits of 64-bit BAR 2/3. | No/Yes | 0 |
| 2:1 | Memory Map Type | RO | When 18h[2:1]=00b, BAR 3 is used as an independent 32-bit BAR. | No | 00b |
| | | RW | When 18h[2:1]=10b, BAR 3 is used as the upper 32 bits of 64-bit BAR 2/3. | No/Yes | 00b |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|----------------|-------|--------------------------------------------------------------------------|----------------------|-----------|
| 3 | Prefetchable | RO | When 18h[2:1]=00b, BAR 3 is used as an independent 32-bit BAR. | No | 0 |
| | | RW | When 18h[2:1]=10b, BAR 3 is used as the upper 32 bits of 64-bit BAR 2/3. | No/Yes | 0 |
| 31:4 | Base Address 3 | RsvdP | When 18h[2:1]=00b, BAR 3 is used as an independent 32-bit BAR. | No | 0000_000h |
| | | RW | When 18h[2:1]=10b, BAR 3 is used as the upper 32 bits of 64-bit BAR 2/3. | No/Yes | 0000_000h |

8.4.14 BAR 4 REGISTER – OFFSET 20h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|------------------------|-------|------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | Memory Space Indicator | RO | Reset to 0b to indicate it is a Memory BAR. | No | 0 |
| 2:1 | Memory Map Type | RO | 00b: support 32-bit Memory Space 10b: support 64-bit Memory Space | No | 00b |
| 3 | Prefetchable | RO | Reset to 0b to indicate NT Port Configuration registers maps to Non-Prefetchable Memory Space. | No | 0 |
| 19:4 | Reserved | RsvdP | Not Support. | No | 0-0h |
| 31:20 | Base Address 4 | RW | Base Address 4. | No/Yes | 000h |

8.4.15 BAR 5 REGISTER – OFFSET 24h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|------------------------|-------|--------------------------------------------------------------------------|----------------------|-----------|
| 0 | Memory Space Indicator | RO | When 20h[2:1]=00b, BAR 5 is used as an independent 32-bit BAR. | No | 0 |
| | | RW | When 20h[2:1]=10b, BAR 5 is used as the upper 32 bits of 64-bit BAR 4/5. | No/Yes | 0 |
| 2:1 | Memory Map Type | RO | When 20h[2:1]=00b, BAR 5 is used as an independent 32-bit BAR. | No | 00b |
| | | RW | When 20h[2:1]=10b, BAR 5 is used as the upper 32 bits of 64-bit BAR 4/5. | No/Yes | 00b |
| 3 | Prefetchable | RO | When 20h[2:1]=00b, BAR 5 is used as an independent 32-bit BAR. | No | 0 |
| | | RW | When 20h[2:1]=10b, BAR 5 is used as the upper 32 bits of 64-bit BAR 4/5. | No/Yes | 0 |
| 31:4 | Base Address 3 | RsvdP | When 20h[2:1]=00b, BAR 5 is used as an independent 32-bit BAR. | No | 0000_000h |
| | | RW | When 20h[2:1]=10b, BAR 5 is used as the upper 32 bits of 64-bit BAR 4/5. | No/Yes | 0000_000h |

8.4.16 SUBSYSTEM VENDOR ID REGISTER – OFFSET 2Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|----------|------|----------------------------------------|----------------------|---------|
| 15:0 | SSVID | RO | It indicates the sub-system vendor id. | No/Yes | 12D8h |

8.4.17 SUBSYSTEM ID REGISTER – OFFSET 2Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------|------|----------------------------------------|----------------------|---------|
| 31:16 | SSID | RO | It indicates the sub-system device id. | No/Yes | 8619h |

8.4.18 CAPABILITY POINTER REGISTER – OFFSET 34h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|--------------------|------|------------------------------------|----------------------|---------|
| 7:0 | Capability Pointer | RO | Indicates next capability pointer. | Yes | 40h |

8.4.19 INTERRUPT LINE REGISTER – OFFSET 3Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|----------------|------|---------------------------|----------------------|---------|
| 7:0 | Interrupt Line | RW | Indicates Interrupt Line. | No/Yes | 00h |

8.4.20 INTERRUPT PIN REGISTER – OFFSET 3Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|---------------|------|-------------------------------------------------------------------------------------|----------------------|---------|
| 15:8 | Interrupt Pin | RO | The Switch implements INTA virtual wire interrupt signal. Only 00h or 01h is valid. | Yes | 01h |

8.4.21 POWER MANAGEMENT CAPABILITIES REGISTER – OFFSET 40h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------------|-------|----------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 7:0 | Enhanced Capabilities ID | RO | Read as 01h to indicate that these are power management enhanced capability registers. | No | 01h |
| 15:8 | Next Item Pointer | RO | Indicates next capability pointer. | Yes | 48h |
| 18:16 | Power Management Revision | RO | Read as 011b to indicate the device is compliant to Revision 1.2 of <i>PCI Power Management Interface Specifications</i> . | No | 011b |
| 19 | PME# Clock | RsvdP | Not Support. | No | 0 |
| 20 | Reserved | RsvdP | Not Support. | No | 0 |
| 21 | Device Specific Initialization | RO | Read as 0b to indicate Switch does not have device specific initialization requirements. | Yes | 0 |
| 24:22 | AUX Current | RO | Reset to 000b. | Yes | 000b |
| 25 | D1 Power State Support | RO | Read as 0b to indicate Switch does not support the D1 power management state. | Yes | 0 |
| 26 | D2 Power State Support | RO | Read as 0b to indicate Switch does not support the D2 power management state. | Yes | 0 |
| 31:27 | PME# Support | RO | Read as 19h to indicate Switch supports the forwarding of PME# message in D0, D3 and D4 states. | Yes | 19h |

8.4.22 POWER MANAGEMENT DATA REGISTER – OFFSET 44h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|-------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 1:0 | Power State | RW | Indicates the current power state of the Switch. Writing a value of D0 when the previous state was D3 cause a hot reset without asserting DWRST_L. 00b: D0 state 01b: D1 state 10b: D2 state 11b: D3 hot state | No/Yes | 00b |
| 2 | Reserved | RsvdP | Not Support. | No | 0 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 3 | No_Soft_Reset | RO | When set, this bit indicates that device transitioning from D3hot to D0 does not perform an internal reset. When clear, an internal reset is performed when power state transits from D3hot to D0. | Yes | 1 |
| 7:4 | Reserved | RsvdP | Not Support. | No | 0h |
| 8 | PME# Enable | RW | When asserted, the Switch will generate the PME# message. | No/Yes | 0 |
| 12:9 | Data Select | RO | Select data registers. | No/Yes | 0h |
| 14:13 | Data Scale | RO | Reset to 00b. | No | 00b |
| 15 | PME Status | RO | Read as 0b as the PME# message is not implemented. | No | 0 |

8.4.23 PPB SUPPORT EXTENSIONS – OFFSET 44h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------------------------|-------|--------------------------------------------------------|----------------------|----------|
| 21:16 | Reserved | RsvdP | Not Support. | No | 00_0000b |
| 22 | B2_B3 Support for D3HOT | RO | Does not apply to PCI Express. Must be hardwired to 0. | No | 0 |
| 23 | Bus Power / Clock Control Enable | RO | Does not apply to PCI Express. Must be hardwired to 0. | No | 0 |

8.4.24 DATA REGISTER – OFFSET 44h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------|------|----------------|----------------------|---------|
| 31:24 | Data Register | RO | Data Register. | Yes | 00h |

8.4.25 MSI CAPABILITIES REGISTER – OFFSET 48h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 7:0 | Enhanced Capabilities ID | RO | Read as 05h to indicate that this is message signal interrupt capability register. | No | 05h |
| 15:8 | Next Item Pointer | RO | Indicates next capability pointer. | Yes | 68h |
| 16 | MSI Enable | RW | 0b: The function is prohibited from using MSI to request service 1b: The function is permitted to use MSI to request service and is prohibited from using its INTx # pin | No/Yes | 0 |
| 19:17 | Multiple Message Capable | RO | Do not support multiple messages. | No | 000b |
| 22:20 | Multiple Message Enable | RW | Reset to 000b. | No/Yes | 000b |
| 23 | 64-bit address capable | RO | 0b: The function is not capable of generating a 64-bit message address 1b: The function is capable of generating a 64-bit message address | No | 1b |
| 31:24 | Reserved | RsvdP | Not Support. | No | 00h |

8.4.26 MESSAGE ADDRESS REGISTER – OFFSET 4Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-----------------|-------|-------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 1:0 | Reserved | RsvdP | Not Support. | No | 00b |
| 31:2 | Message Address | RW | If the message enable bit is set, the contents of this register specify the DWORD aligned address for MSI memory write transaction. | No/Yes | 0-0h |

8.4.27 MESSAGE UPPER ADDRESS REGISTER – OFFSET 50h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-----------------------|------|-----------------------------------------------------------------------------------------|----------------------|------------|
| 31:0 | Message Upper Address | RW | This register is only effective if the device supports a 64-bit message address is set. | No/Yes | 0000_0000h |

8.4.28 MESSAGE DATA REGISTER – OFFSET 54h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------|-------|---------------|----------------------|---------|
| 15:0 | Message Data | RW | Message data. | No/Yes | 0000h |
| 31:16 | Reserved | RsvdP | Not Support. | No | 0000h |

8.4.29 PCI EXPRESS CAPABILITIES REGISTER – OFFSET 68h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------|-------|-------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 7:0 | Enhanced Capabilities ID | RO | Read as 10h to indicate that these are PCI express enhanced capability registers. | No | 10h |
| 15:8 | Next Item Pointer | RO | Indicates next capability pointer. | Yes | A4h |
| 19:16 | Capability Version | RO | Read as 2h to indicate the device is compliant to Revision .2.0 of <i>PCI Express Base Specifications</i> . | No | 2h |
| 23:20 | Device/Port Type | RO | Indicates the type of PCI Express logical device. | No | 0h |
| 24 | Slot Implemented | RO | Reset to 0b. | No | 0 |
| 29:25 | Interrupt Message Number | RO | Read as 0. No MSI messages are generated in the transparent mode. | No | 00_000b |
| 31:30 | Reserved | RsvdP | Not Support. | No | 00b |

8.4.30 DEVICE CAPABILITIES REGISTER – OFFSET 6Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------------------------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 2:0 | Max_Payload_Size Supported | RO | Indicates the maximum payload size that the device can support for TLPs. 000b: 128 payload size 001b: 256 payload size 010b: 512 payload size | Yes | 001b |
| 4:3 | Phantom Functions Supported | RO | Indicates the support for use of unclaimed function numbers as Phantom functions. Read as 0, since the Switch does not act as a requester. | No | 00b |
| 5 | Extended Tag Field Supported | RO | Indicates the maximum supported size of Tag field as a Requester. Read as 0, since the Switch does not act as a requester. | No | 0 |
| 8:6 | Endpoint L0s Acceptable Latency | RO | Acceptable total latency that an Endpoint can withstand due to the transition from L0s state to the L0 state. For Switch, the ASPM software would not check this value. | No | 111b |
| 11:9 | Endpoint L1 Acceptable Latency | RO | Acceptable total latency that an Endpoint can withstand due to the transition from L1 state to the L0 state. For Switch, the ASPM software would not check this value. | No | 111b |
| 14:12 | Reserved | RsvdP | Not Support. | No | 000b |
| 15 | Role_Based Error Reporting | RO | When set, indicates that the device implements the functionality originally defined in the Error Reporting ECN. | Yes | 1 |
| 17:16 | Reserved | RsvdP | Not Support. | No | 00b |
| 25:18 | Captured Slot Power Limit Value | RO | These bits are hardwired to 0. | No | 00h |
| 27:26 | Captured Slot Power Limit Scale | RO | These bits are hardwired to 0. | No | 00b |
| 31:28 | Reserved | RsvdP | Not Support. | No | 0h |

8.4.31 DEVICE CONTROL REGISTER – OFFSET 70h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | Correctable Error Reporting Enable | RW | 0b: Disable Correctable Error Reporting 1b: Enable Correctable Error Reporting | No/Yes | 0 |
| 1 | Non-Fatal Error Reporting Enable | RW | 0b: Disable Non-Fatal Error Reporting 1b: Enable Non-Fatal Error Reporting | No/Yes | 0 |
| 2 | Fatal Error Reporting Enable | RW | 0b: Disable Fatal Error Reporting 1b: Enable Fatal Error Reporting | No/Yes | 0 |
| 3 | Unsupported Request Reporting Enable | RW | 0b: Disable Unsupported Request Reporting 1b: Enable Unsupported Request Reporting | No/Yes | 0 |
| 4 | Enable Relaxed Ordering | RO | When set, it permits the device to set the Relaxed Ordering bit in the attribute field of transaction. Since the Switch can not either act as a requester or alter the content of packet it forwards, this bit always returns '0' when read. | No | 0 |
| 7:5 | Max_Payload_Size | RW | This field sets maximum TLP payload size for the device. Permissible values that can be programmed are indicated by the Max_Payload_Size Supported in the Device Capabilities register. Any value exceeding the Max_Payload_Size Supported written to this register results into clamping to the Max_Payload_Size Supported value. | No/Yes | 000b |
| 8 | Extended Tag Field Enable | RsvdP | Not Support. | No | 0 |
| 9 | Phantom Function Enable | RsvdP | Not Support. | No | 0 |
| 10 | Auxiliary (AUX) Power PM Enable | RsvdP | Not Support. | No | 0 |
| 11 | Enable No Snoop | RsvdP | Not Support. | No | 0 |
| 14:12 | Max_Read_Request_Size | RO | This field sets the maximum Read Request size for the device as a Requester. Since the Switch does not generate read request by itself, these bits are hardwired to 0. | No | 000b |
| 15 | Reserved | RsvdP | Not Support. | No/No | 0 |

8.4.32 DEVICE STATUS REGISTER – OFFSET 70h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|------------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 16 | Correctable Error Detected | RW1C | Asserted when correctable error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. | No/Yes | 0 |
| 17 | Non-Fatal Error Detected | RW1C | Asserted when non-fatal error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. | No/Yes | 0 |
| 18 | Fatal Error Detected | RW1C | Asserted when fatal error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. | No/Yes | 0 |
| 19 | Unsupported Request Detected | RW1C | Asserted when unsupported request is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. | No/Yes | 0 |
| 20 | AUX Power Detected | RO | Asserted when the AUX power is detected by the Switch | No | 0 |
| 21 | Transactions Pending | RO | Each port of Switch does not issue Non-posted Requests on its own behalf, so this bit is hardwired to 0. | No | 0 |
| 31:22 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.4.33 LINK CAPABILITIES REGISTER – OFFSET 74h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------------------------------------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------------------------------------|
| 3:0 | Maximum Link Speed | RO | Indicates the maximum speed of the Express link. 0001b: link is 2.5 Gb/s 0010b: link is 5Gb/s Others: Reserved | No | 2h |
| 9:4 | Maximum Link Width | HWInt RO | Indicates the maximum width of the given PCIe Link. 00_0001b: x1 link 00_0010b: x2 link 00_0100b: x4 link 00_1000b: x8 link Others: Reserved | No | 08h, 04h, 02h or 01h |
| 11:10 | Active State Power Management (ASPM) Support | RO | Indicates the level of ASPM supported on the given PCIe Link. Each port of Switch supports L0s and L1 entry. | Yes | 01b |
| 14:12 | L0s Exit Latency | RO | Indicates the L0s exit latency for the given PCIe Link. The length of time this port requires to complete transition from L0s to L0 is in the range of 256ns to less than 512ns. | Yes | 011b |
| 17:15 | L1 Exit Latency | RO | Indicates the L1 exit latency for the given PCIe Link. The length of time this port requires to complete transition from L1 to L0 is less than 1us. | Yes | 000b |
| 18 | Clock Power Management | RO | This bit must be hardwired to 0. | Yes | 1 |
| 19 | Surprise Down Capability Enable | RsvdP | Not Support. | No | 0 |
| 20 | Data Link Layer Active Reporting Capable | RsvdP | Not Support. | No | 0 |
| 21 | Link BW Notify Capability | RsvdP | Not Support. | No | 0 |
| 23:20 | Reserved | RsvdP | Not Support. | No | 0-0h |
| 31:24 | Port Number | RO | Indicates the NT-Port Number. | Yes | 00h... Port 0 01h... Port 1 ... |

8.4.34 LINK CONTROL REGISTER – OFFSET 78h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-----|----------------------------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 1:0 | Active State Power Management (ASPM) Control | RW | 00b: ASPM is Disabled 01b: L0s Entry Enabled 10b: L1 Entry Enabled 11b: L0s and L1 Entry Enabled Note that the receiver must be capable of entering L0s even when the field is disabled | No/Yes | 00b |
| 2 | Reserved | RsvdP | Not Support. | No | 0 |
| 3 | Read Completion Boundary (RCB) | RO | Does not apply to PCI Express Switch. Returns '0' when read. | No | 0 |
| 4 | Link Disable | RsvdP | Not Support. | No | 0 |
| 5 | Retrain Link | RsvdP | Not Support. | No | 0 |
| 6 | Common Clock Configuration | RW | 0b: The components at both ends of a link are operating with synchronous reference clock. 1b: The components at both ends of a link are operating with a distributed common reference clock | No/Yes | 0 |
| 7 | Extended Synch | RW | When set, it transmits 4096 FTS ordered sets in the L0s state for entering L0 state and transmits 1024 TS1 ordered sets in the L1 state for entering L0 state. | No/Yes | 0 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------------------------|-------|--------------|----------------------|---------|
| 8 | Enable Clock Power Management | RsvdP | Not Support. | No/Yes | 0 |
| 9 | HW Autonomous Width Disable | RW | Reset to 0b. | No/Yes | 0 |
| 10 | Link Bandwidth Management Interrupt Enable | RW | Reset to 0b. | No/Yes | 0 |
| 11 | Link Autonomous Bandwidth Interrupt Enable | RW | Reset to 0b. | No/Yes | 0 |
| 15:12 | Reserved | RsvdP | Not Support. | No | 00h |

8.4.35 LINK STATUS REGISTER – OFFSET 78h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------------------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|----------|
| 19:16 | Link Speed | RO | Indicate the negotiated speed of the Express link. 0001b: link is 2.5 Gb/s 0010b: link is 5.0 Gb/s | No | 1h |
| 25:20 | Negotiated Link Width | RO | Indicates the negotiated width of the given PCIe link. 00_0001b: x1 link 00_0010b: x2 link 00_0100b: x4 link | No | 00_0001b |
| 26 | Training Error | RsvdP | Not Support. | No | 0 |
| 27 | Link Training | RsvdP | Not Support. | No | 0 |
| 28 | Slot Clock Configuration | RO | 0b: the Switch uses an independent clock corresponsive of the presence of a reference on the connector 1b: the Switch uses the same reference clock that the platform provides on the connector | Yes | 1 |
| 29 | Data Link Layer Link Active | RsvdP | Not Support. | No | 0 |
| 30 | Link Bandwidth Management Status | RO | Reset to 0b. | No | 0 |
| 31 | Link Autonomous Bandwidth Status | RO | Reset to 0b. | No | 0 |

8.4.36 LINK CONTROL REGISTER 2 – OFFSET 98h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------------------------------|-------|--------------|----------------------|---------|
| 3:0 | Target Link Speed | RW | Not Support. | No/Yes | 2h |
| 4 | Enter Compliance | RW | Not Support. | No/Yes | 0 |
| 5 | Hardware Autonomous Speed Disable | RW | Not Support. | No/Yes | 0 |
| 6 | Selectable De-Emphasis | RsvdP | Not Support. | No | 0 |
| 9:7 | Tran Margin | RW | Not Support. | No/Yes | 000b |
| 10 | Enter Modify Compliance | RW | Not Support. | No/Yes | 0 |
| 11 | Compliance SOS | RW | Not Support. | No/Yes | 0 |
| 12 | Compliance Deemp | RW | Not Support. | No/Yes | 0 |
| 15:13 | Reserved | RsvdP | Not Support. | No | 000b |

8.4.37 LINK STATUS REGISTER 2 – OFFSET 98h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------------------|------|------------------------|----------------------|---------|
| 16 | Current De-emphasis level | RO | 0b: -6dB 1b: -3.5dB | No | 0 |
| 31:17 | Link status 2 | RO | Not Support. | No | 0-0h |

8.4.38 SSID/SSVID CAPABILITIES REGISTER – OFFSET A4h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------------------|-------|------------------------------------------------------------------------|----------------------|---------|
| 7:0 | SSID/SSVID Capabilities ID | RO | Read as 0D to indicate that these are SSID/SSVID capability registers. | No | 0Dh |
| 15:8 | Next Item Pointer | RO | Indicates next capability pointer. | Yes | C8h |
| 31:16 | Reserved | RsvdP | Not Support. | No | 0000h |

8.4.39 SUBSYSTEM VENDOR ID REGISTER – OFFSET A8h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|----------|------|----------------------------------------|----------------------|---------|
| 15:0 | SSVID | RO | It indicates the sub-system vendor id. | Yes | 12D8h |

8.4.40 SUBSYSTEM ID REGISTER – OFFSET A8h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------|------|----------------------------------------|----------------------|---------|
| 31:16 | SSID | RO | It indicates the sub-system device id. | Yes | 8619h |

8.4.41 VENDOR SPECIFIC CAPABILITIES REGISTER – OFFSET C8h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------|------|--------------------------------------------------------------------------------------------|----------------------|---------|
| 7:0 | Enhanced Capabilities ID | RO | Read as 09h to indicate that these are vendor specific capability registers. | No | 09h |
| 15:8 | Next Item Pointer | RO | Read as 00h. No other ECP registers. | No | 00h |
| 31:16 | Length Information | RO | The length field provides the information for number of bytes in the capability structure. | No | 0038h |

8.4.42 VENDOR SPECIFIC HEADER REGISTER – OFFSET CCh

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|----------|-------|----------------------|----------------------|------------|
| 31:0 | Reserved | RsvdP | Reset to 0380 0002h. | No | 0380 0002h |

8.4.43 NT PORT VIRTUAL INTERFACE BAR 0-1 CONFIGURATION REGISTER – OFFSET D0h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-------------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 1:0 | BAR0 Type | RW | 00b: Disable BAR0/1 01b: Reserved 10b: BAR0 is implemented as a 32 bit Memory BAR 11b: BAR0/1 is implemented as a 64-bit Memory BAR | Yes | 10b |
| 2 | BAR0 Prefetchable | RW | 0b: Non Prefetchable 1b: Prefetchable | Yes | 0 |
| 31:3 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.4.44 NT PORT VIRTUAL INTERFACE BAR 2 CONFIGURATION REGISTER – OFFSET D4h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------|-------|----------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | Type Selector | RsvdP | Not Support. | No | 0 |
| 2:1 | BAR2 Type | RW | 00b: BAR2 is implemented as a 32 bit Memory BAR 10b: BAR2/3 is implemented as a 64-bit Memory BAR | No/Yes | 00b |
| 3 | Prefetchable | RW | 0b: Non Prefetchable 1b: Prefetchable | No/Yes | 0 |
| 19:4 | Reserved | RsvdP | Not Support. | No | 0_000h |
| 30:20 | BAR2 Size | RW | To specify BAR2 size. 0b: Corresponding BAR2 bits are RO bits that always return 0 1b: Corresponding BAR2 bits are RW bits | No/Yes | 0-0h |
| 31 | BAR 2 Enable | RW | Valid when bits[2:1]=00b. 0b: Disable BAR2 1b: Enable BAR2 | No/Yes | 0 |
| | BAR 2 Size | RW | Includes with bits[30:20] when tis BAR is used as a 64-bit BAR (bits[2:1]=10b). | | |

8.4.45 NT PORT VIRTUAL INTERFACE BAR 2-3 CONFIGURATION REGISTER – OFFSET D8h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------|-------|----------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | Type Selector | RsvdP | Not Support. | No | 0 |
| 2:1 | BAR3 Type | RO | 00b: BAR3 is implemented as a 32-bit Memory BAR. | No | 00b |
| 3 | Prefetchable | RW | 0b: Non Prefetchable 1b: Prefetchable | No/Yes | 0 |
| 19:4 | Upper 32 Bits | RsvdP | Not Support when D4h[2:1]=00b. | No | 0_000h |
| | | RW | When D4h[2:1]=10b, BAR2/3 are used as a 64-bit BAR, bit[31:0] (including bit[19:4]) are used as the upper 32-bits. | No/Yes | 0_000h |
| 30:20 | BAR3 Size | RW | To specify BAR3 size. 0b: Corresponding BAR3 bits are RO bits that always return 0 1b: Corresponding BAR3 bits are RW bits | No/Yes | 000h |
| 31 | BAR 3 Enable | RW | Valid when D4h[2:1]=00b. 0b: Disable BAR3 1b: Enable BAR3 | No/Yes | 0 |
| | 64-Bit BAR | RW | Valid when D4h[2:1]=10b. 0b: BAR2/3 is disabled, all BAR2/3 bits read 0. 1b: BAR2/3 is enabled as a 64-bit BAR. | | |

8.4.46 NT PORT VIRTUAL INTERFACE BAR 4 CONFIGURATION REGISTER – OFFSET DCh

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------|-------|----------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | Type Selector | RsvdP | Not Support. | No | 0 |
| 2:1 | BAR4 Type | RW | 00b: BAR4 is implemented as a 32 bit Memory BAR 10b: BAR4/5 is implemented as a 64-bit Memory BAR | No/Yes | 00b |
| 3 | Prefetchable | RW | 0b: Non Prefetchable 1b: Prefetchable | No/Yes | 0 |
| 19:4 | Reserved | RsvdP | Not Support. | No | 0_000h |
| 30:20 | BAR4 Size | RW | To specify BAR4 size. 0b: Corresponding BAR4 bits are RO bits that always return 0 1b: Corresponding BAR4 bits are RW bits | No/Yes | 0-0h |
| 31 | BAR4 Enable | RW | Valid when bis[2:1]=00b. 0b: Disable BAR4 1b: Enable BAR4 | No/Yes | 0 |
| | BAR 4 Size | RW | Includes with bits[30:20] when tis BAR is used as a 64-bit BAR (bits[2:1]=10b). | | |

8.4.47 NT PORT VIRTUAL INTERFACE BAR 4/5 CONFIGURATION REGISTER – OFFSET E0h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|---------------|-------|----------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 0 | Type Selector | RsvdP | Not Support. | No | 0 |
| 2:1 | BAR5 Type | RO | 00b: BAR5 is implemented as a 32-bit Memory BAR. | No | 00b |
| 3 | Prefetchable | RW | 0b: Non Prefetchable 1b: Prefetchable | No/Yes | 0 |
| 19:4 | Upper 32 Bits | RsvdP | Not Support when DCh[2:1]=00b. | No | 0_000h |
| | | RW | When DCh[2:1]=10b, BAR4/5 are used as a 64-bit BAR, bit[31:0] (including bit[19:4]) are used as the upper 32-bits. | No/Yes | 0_000h |
| 30:20 | BAR5 Size | RW | To specify BAR5 size. 0b: Corresponding BAR5 bits are RO bits that always return 0 1b: Corresponding BAR5 bits are RW bits | No/Yes | 000h |
| 31 | BAR 5 Enable | RW | Valid when DCh[2:1]=00b. 0b: Disable BAR5. 1b: Enable BAR5. | No/Yes | 0 |
| | 64-Bit BAR | RW | Valid when DCh[2:1]=10b. 0b: BAR4/5 is disabled, all BAR4/5 bits read 0. 1b: BAR4/5 is enabled as a 64-bit BAR. | | |

8.4.48 DEVICE SERIAL NUMBER ENHANCED CAPABILITY HEADER REGISTER – OFFSET 100h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------|------|-----------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 15:0 | Extended Capabilities ID | RO | Read as 0003h to indicate that these are PCI express extended capability registers for device serial number extend capability register. | No | 0003h |
| 19:16 | Capability Version | RO | Must be 1h for this version. | No | 1h |
| 31:20 | Next Capability Offset | RO | Pointer points to the Advanced Error Reporting Extended Capability structure. | Yes | C34h |

8.4.49 DEVICE SERIAL NUMBER LOWER DW REGISTER – OFFSET 104h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|--------------------------------------------|------|---------------------------------------|----------------------|------------|
| 31:0 | Device serial number 1 st DW | RO | First dword for device serial number. | Yes | 0000_0000h |

8.4.50 DEVICE SERIAL NUMBER HIGHER DW REGISTER – OFFSET 108h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|--------------------------------------------|------|----------------------------------------|----------------------|------------|
| 31:0 | Device serial number 2 nd DW | RO | Second dword for device serial number. | Yes | 0000_0000h |

8.4.51 VENDOR SPECIFIC ENHANCED CAPABILITY HEADER REGISTER – OFFSET C34h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------------------------|------|-------------------------------------------------------------------------------------------------------------------|----------------------|---------|
| 15:0 | Extended Capabilities ID | RO | Read as 000Bh to indicate that these are PCI express extended capability registers for vendor specific registers. | No | 000Bh |
| 19:16 | Capability Version | RO | Read as 1h. | No | 1h |
| 31:20 | Next Capability Offset | RO | Read as 000h. No other ECP registers. | No | 000h |

8.4.52 VENDOR SPECIFIC HEADER REGISTER – OFFSET C38h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|---------------------------|------|----------------------|----------------------|------------|
| 31:0 | Vendor Specific Header | RO | Reset to 0780_0003h. | No | 0780_0003h |

8.4.53 MEMORY BAR 2 ADDRESS TRANSLATION REGISTER – OFFSET C3Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-------------------------------------|-------|-------------------------------------------------|----------------------|---------|
| 19:0 | Reserved | RsvdP | Not Support. | No | 0_0000h |
| 31:20 | Memory BAR 2 Address Translation | RW | Valid when BAR 2 is enabled (offset E8h[31]=1). | Yes | 000h |

8.4.54 MEMORY BAR 3 ADDRESS TRANSLATION REGISTER – OFFSET C40h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-------------------------------------|-------|------------------------------------------|----------------------|---------|
| 19:0 | Reserved | RsvdP | Not Support. | No | 000h |
| 31:20 | Memory BAR 3 Address Translation | RW | Valid when BAR 3 is enabled (ECh[31]=1). | Yes | 000h |

8.4.55 MEMORY BAR4 ADDRESS TRANSLATION REGISTER – OFFSET C44h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-------------------------------------|-------|-------------------------------------------------|----------------------|---------|
| 19:0 | Reserved | RsvdP | Not Support. | No | 0 0000h |
| 31:20 | Memory BAR 4 Address Translation | RW | Valid when BAR 4 is enabled (offset F0h[31]=1). | Yes | 000h |

8.4.56 MEMORY BAR 5 ADDRESS TRANSLATION REGISTER – OFFSET C48h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|-------------------------------------|-------|------------------------------------------|----------------------|---------|
| 19:0 | Reserved | RsvdP | Not Support. | No | 000h |
| 31:0 | Memory BAR 5 Address Translation | RW | Valid when BAR 5 is enabled (F4h[31]=1). | Yes | 000h |

8.4.57 VIRTUAL IF IRQ SET REGISTER – OFFSET C4Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------|-------|----------------------------|----------------------|---------|
| 15:0 | Set IRQ | RW | Set virtual interface IRQ. | No/Yes | 0000h |
| 31:16 | Reserved | RsvdP | Not Support. | No | 0000h |

8.4.58 VIRTUAL IF IRQ CLEAR REGISTER – OFFSET C50h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------|-------|------------------------------|----------------------|---------|
| 15:0 | Clear IRQ | RW1C | Clear virtual interface IRQ. | No/Yes | 0000h |
| 31:16 | Reserved | RsvdP | Not Support. | No | 0000h |

8.4.59 VIRTUAL IF IRQ MASK SET REGISTER – OFFSET C54h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------|-------|-------------------------------------------|----------------------|---------|
| 15:0 | Set IRQ Mask | RW | Set virtual interface interrupt IRQ mask. | No/Yes | FFFFh |
| 31:16 | Reserved | RsvdP | Not Support. | No | 0000h |

8.4.60 VIRTUAL IF IRQ MASK CLEAR REGISTER – OFFSET C58h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------|-------|---------------------------------------------|----------------------|---------|
| 15:0 | Clear IRQ Mask | RW1C | Clear virtual interface interrupt IRQ mask. | No/Yes | FFFFh |
| 31:16 | Reserved | RsvdP | Not Support. | No | 0000h |

8.4.61 LINK IF IRQ SET REGISTER – OFFSET C5Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------|-------|-------------------------|----------------------|---------|
| 15:0 | Set IRQ | RW | Set link interface IRQ. | No/Yes | 0000h |
| 31:16 | Reserved | RsvdP | Not Support. | No | 0000h |

8.4.62 LINK IF IRQ CLEAR REGISTER – OFFSET C60h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|-----------|-------|---------------------------|----------------------|---------|
| 15:0 | Clear IRQ | RW1C | Clear link interface IRQ. | No/Yes | 0000h |
| 31:16 | Reserved | RsvdP | Not Support. | No | 0000h |

8.4.63 LINK IF IRQ MASK SET REGISTER – OFFSET C64h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------|-------|----------------------------------------|----------------------|---------|
| 15:0 | Set IRQ Mask | RW | Set link interface interrupt IRQ mask. | No/Yes | FFFFh |
| 31:16 | Reserved | RsvdP | Not Support. | No | 0000h |

8.4.64 LINK IF IRQ MASK CLEAR REGISTER – OFFSET C68h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|----------------|-------|------------------------------------------|----------------------|---------|
| 15:0 | Clear IRQ Mask | RW1C | Clear link interface interrupt IRQ mask. | No/Yes | FFFFh |
| 31:16 | Reserved | RsvdP | Not Support. | No | 0000h |

8.4.65 SCRATCHPAD 0 REGISTER – OFFSET C6Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|--------------|------|------------------------|----------------------|------------|
| 31:0 | Scratchpad 0 | RW | Scratchpad 0 register. | No/Yes | 0000_0000h |

8.4.66 SCRATCHPAD 1 REGISTER – OFFSET C70h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|--------------|------|------------------------|----------------------|------------|
| 31:0 | Scratchpad 1 | RW | Scratchpad 1 register. | No/Yes | 0000_0000h |

8.4.67 SCRATHPAD 2 REGISTER – OFFSET C74h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|--------------|------|------------------------|----------------------|------------|
| 31:0 | Scratchpad 2 | RW | Scratchpad 2 register. | No/Yes | 0000_0000h |

8.4.68 SCRATCHPAD 3 REGISTER – OFFSET C78h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|--------------|------|------------------------|----------------------|------------|
| 31:0 | Scratchpad 3 | RW | Scratchpad 3 register. | No/Yes | 0000_0000h |

8.4.69 SCRATCHPAD 4 REGISTER – OFFSET C7Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|--------------|------|------------------------|----------------------|------------|
| 31:0 | Scratchpad 4 | RW | Scratchpad 4 register. | No/Yes | 0000_0000h |

8.4.70 SCRATCHPAD 5 REGISTER – OFFSET C80h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|--------------|------|------------------------|----------------------|------------|
| 31:0 | Scratchpad 5 | RW | Scratchpad 5 register. | No/Yes | 0000_0000h |

8.4.71 SCRATCHPAD 6 REGISTER – OFFSET C84h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|--------------|------|------------------------|----------------------|------------|
| 31:0 | Scratchpad 6 | RW | Scratchpad 6 register. | No/Yes | 0000_0000h |

8.4.72 SCRATCHPAD 7 REGISTER – OFFSTE C88h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|--------------|------|------------------------|----------------------|------------|
| 31:0 | Scratchpad 8 | RW | Scratchpad 8 register. | No/Yes | 0000_0000h |

8.4.73 VIRTUAL PORT 32-BITS LTT ENTRY 0-7 – OFFSET D94h to DB0h

Table 8-10 Virtual Port 32-Bits LTT Entry 0-7 Register Locations

| CFG OFFSET | LTT Entry n | CFG OFFSET | LTT Entry n |
|------------|-------------|------------|-------------|
| D94h | 0 | DA4h | 4 |
| D98h | 1 | DA8h | 5 |
| D9Ch | 2 | DACH | 6 |
| DA0h | 3 | DB0h | 7 |

Table 8-11 Virtual Port 32-Bits LTT Entry_n (n=0 through 7)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------------|-------|-------------------------------------------------------------------------------|----------------------|---------|
| 15:0 | ReqID | RW | Bit[2:0]: function number Bit[7:3]: device number Bit[15:8]: bus number | No/Yes | 0000h |
| 29:16 | Reserved | RsvdP | Not Support. | No | 0-0h |
| 30 | LUT Entry_n No Snoop Enable | RsvdP | Not Support. | No | 0 |
| 31 | LUT Entry_n Enable | RW | 0b: disable 1b: enable | No/Yes | 0 |

8.4.74 LINK PORT 16-BITS LTT ENTRY 0-31 REGISTER – OFFSET DB4h – DF4h

Table 8-12 Link Port 16-Bits LTT Entry 0-31 Register Locations

| CFG OFFSET | LTT Entry_n | CFG OFFSET | LTT Entry_n |
|------------|-------------|------------|-------------|
| DB4h | 0-1 | DD4h | 16-17 |
| DB8h | 2-3 | DD8h | 18-19 |
| DBCh | 4-5 | DDCh | 20-21 |
| DC0h | 6-7 | DE0h | 22-23 |
| DC4h | 8-9 | DE4h | 24-25 |
| DC8h | 10-11 | DE8h | 26-27 |
| DCCh | 12-13 | DECh | 28-29 |
| DD0h | 14-15 | DF0h | 30-31 |

Table 8-13 Link Port 16-Bits LTT Entry_n_m (n_m 0-1 to 30-31)

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|-------|--------------------------------|-------|-------------------------------------------------|----------------------|---------|
| 0 | LUT Entry_n Enable | RW | 0b: disable 1b: enable | No/Yes | 0 |
| 1 | LUT Entry_n No Snoop Enable | RsvdP | Not Support. | No | 0 |
| 2 | Reserved | RsvdP | Not Support. | No | 0 |
| 15:3 | ReqID | RW | Bit[7:3]: device number Bit[15:8]: device id | No/Yes | 00h |
| 16 | LUT Entry_m Enable | RW | 0b: disable 1b: enable | No/Yes | 0 |
| 17 | LUT Entry_m No Snoop Enable | RsvdP | Not Support. | No | 0 |
| 18 | Reserved | RsvdP | Not Support. | No | 0 |
| 31:19 | ReqID | RW | Bit[7:3]: device number Bit[15:8]: device id | No/Yes | 00h |

8.4.75 FAIL-OVER CSR REGISTER – OFFSET DF4h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C-SMBUS | DEFAULT |
|------|--------------------|-------|-----------------|----------------------|---------|
| 0 | Pri Linksdwn Force | RW | Test used only. | Yes | 0 |
| 1 | 2nd Linksdwn Force | RW | Test used only. | Yes | 0 |
| 2 | Failover Enable | RW | Test used only. | Yes | 0 |
| 3 | Disable Hot Reset | RW | Test used only. | Yes | 0 |
| 31:4 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.5 DMA ENGINE CONFIGURATION REGISTERS (FUNC1)

The switch contains one DMA engine (function number 1). The following table details the allocation of the register fields of the PCI 2.3 compatible type 0 configuration space header.

| 31 – 24 | 23 – 16 | 15 – 8 | 7 – 0 | BYTE OFFSET |
|-----------------------------------|------------------------|-----------------------|---------------------------------|-------------|
| Device ID | | Vendor ID | | 00h |
| Primary Status | | Command | | 04h |
| Class Code | | | Revision ID | 08h |
| Reserved | Header Type | Reserved | Cache Line Size | 0Ch |
| BAR 0 | | | | 10h |
| Reserved | | | | 14h - 28h |
| SSID | | SSVID | | 2Ch |
| Reserved | | | | 30h |
| Reserved | | | Capability Pointer to 40h | 34h |
| Reserved | | | | 38h |
| Reserved | | Interrupt Pin | Interrupt Line | 3Ch |
| Power Management Capabilities | | Next Item Pointer=48h | Capability ID=01h | 40h |
| PM Data | PPB Support Extensions | Power Management Data | | 44h |
| Message Control | | Next Item Pointer=68h | Capability ID=05h | 48h |
| Message Address | | | | 4Ch |
| Message Upper Address | | | | 50h |
| Reserved | | Message Data | | 54h |
| Reserved | | | | 58h – 64h |
| PCI Express Capabilities Register | | Next Item Pointer=A4h | Capability ID=10h | 68h |
| Device Capabilities | | | | 6Ch |
| Device Status | | Device Control | | 70h |
| Link Capabilities | | | | 74h |
| Link Status | | Link Control | | 78h |
| Reserved | | | | 7Ch - 90h |
| Link Capabilities 2 | | | | 94h |
| Link Status 2 | | Link Control 2 | | 98h |
| Reserved | | | | 9Ch – A0h |
| Reserved | | Next Item Pointer=C8h | SSID/SSVID Capability ID=0Dh | A4h |
| SSID | | SSVID | | A8h |
| Reserved | | | | ACH - FCh |

Other than the PCI 2.3 compatible configuration space header, Func 0 (upstream port of the switch) and Func 1 (DMA engine) share the PCI express extended configuration space header, which includes advanced error reporting, virtual channel, and power budgeting capability registers. Please refer to Section 8-2.

8.5.1 VENDOR ID REGISTER – OFFSET 00h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|------|-----------|------|-------------------------------------------------|----------------|---------|
| 15:0 | Vendor ID | RO | Identifies Diodes as the vendor of this device. | Yes | 12D8h |

8.5.2 DEVICE ID REGISTER – OFFSET 00h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|-------|-----------|------|-----------------------------------------------|----------------|---------|
| 31:16 | Device ID | RO | Identifies this device as the PI7C9X2G1224GP. | Yes | 1224h |

8.5.3 COMMAND REGISTER – OFFSET 04h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|-------|------------------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|---------|
| 0 | I/O Space Enable | RW | 0b: Ignores I/O transactions on the primary interface 1b: Enables responses to I/O transactions on the primary interface | No/Yes | 0 |
| 1 | Memory Space Enable | RW | 0b: Ignores memory transactions on the primary interface 1b: Enables responses to memory transactions on the primary interface | No/Yes | 0 |
| 2 | Bus Master Enable | RW | 0b: Does not initiate memory or I/O transactions on the upstream port and handles as an Unsupported Request (UR) to memory and I/O transactions on the downstream port. For Non-Posted Requests, a completion with UR completion status must be returned 1b: Enables the Switch Port to forward memory and I/O Read/Write transactions in the upstream direction | No/Yes | 0 |
| 3 | Special Cycle Enable | RsvdP | Not Support. | No | 0 |
| 4 | Memory Write And Invalidate Enable | RsvdP | Not Support. | No | 0 |
| 5 | VGA Palette Snoop Enable | RsvdP | Not Support. | No | 0 |
| 6 | Parity Error Response Enable | RW | 0b: Switch may ignore any parity errors that it detects and continue normal operation 1b: Switch must take its normal action when a parity error is detected | No/Yes | 0 |
| 7 | Wait Cycle Control | RsvdP | Not Support. | No | 0 |
| 8 | SERR# enable | RW | 0b: Disables the reporting of Non-fatal and Fatal errors detected by the Switch to the Root Complex b1: Enables the Non-fatal and Fatal error reporting to Root Complex | No/Yes | 0 |
| 9 | Fast Back-to-Back Enable | RsvdP | Not Support. | No | 0 |
| 10 | Interrupt Disable | RW | 0b: Enable to generate INTx Interrupt Messages 1b: Disable to generate INTx Interrupt Messages | No/Yes | 0 |
| 15:11 | Reserved | RsvdP | Reset to 5'b0. | No | 0000 0b |

8.5.4 PRIMARY STATUS REGISTER – OFFSET 04h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|-------|---------------------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|---------|
| 18:16 | Reserved | RsvdP | Not Support. | No | 000b |
| 19 | Interrupt Status | RO | Indicates that an INTx Interrupt Message is pending internally to the device. In the Switch, the forwarding of INTx messages from the downstream device of the Switch port is not reflected in this bit. Must be hardwired to 1'b0. | No | 0 |
| 20 | Capabilities List | RO | Set to 1b to enable support for the capability list (offset 34h is the pointer to the data structure). | No | 1 |
| 21 | 66MHz Capable | RsvdP | Not Support | No | 0 |
| 22 | Reserved | RsvdP | Not Support. | No | 0 |
| 23 | Fast Back-to-Back Capable | RsvdP | Not Support. | No | 0 |
| 24 | Master Data Parity Error | RW1C | Set to 1b (by a requester) whenever a Parity error is detected or forwarded on the primary side of the port in a Switch. If the Parity Error Response Enable bit is cleared, this bit is never set. | No/Yes | |
| 26:25 | DEVSEL# timing | RsvdP | Not Support. | No | 00b |
| 27 | Signaled Target Abort | RW1C | Set to 1b (by a requester) whenever a Completer Abort is detected. | No/Yes | 0 |
| 28 | Received Target Abort | RsvdP | Not Support. | No | 0 |
| 29 | Received Master Abort | RsvdP | Not Support. | No | 0 |
| 30 | Signaled System Error | RW1C | Set to 1b when the Switch sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR Enable bit in the Command register is 1b. | No | 0 |
| 31 | Detected Parity Error | RW1C | Set to 1b whenever the primary side of the port in a Switch receives a Poisoned TLP. | No/Yes | 0 |

8.5.5 REVISION ID REGISTER – OFFSET 08h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|-----|----------|------|--------------------------------------|----------------|---------|
| 7:0 | Revision | RO | Indicates revision number of device. | No/Yes | 00h |

8.5.6 CLASS CODE REGISTER – OFFSET 08h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|-------|-----------------------|------|------------------------------------------------------------|----------------|---------|
| 15:8 | Programming Interface | RO | Read as 00h. | No | 00h |
| 23:16 | Sub-Class Code | RO | Read as 80h. | No | 80h |
| 31:24 | Base Class Code | RO | Read as 08h to indicate device is other system peripheral. | No | 06h |

8.5.7 CACHE LINE REGISTER – OFFSET 0Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|-----|-----------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|---------|
| 7:0 | Cache Line Size | RW | The cache line size register is set by the system firmware and the operating system cache line size. This field is implemented by PCI Express devices as a RW field for legacy compatibility, but it has no impact on any PCI Express device functionality. | No/Yes | 00h |

8.5.8 PRIMARY LATENCY TIMER REGISTER – OFFSET 0Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|------|-----------------------|-------|--------------|----------------|---------|
| 15:8 | Primary Latency Timer | RsvdP | Not Support. | No | 00h |

8.5.9 HEADER TYPE REGISTER – OFFSET 0Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|-------|-------------|------|-----------------------------------------------------------------------------------------------------------|----------------|---------|
| 23:16 | Header Type | RO | Read as 00h to indicate that the register layout conforms to Type 0 Configuration Header for the NT Port. | No | 00h |

8.5.10 BAR 0 REGISTER – OFFSET 10h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|------|----------------|------|-----------------------------------------------------------|----------------|---------|
| 8:0 | Base Address 0 | RO | Reset to 000h. | No | 0-0h |
| 31:9 | Base Address 0 | RW | Use this Memory base address to map DMA engine registers. | No/Yes | 0-0h |

8.5.11 SUBSYSTEM VENDOR ID REGISTER – OFFSET 2Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|------|----------|------|----------------------------------------|----------------|---------|
| 15:0 | SSVID | RO | It indicates the sub-system vendor id. | No/Yes | 12D8h |

8.5.12 SUBSYSTEM ID REGISTER – OFFSET 2Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|-------|----------|------|----------------------------------------|----------------|---------|
| 31:16 | SSID | RO | It indicates the sub-system device id. | No/Yes | 1224h |

8.5.13 CAPABILITY POINTER REGISTER – OFFSET 34h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|-----|--------------------|------|-------------------------------------------------------|----------------|---------|
| 7:0 | Capability Pointer | RO | Pointer points to the PCI power management registers. | Yes | 40h |

8.5.14 INTERRUPT LINE REGISTER – OFFSET 3Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|-----|----------------|------|----------------|----------------|---------|
| 7:0 | Interrupt Line | RW | Reset to 8'h0. | No/Yes | 00h |

8.5.15 INTERRUPT PIN REGISTER – OFFSET 3Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|------|---------------|------|-------------------------------------------------------------------------------------|----------------|---------|
| 15:8 | Interrupt Pin | RO | The Switch implements INTA virtual wire interrupt signal. Only 00h or 01h is valid. | Yes | 01h |

8.5.16 POWER MANAGEMENT CAPABILITIES REGISTER – OFFSET 40h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|-------|--------------------------------|-------|----------------------------------------------------------------------------------------------------------------------------|----------------|---------|
| 7:0 | Enhanced Capabilities ID | RO | Read as 01h to indicate that these are power management enhanced capability registers. | No | 01h |
| 15:8 | Next Item Pointer | RO | The pointer points to the MSI capability Structure. | Yes | 48h |
| 18:16 | Power Management Revision | RO | Read as 011b to indicate the device is compliant to Revision 1.2 of <i>PCI Power Management Interface Specifications</i> . | No | 011b |
| 19 | PME# Clock | RsvdP | Not Support. | No | 0 |
| 20 | Reserved | RsvdP | Not Support. | No | 0 |
| 21 | Device Specific Initialization | RO | Read as 0b to indicate Switch does not have device specific initialization requirements. | Yes | 0 |
| 24:22 | AUX Current | RO | Reset to 3'b0. | Yes | 000b |
| 25 | D1 Power State Support | RO | Read as 0b to indicate Switch does not support the D1 power management state. | Yes | 0 |
| 26 | D2 Power State Support | RO | Read as 0b to indicate Switch does not support the D2 power management state. | Yes | 0 |
| 31:27 | PME# Support | RO | Read as 19h to indicate Switch supports the forwarding of PME# message in D0, D3 and D4 states. | Yes | 19h |

8.5.17 POWER MANAGEMENT DATA REGISTER – OFFSET 44h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|-------|---------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|---------|
| 1:0 | Power State | RW | Indicates the current power state of the Switch. Writing a value of D0 when the previous state was D3 cause a hot reset without asserting DWRST_L. 00b: D0 state 01b: D1 state 10b: D2 state 11b: D3 hot state | No/Yes | 00b |
| 2 | Reserved | RsvdP | Not Support. | No | 0 |
| 3 | No_Soft_Reset | RO | When set, this bit indicates that device transitioning from D3hot to D0 does not perform an internal reset. When clear, an internal reset is performed when power state transits from D3hot to D0. | Yes | 1 |
| 7:4 | Reserved | RsvdP | Not Support. | No | 0h |
| 8 | PME# Enable | RW | When asserted, the Switch will generate the PME# message. | No/Yes | 0 |
| 12:9 | Data Select | RO | Select data registers. | No/Yes | 0h |
| 14:13 | Data Scale | RO | Reset to 2'b0. | No | 00b |
| 15 | PME Status | RO | Read as 1'b0 as the PME# message is not implemented. | No | 0 |

8.5.18 PPB SUPPORT EXTENSIONS – OFFSET 44h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|-------|----------------------------------|-------|-----------------------------------------------------------|----------------|----------|
| 21:16 | Reserved | RsvdP | Not Support. | No | 00 0000b |
| 22 | B2_B3 Support for D3HOT | RO | Does not apply to PCI Express. Must be hardwired to 1'b0. | No | 0 |
| 23 | Bus Power / Clock Control Enable | RO | Does not apply to PCI Express. Must be hardwired to 1'b0. | No | 0 |

8.5.19 DATA REGISTER – OFFSET 44h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|-------|---------------|------|----------------|----------------|---------|
| 31:24 | Data Register | RO | Data Register. | Yes | 00h |

8.5.20 MSI CAPABILITIES REGISTER – OFFSET 48h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|-------|--------------------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|---------|
| 7:0 | Enhanced Capabilities ID | RO | Read as 05h to indicate that this is message signal interrupt capability register. | No | 05h |
| 15:8 | Next Item Pointer | RO | Pointer points to the PCI Express Enhanced Capability Structure. | Yes | 68h |
| 16 | MSI Enable | RW | 0b: The function is prohibited from using MSI to request service 1b: The function is permitted to use MSI to request service and is prohibited from using its INTx # pin | No/Yes | 0 |
| 19:17 | Multiple Message Capable | RO | Do not support multiple messages. | No | 000b |
| 22:20 | Multiple Message Enable | RW | Reset to 3'b0. | No/Yes | 000b |
| 23 | 64-bit address capable | RO | 0b: The function is not capable of generating a 64-bit message address 1b: The function is capable of generating a 64-bit message address | No | 1b |
| 31:24 | Reserved | RsvdP | Not Support. | No | 00h |

8.5.21 MESSAGE ADDRESS REGISTER – OFFSET 4Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|------|-----------------|-------|-------------------------------------------------------------------------------------------------------------------------------------|----------------|---------|
| 1:0 | Reserved | RsvdP | Reset to 2'b0. | No | 00b |
| 31:2 | Message Address | RW | If the message enable bit is set, the contents of this register specify the DWORD aligned address for MSI memory write transaction. | No/Yes | 0-0h |

8.5.22 MESSAGE UPPER ADDRESS REGISTER – OFFSET 50h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|------|-----------------------|------|-----------------------------------------------------------------------------------------|----------------|------------|
| 31:0 | Message Upper Address | RW | This register is only effective if the device supports a 64-bit message address is set. | No/Yes | 0000_0000h |

8.5.23 MESSAGE DATA REGISTER – OFFSET 54h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|-------|--------------|-------|-----------------|----------------|---------|
| 15:0 | Message Data | RW | Reset to 16'd0. | No/Yes | 0000h |
| 31:16 | Reserved | RsvdP | Not Support. | No | 0000h |

8.5.24 PCI EXPRESS CAPABILITIES REGISTER – OFFSET 68h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|-------|--------------------------|-------|---------------------------------------------------------------------------------------------------------------|----------------|---------|
| 7:0 | Enhanced Capabilities ID | RO | Read as 8'h10 to indicate that these are PCI express enhanced capability registers. | No | 10h |
| 15:8 | Next Item Pointer | RO | Pointer points to the SSID/SSVID Extended Capability Structure. | Yes | A4h |
| 19:16 | Capability Version | RO | Read as 4'h2 to indicate the device is compliant to Revision .2.0 of <i>PCI Express Base Specifications</i> . | No | 2h |
| 23:20 | Device/Port Type | RO | Indicates the type of PCI Express logical device. | No | 0h |
| 24 | Slot Implemented | RO | Reset to 1'b0. | No | 0 |
| 29:25 | Interrupt Message Number | RO | Read as 5'd0. No MSI messages are generated in the transparent mode. | No | 00_000b |
| 31:30 | Reserved | RsvdP | Not Support. | No | 00b |

8.5.25 DEVICE CAPABILITIES REGISTER – OFFSET 6Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|-------|---------------------------------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|---------|
| 2:0 | Max_Payload_Size Supported | RO | Indicates the maximum payload size that the device can support for TLPs. Each port of the Switch supports 256 bytes max payload size. | Yes | 001b |
| 4:3 | Phantom Functions Supported | RO | Indicates the support for use of unclaimed function numbers as Phantom functions. Read as 00b, since the Switch does not act as a requester. | No | 00b |
| 5 | Extended Tag Field Supported | RO | Indicates the maximum supported size of Tag field as a Requester. Read as 0, since the Switch does not act as a requester. | No | 0 |
| 8:6 | Endpoint L0s Acceptable Latency | RO | Acceptable total latency that an Endpoint can withstand due to the transition from L0s state to the L0 state. For Switch, the ASPM software would not check this value. | No | 111b |
| 11:9 | Endpoint L1 Acceptable Latency | RO | Acceptable total latency that an Endpoint can withstand due to the transition from L1 state to the L0 state. For Switch, the ASPM software would not check this value. | No | 111b |
| 14:12 | Reserved | RsvdP | Not Support. | No | 000b |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|-------|---------------------------------|-------|-----------------------------------------------------------------------------------------------------------------|----------------|---------|
| 15 | Role_Based Error Reporting | RO | When set, indicates that the device implements the functionality originally defined in the Error Reporting ECN. | Yes | 1 |
| 17:16 | Reserved | RsvdP | Not Support. | No | 00b |
| 25:18 | Captured Slot Power Limit Value | RO | These bits are hardwired to 00h. | No | 00h |
| 27:26 | Captured Slot Power Limit Scale | RO | These bits are hardwired to 00b. | No | 00b |
| 31:28 | Reserved | RsvdP | Not Support. | No | 0h |

8.5.26 DEVICE CONTROL REGISTER – OFFSET 70h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|-------|--------------------------------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|---------|
| 0 | Correctable Error Reporting Enable | RW | 0b: Disable Correctable Error Reporting 1b: Enable Correctable Error Reporting | No/Yes | 0 |
| 1 | Non-Fatal Error Reporting Enable | RW | 0b: Disable Non-Fatal Error Reporting 1b: Enable Non-Fatal Error Reporting | No/Yes | 0 |
| 2 | Fatal Error Reporting Enable | RW | 0b: Disable Fatal Error Reporting 1b: Enable Fatal Error Reporting | No/Yes | 0 |
| 3 | Unsupported Request Reporting Enable | RW | 0b: Disable Unsupported Request Reporting 1b: Enable Unsupported Request Reporting | No/Yes | 0 |
| 4 | Enable Relaxed Ordering | RO | When set, it permits the device to set the Relaxed Ordering bit in the attribute field of transaction. Since the Switch can not either act as a requester or alter the content of packet it forwards, this bit always returns '0' when read. | No | 0 |
| 7:5 | Max_Payload_Size | RW | This field sets maximum TLP payload size for the device. Permissible values that can be programmed are indicated by the Max_Payload_Size Supported in the Device Capabilities register. Any value exceeding the Max_Payload_Size Supported written to this register results into clamping to the Max_Payload_Size Supported value. | No/Yes | 000b |
| 8 | Extended Tag Field Enable | RsvdP | Not Supported. | No | 0 |
| 9 | Phantom Function Enable | RsvdP | Not Supported. | No | 0 |
| 10 | Auxiliary (AUX) Power PM Enable | RsvdP | Not Supported. | No | 0 |
| 11 | Enable No Snoop | RsvdP | Not Supported. | No | 0 |
| 14:12 | Max_Read_Request_Size | RO | This field sets the maximum Read Request size for the device as a Requester. Since the Switch does not generate read request by itself, these bits are hardwired to 3'b0. | No | 000b |
| 15 | Reserved | RsvdP | Reset to 1'b0. | No/No | 0 |

8.5.27 DEVICE STATUS REGISTER – OFFSET 70h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|-----|------------------------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|---------|
| 16 | Correctable Error Detected | RW1C | Asserted when correctable error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. | No/Yes | 0 |
| 17 | Non-Fatal Error Detected | RW1C | Asserted when non-fatal error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. | No/Yes | 0 |
| 18 | Fatal Error Detected | RW1C | Asserted when fatal error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. | No/Yes | 0 |
| 19 | Unsupported Request Detected | RW1C | Asserted when unsupported request is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. | No/Yes | 0 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/I2C | DEFAULT |
|-------|----------------------|-------|-----------------------------------------------------------------------------------------------------------|------------|---------|
| 20 | AUX Power Detected | RO | Asserted when the AUX power is detected by the Switch | No | 0 |
| 21 | Transactions Pending | RO | Each port of Switch does not issue Non-posted Requests on its own behalf, so this bit is hardwired to 0b. | No | 0 |
| 31:22 | Reserved | RsvdP | Not Support. | No | 0-0h |

8.5.28 LINK CAPABILITIES REGISTER – OFFSET 74h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/I2C | DEFAULT |
|-------|----------------------------------------------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|---------------------------------------|
| 3:0 | Maximum Link Speed | RO | Read as 4'b0010 to indicate the maximum speed of the Express link is 5Gb/s and 2.5 Gb/s. | No | 2h |
| 9:4 | Maximum Link Width | HWInt RO | Indicates the maximum width of the given PCIe Link. 00_0001b: x1 link 00_0010b: x2 link 00_0100b: x4 link 00_1000b: x8 link Others: Reserved | No | 08h, 04h, 02h or 01h |
| 11:10 | Active State Power Management (ASPM) Support | RO | Indicates the level of ASPM supported on the given PCIe Link. Each port of Switch supports L0s and L1 entry. | Yes | 01b |
| 14:12 | L0s Exit Latency | RO | Indicates the L0s exit latency for the given PCIe Link. The length of time this port requires to complete transition from L0s to L0 is in the range of 256ns to less than 512ns. | Yes | 011b |
| 17:15 | L1 Exit Latency | RO | Indicates the L1 exit latency for the given PCIe Link. The length of time this port requires to complete transition from L1 to L0 is less than 1us. | Yes | 000b |
| 18 | Clock Power Management | RO | This bit must be hardwired to 0b. | Yes | 1 |
| 19 | Surprise Down Capability Enable | RsvdP | Not Support. | No | 0 |
| 20 | Data Link Layer Active Reporting Capable | RsvdP | Not Support. | No | 0 |
| 21 | Link BW Notify Capability | RsvdP | Not Support. | No | 0 |
| 23:20 | Reserved | RsvdP | Not Support. | No | 0-0h |
| 31:24 | Port Number | RO | Indicates the NT-Port Number. | Yes | 00h... port 0 01h... port 1 ... |

8.5.29 LINK CONTROL REGISTER – OFFSET 78h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/I2C | DEFAULT |
|-----|----------------------------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|---------|
| 1:0 | Active State Power Management (ASPM) Control | RW | 00b: ASPM is Disabled 01b: L0s Entry Enabled 10b: L1 Entry Enabled 11b: L0s and L1 Entry Enabled Note that the receiver must be capable of entering L0s even when the field is disabled | No/Yes | 00b |
| 2 | Reserved | RsvdP | Reset to 1'b0. | No | 0 |
| 3 | Read Completion Boundary (RCB) | RO | Does not apply to PCI Express Switch. Returns '0' when read. | No | 0 |
| 4 | Link Disable | RsvdP | Not Supported. | No | 0 |
| 5 | Retrain Link | RsvdP | Not Supported. | No | 0 |

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|-------|--------------------------------------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|---------|
| 6 | Common Clock Configuration | RW | 0b: The components at both ends of a link are operating with synchronous reference clock. 1b: The components at both ends of a link are operating with a distributed common reference clock | No/Yes | 0 |
| 7 | Extended Synch | RW | When set, it transmits 4096 FTS ordered sets in the L0s state for entering L0 state and transmits 1024 TS1 ordered sets in the L1 state for entering L0 state. | No/Yes | 0 |
| 8 | Enable Clock Power Management | RsvdP | Not Support. | No/Yes | 0 |
| 9 | HW Autonomous Width Disable | RW | Reset to 1'b0. | No/Yes | 0 |
| 10 | Link Bandwidth Management Interrupt Enable | RW | Reset to 1'b0. | No/Yes | 0 |
| 11 | Link Autonomous Bandwidth Interrupt Enable | RW | Reset to 1'b0. | No/Yes | 0 |
| 15:12 | Reserved | RsvdP | Not Support. | No | 00h |

8.5.30 LINK STATUS REGISTER – OFFSET 78h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|-------|----------------------------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|----------|
| 19:16 | Link Speed | RO | Indicate the negotiated speed of the Express link. Read as 4'b0001 is 2.5 Gb/s. Read as 4'b0010 is 5.0 Gb/s | No | 1h |
| 25:20 | Negotiated Link Width | RO | Indicates the negotiated width of the given PCIe link. | No | 00_0001b |
| 26 | Training Error | RsvdP | Not Supported. | No | 0 |
| 27 | Link Training | RsvdP | Not Supported. | No | 0 |
| 28 | Slot Clock Configuration | RO | 0b: the Switch uses an independent clock corresponsive of the presence of a reference on the connector 1b: the Switch uses the same reference clock that the platform provides on the connector | Yes | 1 |
| 29 | Data Link Layer Link Active | RsvdP | Not Support. | No | 0 |
| 30 | Link Bandwidth Management Status | RO | Reset to 1'b0. | No | 0 |
| 31 | Link Autonomous Bandwidth Status | RO | Reset to 1'b0. | No | 0 |

8.5.31 LINK CONTROL REGISTER 2 – OFFSET 98h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|-------|-----------------------------------|-------|-------------------|----------------|---------|
| 3:0 | Target Link Speed | RW | Reset to 4'b0010. | No/Yes | 2h |
| 4 | Enter Compliance | RW | Reset to 1'b0. | No/Yes | 0 |
| 5 | Hardware Autonomous Speed Disable | RW | Not Supported. | No/Yes | 0 |
| 6 | Selectable De-Emphasis | RsvdP | Not Supported. | No | 0 |
| 9:7 | Tran Margin | RW | Test used only. | No/Yes | 000b |
| 10 | Enter Modify Compliance | RW | Test used only. | No/Yes | 0 |
| 11 | Compliance SOS | RW | Test used only. | No/Yes | 0 |
| 12 | Compliance Deemp | RW | Test used only. | No/Yes | 0 |
| 15:13 | Reserved | RsvdP | Not Support. | No | 000b |

8.5.32 LINK STATUS REGISTER 2 – OFFSET 98h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|-------|---------------------------|------|------------------------|----------------|---------|
| 16 | Current De-emphasis level | RO | 0b: -6dB 1b: -3.5dB | No | 0 |
| 31:17 | Link status 2 | RO | Reset to 15'd0. | No | 0-0h |

8.5.33 SSID/SSVID CAPABILITIES REGISTER – OFFSET A4h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|-------|----------------------------|-------|---------------------------------------------------------------------------|----------------|---------|
| 7:0 | SSID/SSVID Capabilities ID | RO | Read as 8'h0D to indicate that these are SSID/SSVID capability registers. | No | 0Dh |
| 15:8 | Next Item Pointer | RO | Point to Vendor Specific Capability structure. | Yes | C8h |
| 31:16 | Reserved | RsvdP | Not Support. | No | 0000h |

8.5.34 SUBSYSTEM VENDOR ID REGISTER – OFFSET A8h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|------|----------|------|----------------------------------------|----------------|---------|
| 15:0 | SSVID | RO | It indicates the sub-system vendor id. | Yes | 12D8h |

8.5.35 SUBSYSTEM ID REGISTER – OFFSET A8h

| BIT | FUNCTION | TYPE | DESCRIPTION | EEPROM/ I2C | DEFAULT |
|-------|----------|------|----------------------------------------|----------------|---------|
| 31:16 | SSID | RO | It indicates the sub-system device id. | Yes | 1224h |

8.6 DMA ENGINE INTERFACE REGISTERS

To enable DMA function, the packet switch defines a set of interface registers for software to control the DMA engine and monitor the status of DMA transfer. There are two DMA engines (DMA_UP and DMA_NT) facing different CPU domains respectively, so it exists an independent interface for software to access its own registers in each CPU domain. The interface registers contain one global control DMA register, descriptor ownership registers shared by channels and per-channel control/status registers etc.

The interface registers are mapped to a dedicated 256-byte register block in Memory mode. The register block can be accessed by the DMA Memory Base Address, which is obtained by DMA Base Address Register 0 (Func1, CFG offset 10h).

Table 8-14 DMA Base Address in Memory Mode when NT function is enabled

| DMA Engine | DMA Memory Base Address |
|------------------------|--------------------------------|
| DMA_UP for channel 0/1 | BAR0 in the Virtual IF + 0000h |
| DMA_NT for channel 0/1 | BAR0 in the Link IF + 0000h |

Table 8-15 DMA Base Address in Memory Mode when NT function is disabled

| DMA Engine | DMA Memory Base Address |
|------------------------|-------------------------|
| DMA_UP for channel 0/1 | BAR0 + 0000h |
| DMA_UP for channel 2/3 | BAR0 + 0100h |

Following is a summary of addressing map for interface registers. Please note that the max. length for read/write register only supports 4 bytes.

| 31 – 24 | 23 – 16 | 15 – 8 | 7 – 0 | BYTE OFFSET |
|-----------------------------------------------------------------|---------|--------------------------------|-------|-------------|
| Global DMA Status | | Global DMA Control | | 00h |
| Descriptor Ownership 0 | | | | 04h |
| Descriptor Ownership 1 | | | | 08h |
| Descriptor Ownership 2 | | | | 0Ch |
| Descriptor Ownership 3 | | | | 10h |
| Reserved | | | | 14h ~ 20h |
| Channel 0 Descriptor Ring Base Pointer (Low 32-bit) | | | | 24h |
| Channel 0 Descriptor Ring Base Pointer (High 32-bit) | | | | 28h |
| Channel 0 Descriptor Current Pointer (offset from Base Pointer) | | | | 2Ch |
| Channel 0 Transfer Count Status of Descriptor Current Pointer | | | | 30h |
| Channel 0 Prefetch Upper Limit | | Channel 0 Descriptor Ring Size | | 34h |
| Channel 0 DMA Status | | Channel 0 DMA Control | | 38h |
| Channel 1 Descriptor Ring Base Pointer (Low 32-bit) | | | | 3Ch |
| Channel 1 Descriptor Ring Base Pointer (High 32-bit) | | | | 40h |
| Channel 1 Descriptor Current Pointer (offset from Base Pointer) | | | | 44h |
| Channel 1 Transfer Count Status of Descriptor Current Pointer | | | | 48h |
| Channel 1 Prefetch Upper Limit | | Channel 1 Descriptor Ring Size | | 4Ch |
| Channel 1 DMA Status | | Channel 1 DMA Control | | 50h |

8.6.1 GLOBAL DMA CONTROL AND STATUS REGISTER – OFFSET 00h

| BIT | FUNCTION | TYPE | DESCRIPTION | DEFAULT |
|-----|---------------------------------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 0 | No Snooping Mode | RW | Configuration of No Snooping. 0b: Disable no snooping 1b: Enable no snooping | 0 |
| 1 | Address Format | RW | Indicate the addressing system a DMA engine is riding on. 0b: 32-bit addressing system 1b: 64-bit addressing system | 0 |
| 3:2 | DMA Channel 0 Mapping | RW | Mapping the channel number of another DMA engine to the channel 0 of current DMA engine. This field has to be programmed for inter-processor domain data transfer model. 00b: No Mapping (For DMA_UP, it means data transfer just occurring in Upstream port CPU domain. But for DMA_NT, it represents a test mode.) 01b: Mapping to remote channel 0 10b: Mapping to remote channel 1 11b: Reserved. When mapping value is not zero the other DMA shall be relative | 00b |
| 5:4 | DMA Channel 1 Mapping | RW | Mapping the channel number of another DMA engine to the channel 1 of current DMA engine. This field has to be programmed for inter-processor domain data transfer model. 00b: No Mapping (For DMA_UP, it means data transfer just occurring in Upstream port CPU domain. But for DMA_NT, it represents a test mode.) 01b: Mapping to remote channel 0 10b: Mapping to remote channel 1 11b: Reserved. When mapping value is not zero the other DMA shall be relative | 00b |
| 9:6 | Descriptor Channel Ownership | RW | Assignment of descriptor ownership registers located from offset 04H to 10H for either channel 0 or channel 1. 1b: the ownership register is assigned to channel 1 0b: the ownership register is assigned to channel 0 Descriptor Channel Ownership register [3:0] is corresponding to descriptor ownership registers from #3 to #0. | Ch |
| 10 | Remote Channel 0 DMA Stop Interrupt Enable | RW | Enable Interrupt when Remote DMA engine is stopped. | 0 |
| 11 | Remote Channel 0 DMA Pause Interrupt Enable | RW | Enable Interrupt when Remote DMA engine is paused. | 0 |
| 12 | Remote Channel 0 DMA Abort Interrupt Enable | RW | Enable Interrupt when Remote DMA engine is aborted. | 0 |
| 13 | Remote Channel 1 DMA Stop Interrupt Enable | RW | Enable Interrupt when Remote DMA engine is stopped. | 0 |
| 14 | Remote Channel 1 DMA Pause Interrupt Enable | RW | Enable Interrupt when Remote DMA engine is paused. | 0 |

| BIT | FUNCTION | TYPE | DESCRIPTION | DEFAULT |
|-------|---------------------------------------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15 | Remote Channel 1 DMA Abort Interrupt Enable | RW | Enable Interrupt when Remote DMA engine is aborted. | 0 |
| 16 | ECRC Check Enable | RW | If configuration of ECRC check is enable the value is available. | 0 |
| 17 | ECRC Generate Enable | RW | If configuration of ECRC generate is enable the value is available | 0 |
| 22:18 | Reserved | RsvdP | Not Support. | 0_0000b |
| 23 | Packet Error | RW1C | Internal packer error indicates non-complete packet. | 0 |
| 24 | Remote Channel 0 DMA Run Status | RO | Indicates the Remote DMA engine running status. 1b: the Remote DMA engine is started and running 0b: the Remote DMA is in “stopped” condition | 0 |
| 25 | Remote Channel 0 DMA Pause Done Status | RO | Indicates the Remote DMA engine is in “Paused” condition. | 0 |
| 26 | Remote Channel 0 DMA Abort Done Status | RO | Indicates the Remote DMA engine is in “Aborted” condition. | 0 |
| 27 | Remote Channel 1 DMA Run Status | RO | Indicates the Remote DMA engine running status. 1b: the Remote DMA engine is started and running 0b: the Remote DMA is in “stopped” condition | 0 |
| 28 | Remote Channel 1 DMA Pause Done Status | RO | Indicates the Remote DMA engine is in “Paused” condition. | 0 |
| 29 | Remote Channel 1 DMA Abort Done Status | RO | Indicates the Remote DMA engine is in “Aborted” condition. | 0 |
| 30 | ECRC Error | RW1C | Indicates ECRC is error. | 0 |
| 31 | CPLD Abort | RW1C | Completion abort asserted. | 0 |

8.6.2 DESCRIPTOR OWNERSHIP REGISTER 0/1/2/3 – OFFSET 04h/08h/0Ch/10h

| BIT | FUNCTION | TYPE | DESCRIPTION | DEFAULT |
|------|----------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|
| 31:0 | Descriptor Ownership | RW | Indicate the ownership of descriptor. That means the owner can access the buffer pointed by the address field of descriptor. 1b: the DMA engine owns the descriptor 0b: the DMA driver owns the descriptor After the buffer prepared by DMA driver, it will write “1” to the corresponding descriptor ownership bit. After the descriptor is done, the DMA engine will clear the corresponding bit to “0”. | 0000_000h |

8.6.3 CHANNEL 0/1 DESCRIPTOR RING BASE POINTER (LOW 32-bit) REGISTER – OFFSET 24h/3Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | DEFAULT |
|------|-------------------------------------------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|
| 5:0 | Reserved | RsvdP | Not Support. | 00_0000b |
| 31:6 | Descriptor Ring Base Pointer (Low 32-bit) | RW | Lower 32-bit of Base Pointer referring to the 1 st entry of descriptor ring. It tells DMA engine where the descriptor is starting at. The base pointer is in 64-bit alignment. | 000_0000h |

8.6.4 CHANNEL 0/1 DESCRIPTOR RING BASE POINTER (HIGH 32-bit) REGISTER – OFFSET 28h/40h

| BIT | FUNCTION | TYPE | DESCRIPTION | DEFAULT |
|------|--------------------------------------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|
| 5:0 | Reserved | RsvdP | Not Support. | 00_0000b |
| 31:6 | Descriptor Ring Base Pointer (High 32-bit) | RW | Upper 32-bit of Base Pointer referring to the 1st entry of descriptor ring if 64-bit addressing system is used. It tells DMA engine where the descriptor is starting at. | 000_0000h |

8.6.5 CHANNEL 0/1 DESCRIPTOR CURRENT POINTER REGISTER – OFFSET 2Ch/44h

| BIT | FUNCTION | TYPE | DESCRIPTION | DEFAULT |
|-------|-------------------------------------------------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 11:0 | Descriptor Current Pointer (Offset from Base Pointer) | RO | Indicating the current pointer (Offset from Base Pointer) referring to the descriptor that is under processing by DMA Engine. A maximum of 128 pointers are allowed. | 000h |
| 31:12 | Reserved | RsvdP | Not Support. | 0_0000h |

8.6.6 CHANNEL 0/1 TRANSFER COUNT STATUS of DESCRIPTOR CURRENT POINTER REGISTER – OFFSET 30h/48h

| BIT | FUNCTION | TYPE | DESCRIPTION | DEFAULT |
|-------|-----------------------|-------|-----------------------------------------------------------------------------------------------|----------|
| 23:0 | Transfer Count Status | RO | Indicating how many byte counts have been not transferred for the current descriptor pointer. | 0000_00h |
| 31:24 | Reserved | RsvdP | Not Support. | 00h |

8.6.7 CHANNEL 0/1 DESCRIPTOR RING SIZE AND PREFETCH UPPER LIMIT REGISTER – OFFSET 34h/4Ch

| BIT | FUNCTION | TYPE | DESCRIPTION | DEFAULT |
|-------|----------------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 7:0 | Descriptor Ring Size | RW | It represents the quantity of descriptors in the ring. The size of ring must be greater than or equal to Prefetch Upper Limit. The sum of two channels of descriptor ring size cannot be larger than 128. | 02h |
| 11:8 | Prefetch Upper Limit | RW | It represents the maximum number of prefetch-able descriptors for this channel. Only the value with a multiple of 4 or 1 can be set into this register. Any value other than these will be rounded to the nearest of multiple of 4 or 1. When the programmed limit is reached, the descriptor prefetching is stopped, and restarted again after the value drops below the limit. For a value of 1, only one descriptor is prefetched (Note: When that one descriptor is active, a second descriptor is prefetched). For a value of 4N, four descriptors are prefetched (Note: When the 4 th descriptor is active, another four descriptors are prefetched). Due to different descriptor length stored in the same queue, the maximum allowable prefetch upper limit is various among different addressing system or DMA engines. For DMA_UP in 32-bit address, the prefetch upper limit is 13. For DMA_UP in 64-bit address, the prefetch upper limit is 8. For DMA_NT in 32-bit address, the prefetch upper limit is 13. For DMA_NT in 64-bit address, the prefetch upper limit is 8. | 1h |
| 15:12 | Reserved | RsvdP | Not Support. | 0h |

| BIT | FUNCTION | TYPE | DESCRIPTION | DEFAULT |
|-------|-----------------------------|------|-------------------|---------|
| 31:16 | Fetch Data Gap Time Control | RW | 16bits – per 4ns. | 0000h |

8.6.8 CHANNEL 0/1 DMA CONTROL AND STATUS REGISTER – OFFSET 38h/50h

| BIT | FUNCTION | TYPE | DESCRIPTION | DEFAULT |
|-------|----------------------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 0 | DMA Start | RW | Start DMA Engine. 1b: the DMA engine starts to fetch and process the descriptors except the DMA abort or pause status is on. 0b: the current pointer will be moved to the descriptor ring base pointer and stop the DMA engine. It can only set stop when abort or ownership is empty. | 0 |
| 1 | DMA Pause Control | RW | Pause DMA Engine. When set, the DMA engine is paused to the next active descriptor after completing the processing on current descriptor. It means that no more descriptors are processed and prefetched until the “Paused” condition is lifted. Remote end firstly shall stop or pause and run status (offset 0x00 bit 27 or bit 24) or pause done status (offset 0x00 bit 28 or bit 25) has been asserted if local pause set. If pause interrupt is enable and pause control is enable the interrupt is asserted until pause interrupt or control is disable | 0 |
| 2 | DMA Abort Control | RW | Abort DMA Engine. When set, the DMA engine drops the current active descriptor by flushing out all outstanding read commands and discarding all received completion data. The pointer does not move to the next active descriptor. No more descriptors are processed and prefetched until the “Aborted” condition is lifted. All receiving data will be discarded if DMA abort asserted. Removing abort condition can only use DMA start disable If abort interrupt is enable and abort control is enable the interrupt is asserted until abort interrupt or control is disable. | 0 |
| 3 | DMA Pause Interrupt Enable | RW | Enable Interrupt when DMA engine is paused. | 0 |
| 4 | DMA Ring Stop Mode | RW | Notify DMA Engine how to run through descriptor ring. 0b: it continues to run over the end of descriptor ring 1b: it stops at descriptor ring base pointer when the last descriptor of ring is done | 0 |
| 5 | Ownership Flash | RW | Clear ownership register. | 0 |
| 6 | DMA Abort Interrupt Enable | RW | Enable Interrupt when DMA engine is abort. | 0 |
| 15:7 | Reserved | RsvdP | Not Support. | 000h |
| 16 | DMA Pause Done Status | RO | Indicates the DMA engine is in “Paused” condition. Removing pause done status can use DMA Pause control. | 0 |
| 17 | DMA Abort Done Status | RO | Indicates the DMA engine is in “Aborted” condition. Removing abort done status can only use stop. | 0 |
| 18 | Reserved | RsvdP | Not Support. | 0 |
| 19 | Completer Status Error | RW1C | Error condition: unsupported request, completer abort. | 0 |
| 30:20 | Reserved | RsvdP | Not Support. | 000h |
| 31 | Interrupt Flag | RW1C | Indicates the interrupt asserted. | 0 |

9 CLOCK SCHEME

The built-in Integrated Reference Clock Buffer of the PI7C9X2G1224GP supports eight reference clock outputs in 324, 424, 524 or 624 modes. The clock buffer feature can be enabled and disabled by EEPROM, I2C or SMBUS.

When set to 324, 424, 524 or 624 mode, the clock buffer is enabled by default. The clock buffer distributes a single 100MHz reference clock input to eight Reference Clock Output Pairs, REFCLKO_P[8:1] and REFCLKO_N[8:1]. The clock buffer requires 100MHz differential clock inputs through REFCLKI_P and REFCLKI_N Pins as show in Table 9-1.

Table 9-1 AC Switching and DC Electrical Characteristics for REFCLKI_P/N and REFCLKO_P/N[8:1]

| Symbol | Parameters | Min. | Typ. | Max. | Unit | Note |
|------------------------------------|----------------------------------|------|------|-----------------|------|------|
| F_{IN} | Reference Clock Frequency | | 100 | | MHz | |
| T_{rise}/ T_{fall} | Rise and Fall Time in 20-80% | 175 | | 700 | ps | 2 |
| $\Delta T_{rise}/ \Delta T_{fall}$ | Rise and Fall Time Variation | | | 125 | ps | 2 |
| T_{pd} | Propagation Delay | 2.5 | | 6.5 | ns | |
| V_{HIGH} | Voltage High including overshoot | 660 | | 1150 | mV | 2 |
| V_{LOW} | Voltage Low including undershoot | -300 | | $V_{HIGH}-0.5V$ | mV | 2 |
| V_{cross} | Absolute crossing point voltage | 250 | | 550 | mV | 2 |
| V_{swing} | Voltage including overshoot | 550 | | 1800 | mV | 2, 4 |
| T_{DC} | Duty Cycle | 45 | | 55 | % | 3 |

Note:

1. Test configuration is $R_s=33.2\Omega$, $R_p=49.9\Omega$, and 2pF.
2. Measurement taken from Single Ended waveform.
3. Measurement taken from Differential waveform.
4. If the reference clock input is HCSL type, it should use DC coupling; if not in HCSL protocol (ex: LVPECL, LVDS, etc), it should be AC coupling, and refer to application note to add application circuit to rebuild dc bias. If rebuild dc bias for the best 400mV, there is no limit on the V_{swing} . However, there have two exceptions can be accepted:
 - a. If input is LVPECL, use ac-coupling and no rebuild dc bias, the min V_{swing} is 550mV (single ended).
 - b. If input is LVDS with 100 ohm cross at the inputs and use dc-coupling, the min V_{swing} is 250mV (single ended).

When set to 1124 or 1224 mode, the clock buffer is in power down mode and disabled by default. The 100MHz Reference Clock Output Pairs are disabled, and The PI7C9X2G1224GP requires 100MHz differential clock inputs through REFCLKP and REFCLKN Pins as shown in Table 9-2.

Table 9-2 AC Switching and DC Electrical Characteristics for REFCLKP/N

| Symbol | Parameters | Min. | Typ. | Max. | Unit | Note |
|------------------------------------|---------------------------------------------------------------------|------|------|------|--------|------|
| F_{IN} | Reference Clock Frequency | | 100 | | MHz | 1, 2 |
| A_j | Accuracy | -300 | | +300 | ppm | 3 |
| $T_{REFCLK-HF-RMS}$ | > 1.5 MHz to Nyquist RMS jitter after applying PCIe filter function | | | 3.1 | ps RMS | 3 |
| $T_{REFCLK-LF-RMS}$ | 10 kHz - 1.5 MHz RMS jitter | | | 3.0 | ps RMS | 3 |
| SSC_{freq} | Spread Spectrum Clock frequency | 30 | | 33 | kHz | 3 |
| T_{rise}/ T_{fall} | Rise and Fall Time in 20-80% | 175 | | 700 | ps | 2 |
| $\Delta T_{rise}/ \Delta T_{fall}$ | Rise and Fall Time Variation | | | 125 | ps | 2 |
| T_{pd} | Propagation Delay | 2.5 | | 6.5 | ns | |
| V_{HIGH} | Voltage High including overshoot | 0.8 | | | V | 2 |
| V_{LOW} | Voltage Low including undershoot | | | 800 | mV | 2 |
| V_{swing} | Voltage including overshoot | 300 | | | mV | 2 |
| T_{DC} | Duty Cycle | 45 | | 55 | % | 3 |

Note:

1. Does not include ± 300 ppm. Only certain clock frequencies will produce valid PCI Express data.
2. Measurement taken from Single-end waveform.
3. Measurement taken from Differential waveform.
4. As PCIe PHY accept CML type reference clock source and will rebuild command mode voltage by itself, it needs add ac-coupling.

10 POWER MANAGEMENT

The PI7C9X2G1224GP supports D0, D1, D2, D3-hot, and D3-cold Power States. The PCI Express Physical Link Layer of the PI7C9X2G1224GP device supports the PCI Express Link Power Management with L0, L0s, L1, L2/L3 ready and L3 Power States.

PI7C9X2G1224GP also supports ASPM (Active State Power Management) to facilitate the link power saving.

11 POWER SEQUENCE

As long as PERST# is active, all PCI Express functions are held in reset. The main supplies ramp up to their specified levels (3.3V). Sometime during this stabilization time, the REFCLK starts and stabilizes. After there has been time (100 ms) for the power and clock to become stable, PERST# is deasserted high and the PCI Express functions can start up.

It is recommended to power up the I/O voltage (3.3V) first and then the core voltage (1.0V) or power up I/O voltage and core voltage simultaneously.

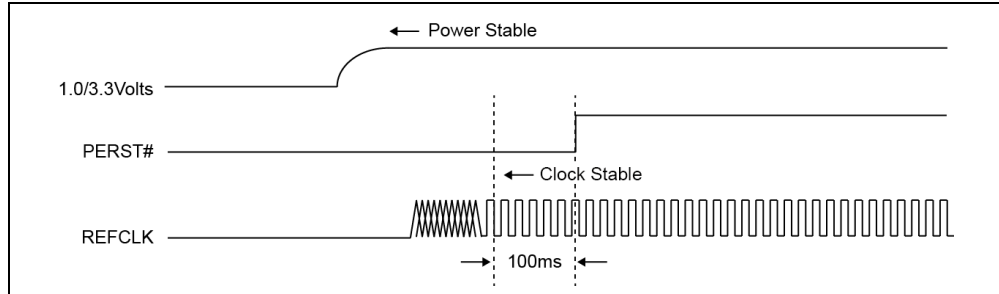


Figure 11-1 Initial Power-Up Sequence

Power-down sequence is the reverse of power-up sequence.

12 IEEE 1149.1 COMPATIBLE JTAG CONTROLLER

An IEEE 1149.1 compatible Test Access Port (TAP) controller and associated TAP pins are provided to support boundary scan in PI7C9X2G1224GP for board-level continuity test and diagnostics. The TAP pins assigned are TCK, TDI, TDO, TMS and TRST_L. All digital input, output, input/output pins are tested except TAP pins.

12.1 INSTRUCTION REGISTER

The IEEE 1149.1 Test Logic consists of a TAP controller, an instruction register, and a group of test data registers including Bypass and Boundary Scan registers. The TAP controller is a synchronous 16-state machine driven by the Test Clock (TCK) and the Test Mode Select (TMS) pins. An independent power on reset circuit is provided to ensure the machine is in TEST_LOGIC_RESET state at power-up.

PI7C9X2G1224GP implements a 5-bit Instruction register to control the operation of the JTAG logic. The defined instruction codes are shown in the following table. Those bit combinations that are not listed are equivalent to the BYPASS (11111) instruction.

Table 12-1 Instruction Register Codes

| Instruction | Operation Code (binary) | Register Selected | Operation |
|-------------|-------------------------|-------------------|-------------------------------------------------------------------------------------------|
| EXTEST | 00000 | Boundary Scan | Drives / receives off-chip test data |
| SAMPLE | 00001 | Boundary Scan | Samples inputs / pre-loads outputs |
| HIGHZ | 00101 | Bypass | Tri-states output and I/O pins except TDO pin |
| CLAMP | 00100 | Bypass | Drives pins from boundary-scan register and selects Bypass register for shifts |
| IDCODE | 01100 | Device ID | Accesses the Device ID register, to read manufacturer ID, part number, and version number |
| BYPASS | 11111 | Bypass | Selected Bypass Register |
| INT_SCAN | 00010 | Internal Scan | Scan test |
| MEM_BIST | 01010 | Memory BIST | Memory BIST test |

12.2 BYPASS REGISTER

The required bypass register (one-bit shift register) provides the shortest path between TDI and TDO when a bypass instruction is in effect. This allows rapid movement of test data to and from other components on the board. This path can be selected when no test operation is being performed on the PI7C9X2G1224GP.

12.3 DEVICE ID REGISTER

This register identifies Diodes as the manufacturer of the device and details the part number and revision number for the device.

Table 12-2 JTAG Device ID Register

| Bit | Type | Value | Description |
|-------|------|------------------|--------------------------------------------|
| 31-28 | RO | 0001 | Version number |
| 27-12 | RO | 0001011000010110 | Last 4 digits (hex) of the die part number |
| 11-1 | RO | 010001111111 | Diodes identifier assigned by JEDEC |
| 0 | RO | 1 | Fixed bit equal to 1'b1 |

12.4 BOUNDARY SCAN REGISTER

The boundary scan register has a set of serial shift-register cells. A chain of boundary scan cells is formed by connected the internal signal of the PI7C9X2G1224GP package pins. The VDD, VSS, and JTAG pins are not in the boundary scan chain. The input to the shift register is TDI and the output from the shift register is TDO. There are 4 different types of boundary scan cells, based on the function of each signal pin.

The boundary scan register cells are dedicated logic and do not have any system function. Data may be loaded into the boundary scan register master cells from the device input pins and output pin-drivers in parallel by the mandatory SAMPLE and EXTEST instructions. Parallel loading takes place on the rising edge of TCK.

12.5 JTAG BOUNDARY SCAN REGISTER ORDER

Table 12-3 JTAG Boundary Scan Register Definition

| Boundary Scan Register Number | Pin Name | Ball Location | Type | Tri-state Control Cell |
|-------------------------------|----------------|---------------|----------|------------------------|
| 0 | FATAL_ERR_L | A14 | Output3 | 1 |
| 1 | | | Control | |
| 2 | HP_PERST_C_L | B14 | Birdir | 3 |
| 3 | | | Control | |
| 4 | | | Internal | |
| 5 | | | Internal | |
| 6 | HP_ATNLED_C_L | C14 | Birdir | 7 |
| 7 | | | Control | |
| 8 | | | Internal | |
| 9 | | | Internal | |
| 10 | PORTCFG[2] | B13 | Input | |
| 11 | | | Internal | |
| 12 | UPS_PORTSEL[0] | C13 | Input | |
| 13 | | | Internal | |
| 14 | | | Internal | |
| 15 | | | Internal | |
| 16 | NT_EN_L | A3 | Input | |
| 17 | | | Internal | |
| 18 | PORTCFG[1] | B3 | Input | |
| 19 | | | Internal | |
| 20 | | | Internal | |
| 21 | | | internal | |
| 22 | NT_PORTSEL[0] | C3 | Input | |
| 23 | | | Internal | |
| 24 | | | Internal | |
| 25 | | | Internal | |
| 26 | NT_PORTSEL[1] | D3 | Input | |
| 27 | | | Internal | |
| 28 | | | Internal | |
| 29 | | | Internal | |
| 30 | SHPINT_L | E3 | Input | |
| 31 | | | Internal | |
| 32 | | | Internal | |
| 33 | | | Internal | |
| 34 | | | Internal | |
| 35 | | | Internal | |
| 36 | | | Internal | |
| 37 | | | Internal | |
| 38 | | | Internal | |
| 39 | | | Internal | |
| 40 | | | Internal | |
| 41 | | | Internal | |

| Boundary Scan Register Number | Pin Name | Ball Location | Type | Tri-state Control Cell |
|-------------------------------|----------------|---------------|----------|------------------------|
| 42 | | | Internal | |
| 43 | | | Internal | |
| 44 | | | Internal | |
| 45 | INTA L | B1 | Output3 | 46 |
| 46 | | | Control | |
| 47 | SCL I2C | C1 | Output3 | 48 |
| 48 | | | Control | |
| 49 | SDA I2C | D1 | Output3 | 50 |
| 50 | | | Control | |
| 51 | PORT_GOOD_L[1] | E1 | Output3 | 52 |
| 52 | | | Control | |
| 53 | PORT_GOOD_L[0] | F1 | Output3 | 54 |
| 54 | | | Control | |
| 55 | PORT_GOOD_L[5] | F2 | Output3 | 56 |
| 56 | | | Control | |
| 57 | I2C_ADDR[1] | F3 | Input | |
| 58 | | | Internal | |
| 59 | I2C_ADDR[0] | G1 | Input | |
| 60 | | | Internal | |
| 61 | PORT_GOOD_L[6] | G2 | Output3 | 62 |
| 62 | | | Control | |
| 63 | GPIO[4] | G3 | Birdir | 64 |
| 64 | | | Control | |
| 65 | | | Internal | |
| 66 | | | Internal | |
| 67 | I2C_ADDR[2] | G4 | Input | |
| 68 | | | Internal | |
| 69 | GPIO[7] | G5 | Output3 | 70 |
| 70 | | | Control | |
| 71 | | | Internal | |
| 72 | | | Internal | |
| 73 | HP_ATNLED_B_L | H5 | Birdir | 74 |
| 74 | | | Control | |
| 75 | | | Internal | |
| 76 | | | Internal | |
| 77 | HP_PWR_GOOD_B | N1 | Input | |
| 78 | | | Internal | |
| 79 | GPIO[2] | N2 | Birdir | 80 |
| 80 | | | Control | |
| 81 | HP_MRL_B_L | N3 | Input | |
| 82 | | | Internal | |
| 83 | | | Internal | |
| 84 | | | Internal | |
| 85 | GPIO[3] | P1 | Birdir | 86 |
| 86 | | | Control | |
| 87 | | | Internal | |
| 88 | | | Internal | |
| 89 | HP_BUTTON_B_L | R1 | Birdir | 90 |
| 90 | | | Control | |
| 91 | | | Internal | |
| 92 | | | Internal | |
| 93 | HP_PRSNT_B_L | R2 | Birdir | 94 |
| 94 | | | Control | |
| 95 | | | Internal | |
| 96 | | | Internal | |
| 97 | PERST_L | U1 | Input | |
| 98 | | | Internal | |
| 99 | | | Internal | |
| 100 | HP_PWREN_B_L | V1 | Birdir | 101 |
| 101 | | | Control | |
| 102 | | | Internal | |
| 103 | | | Internal | |
| 104 | HP_PWRFLT_B_L | P2 | Birdir | 105 |

| Boundary Scan Register Number | Pin Name | Ball Location | Type | Tri-state Control Cell |
|-------------------------------|---------------|---------------|----------|------------------------|
| 105 | | | Control | |
| 106 | | | Internal | |
| 107 | | | Internal | |
| 108 | HP PERST B L | T1 | Birdir | 109 |
| 109 | | | Control | |
| 110 | | | Internal | |
| 111 | | | Internal | |
| 112 | HP PWRLD B L | T2 | Birdir | 113 |
| 113 | | | Control | |
| 114 | DEBUG_SEL[1] | U2 | Input | |
| 115 | | | Internal | |
| 116 | | | Internal | |
| 117 | | | Internal | |
| 118 | GPIO[19] | V2 | Birdir | 119 |
| 119 | | | Control | |
| 120 | | | Internal | |
| 121 | | | Internal | |
| 122 | HP CLKEN B L | P3 | Birdir | 123 |
| 123 | | | Control | |
| 124 | GPIO[17] | R3 | Birdir | 125 |
| 125 | | | Control | |
| 126 | GPIO[18] | T3 | Birdir | 127 |
| 127 | | | Control | |
| 128 | GPIO[16] | U3 | Birdir | 129 |
| 129 | | | Control | |
| 130 | | | Internal | |
| 131 | | | Internal | |
| 132 | TESTMODE[0] | V3 | Input | |
| 133 | | | Internal | |
| 134 | | | Internal | |
| 135 | TESTMODE[1] | V13 | Input | |
| 136 | | | Internal | |
| 137 | | | Internal | |
| 138 | DEBUG_SEL[0] | U13 | Input | |
| 139 | TESTMODE[2] | T13 | Input | |
| 140 | | | Internal | |
| 141 | SWG_LVL | R13 | Input | |
| 142 | | | Internal | |
| 143 | PORTCFG[0] | P13 | Input | |
| 144 | | | Internal | |
| 145 | FAST_MODE_L | N13 | Input | |
| 146 | | | Internal | |
| 147 | SHDA_I2C | V14 | Output3 | 148 |
| 148 | | | Control | |
| 149 | NT_P2P_EN_L | U14 | Input | |
| 150 | | | Internal | |
| 151 | | | Internal | |
| 152 | | | Internal | |
| 153 | NT_RESET_L | T14 | Output3 | 154 |
| 154 | | | Control | |
| 155 | | | Internal | |
| 156 | | | Internal | |
| 157 | SHCL_I2C | R14 | Output3 | 158 |
| 158 | | | Control | |
| 159 | | | Internal | |
| 160 | | | Internal | |
| 161 | HP PWRLD A L | V15 | Birdir | 162 |
| 162 | | | Control | |
| 163 | | | Internal | |
| 164 | | | Internal | |
| 165 | HP_PWR_GOOD_A | U15 | Input | |
| 166 | | | Internal | |
| 167 | | | Internal | |

| Boundary Scan Register Number | Pin Name | Ball Location | Type | Tri-state Control Cell |
|-------------------------------|------------------|---------------|----------|------------------------|
| 168 | | | Internal | |
| 169 | HP_CLKEN_A_L | R15 | Birdir | 170 |
| 170 | | | Control | |
| 171 | | | Internal | |
| 172 | | | Internal | |
| 173 | HP_PWREN_A_L | V16 | Birdir | 174 |
| 174 | | | Control | |
| 175 | | | Internal | |
| 176 | | | Internal | |
| 177 | HP_MRL_A_L | U16 | Birdir | 178 |
| 178 | | | Control | |
| 179 | | | Internal | |
| 180 | | | Internal | |
| 181 | HP_PERST_A_L | T16 | Birdir | 182 |
| 182 | | | Control | |
| 183 | | | Internal | |
| 184 | | | Internal | |
| 185 | HP_PWRFLT_A_L | R16 | Birdir | 186 |
| 186 | | | Control | |
| 187 | HP_PRSNT_A_L | V17 | Birdir | 188 |
| 188 | | | Control | |
| 189 | HP_ATNLED_A_L | U17 | Birdir | 190 |
| 190 | | | Control | |
| 191 | HP_BUTTON_A_L | T17 | Birdir | 192 |
| 192 | | | Control | |
| 193 | GPIO[14] | V18 | Birdir | 194 |
| 194 | | | Control | |
| 195 | PORT_GOOD_L[9] | U18 | Output3 | 196 |
| 196 | | | Control | |
| 197 | GPIO[11] | T18 | Birdir | 198 |
| 198 | | | Control | |
| 199 | | | Internal | |
| 200 | | | Internal | |
| 201 | | | Internal | |
| 202 | | | Internal | |
| 203 | | | Internal | |
| 204 | GPIO[15] | R18 | Birdir | 205 |
| 205 | | | Control | |
| 206 | | | Internal | |
| 207 | | | Internal | |
| 208 | GPIO[10] | R17 | Birdir | 209 |
| 209 | | | Control | |
| 210 | SERDES_MODE_EN_L | P18 | Input | |
| 211 | | | Internal | |
| 212 | PLL_BYPASS_L | P17 | Input | |
| 213 | | | Internal | |
| 214 | PORT_GOOD_L[8] | P16 | Output3 | 215 |
| 215 | | | Control | |
| 216 | | | Internal | |
| 217 | | | Internal | |
| 218 | UPS_PORTSEL[2] | P15 | Input | |
| 219 | | | Internal | |
| 220 | UPS_PORTSEL[1] | P14 | Input | |
| 221 | | | Internal | |
| 222 | EEDO | D16 | Input | |
| 223 | | | Internal | |
| 224 | | | Internal | |
| 225 | | | Internal | |
| 226 | HP_PWR_GOOD_C | D17 | Input | |
| 227 | | | Internal | |
| 228 | | | Internal | |
| 229 | | | Internal | |
| 230 | EECS_L | C18 | Output3 | 231 |

| Boundary Scan Register Number | Pin Name | Ball Location | Type | Tri-state Control Cell |
|-------------------------------|----------------|---------------|----------|------------------------|
| 231 | | | Control | |
| 232 | EECK | C17 | Birdir | 233 |
| 233 | | | Control | |
| 234 | HP_PWRLED_C_L | D15 | Birdir | 235 |
| 235 | | | Control | |
| 236 | EEDI | C16 | Output3 | 237 |
| 237 | | | Control | |
| 238 | | | Internal | |
| 239 | | | Internal | |
| 240 | HP_CLKEN_C_L | C15 | Birdir | 241 |
| 241 | | | Control | |
| 242 | | | Internal | |
| 243 | | | Internal | |
| 244 | GPIO[13] | B18 | Birdir | 245 |
| 245 | | | Control | |
| 246 | HP_PRSNT_C_L | B17 | Birdir | 247 |
| 247 | | | Control | |
| 248 | | | Internal | |
| 249 | | | Internal | |
| 250 | | | Internal | |
| 251 | | | Internal | |
| 252 | GPIO[12] | A18 | Birdir | 253 |
| 253 | | | Control | |
| 254 | HP_PWRFLT_C_L | A17 | Birdir | 255 |
| 255 | | | Control | |
| 256 | HP_PWREN_C_L | A16 | Birdir | 257 |
| 257 | | | Control | |
| 258 | HP_BUTTON_C_L | B16 | Birdir | 259 |
| 259 | | | Control | |
| 260 | UPS_PORTSEL[3] | A15 | Input | |
| 261 | HP_MRL_C_L | B15 | Birdir | 262 |
| 262 | | | Control | |

13 ELECTRICAL AND TIMING SPECIFICATIONS

13.1 ABSOLUTE MAXIMUM RATINGS

Table 13-1 Absolute Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

| Item | Absolute Max. Rating |
|---------------------------------------------------------------------------------|----------------------|
| Storage Temperature | -65°C to 150°C |
| Junction Temperature, T _j | 125°C |
| Digital core and analog supply voltage to ground potential (VDDC and AVDD) | -0.3v to 1.2v |
| Digital I/O and analog high supply voltage to ground potential (VDDR and AVDDH) | -0.3v to 3.8v |
| Reference Clock supply voltage to ground potential (CVDDR) | -0.3v to 3.8v |
| DC input voltage for Digital I/O signals | -0.3v to 3.8v |

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

13.2 DC SPECIFICATIONS

Table 13-2 DC Electrical Characteristics

| Symbol | Description | Min. | Typ. | Max. | Unit |
|-----------------------------------|---------------------------------------|------|------|------|-------|
| VDDC | Digital Core Power | 1.0 | | 1.1 | V |
| VDDR | Digital I/O Power | 3.0 | 3.3 | 3.6 | |
| CVDDR | Reference Clock Power | 3.0 | 3.3 | 3.6 | |
| AVDD | PCI Express Analog Power | 1.0 | | 1.1 | |
| AVDDH | PCI Express Analog High Voltage Power | 3.0 | 3.3 | 3.6 | |
| V _{IH} | Input High Voltage | 2.0 | | 5.5 | |
| V _{IL} | Input Low Voltage | -0.3 | | 0.8 | Ω |
| R _{PU} | Pull-up Resistor | 63K | 92K | 142K | |
| R _{PD} | Pull-down Resistor | 57K | 91K | 159K | |
| RST# _{Slew} ¹ | PERST_L Slew Rate | 50 | | | mV/ns |

Note:

- The min. value for PERST_L Slew Rate is 50 mV/ns, which translates to the requirement that the time for PERST_L from 0V to 3.3V should be less than 50 ns.

13.3 AC SPECIFICATIONS

Table 13-3 PCI Express Interface - Differential Transmitter (TX) Output (5.0 Gbps) Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit |
|----------------------------------------------|--------------------------------|--------|-------|--------|--------|
| Unit Interval | UI | 199.94 | 200.0 | 200.06 | ps |
| Differential p-p TX voltage swing | V _{TX-DIFF-P-P} | 800 | - | - | mV ppd |
| Low power differential p-p TX voltage swing | V _{TX-DIFF-P-P-LOW} | 400 | - | - | mV ppd |
| TX de-emphasis level ratio | V _{TX-DE-RATIO-3.5dB} | -3.0 | - | -4.0 | dB |
| TX de-emphasis level ratio | V _{TX-DE-RATIO-6dB} | -5.5 | - | -6.5 | dB |
| Transmitter Eye including all jitter sources | T _{TX-EYE} | 0.75 | - | - | UI |
| TX deterministic jitter > 1.5 MHz | T _{TX-HF-DJ-DD} | - | - | 0.15 | UI |
| TX RMS jitter < 1.5 MHz | T _{TX-LF-RMS} | - | - | 3.0 | Ps RMS |
| Transmitter rise and fall time | T _{TX-RISE-FALL} | 0.15 | - | - | UI |
| TX rise/fall mismatch | T _{RF-MISMATCH} | - | - | 0.1 | UI |

| Parameter | Symbol | Min | Typ | Max | Unit |
|------------------------------------------------------------------------|-----------------------------------------|-----|-----|------------------|------|
| Maximum TX PLL Bandwidth | BW _{TX-PLL} | - | - | 16 | MHz |
| Minimum TX PLL BW for 3dB peaking | BW _{TX-PLL-LO-3DB} | 8 | - | - | MHz |
| TX PLL peaking with 8 MHz min BW | PKG _{TX-PLL1} | - | - | 3.0 | dB |
| DC Differential TX Impedance | Z _{TX-DIFF-DC} | 80 | - | 120 | Ω |
| Transmitter Short-Circuit Current Limit | I _{TX-SHORT} | - | - | 90 | mA |
| TX DC Common Mode Voltage | V _{TX-DC-CM} | 0 | - | 3.6 | V |
| Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle | V _{TX-CM-DC-ACTIVE-IDLE-DELTA} | 0 | - | 100 | mV |
| Absolute Delta of DC Common Mode Voltage between D+ and D- | V _{TX-CM-DC-LINE-DELTA} | 0 | - | 25 | mV |
| Electrical Idle Differential Peak Output Voltage | V _{TX-IDLE-DIFF-AC-P} | 0 | - | 20 | mV |
| DC Electrical Idle Differential Output Voltage | V _{TX-IDLE-DIFF-DC} | 0 | - | 5 | mV |
| The Amount of Voltage Change Allowed During Receiver Detection | V _{TX-RCV-DETECT} | - | - | 600 | mV |
| Lane-to-Lane Output Skew | L _{TX-SKEW} | - | - | 500 ps + 4 UI | ps |

Table 13-4 PCI Express Interface - Differential Transmitter (TX) Output (2.5 Gbps) Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit |
|--------------------------------------------------------------------------|------------------------------------------|--------|-------|------------------|--------|
| Unit Interval | UI | 399.88 | 400.0 | 400.12 | ps |
| Differential p-p TX voltage swing | V _{TX-DIFF-P-P} | 800 | - | - | mV ppd |
| Low power differential p-p TX voltage swing | V _{TX-DIFF-P-P-LOW} | 400 | - | - | mV ppd |
| TX de-emphasis level ratio | V _{TX-DE-RATIO} | -3.0 | - | -4.0 | dB |
| Minimum TX eye width | T _{TX-EYE} | 0.75 | - | - | UI |
| Maximum time between the jitter median and max deviation from the median | T _{TX-EYE-MEDIAN-to-MAX-JITTER} | - | - | 0.125 | UI |
| Transmitter rise and fall time | T _{TX-RISE-FALL} | 0.125 | - | - | UI |
| Maximum TX PLL Bandwidth | BW _{TX-PLL} | - | - | 22 | MHz |
| Maximum TX PLL BW for 3dB peaking | BW _{TX-PLL-LO-3DB} | 1.5 | - | - | MHz |
| Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle | V _{TX-CM-DC-ACTIVE-IDLE-DELTA} | 0 | - | 100 | mV |
| Absolute Delta of DC Common Mode Voltage between D+ and D- | V _{TX-CM-DC-LINE-DELTA} | 0 | - | 25 | mV |
| Electrical Idle Differential Peak Output Voltage | V _{TX-IDLE-DIFF-AC-P} | 0 | - | 20 | mV |
| The Amount of Voltage Change Allowed During Receiver Detection | V _{TX-RCV-DETECT} | - | - | 600 | mV |
| Transmitter DC Common Mode Voltage | V _{TX-DC-CM} | 0 | - | 3.6 | V |
| Transmitter Short-Circuit Current Limit | I _{TX-SHORT} | - | - | 90 | mA |
| DC Differential TX Impedance | Z _{TX-DIFF-DC} | 80 | 100 | 120 | Ω |
| Lane-to-Lane Output Skew | L _{TX-SKEW} | - | - | 500 ps + 2 UI | ps |

Table 13-5 PCI Express Interface - Differential Receiver (RX) Input (5.0 Gbps) Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit |
|--------------------------------------|---------------------------------|--------|-------|--------|------|
| Unit Interval | UI | 199.94 | 200.0 | 200.06 | ps |
| Differential RX Peak-to-Peak Voltage | V _{RX-DIFF-PP-CC} | 120 | - | 1200 | mV |
| Total jitter tolerance | T _{JRX} | 0.68 | - | - | UI |
| Receiver DC common mode impedance | Z _{RX-DC} | 40 | - | 60 | Ω |
| RX AC Common Mode Voltage | V _{RX-CM-AC-P} | - | - | 150 | mV |
| Electrical Idle Detect Threshold | V _{RX-IDLE-DET-DIFF-P} | 65 | - | 175 | mV |

Table 13-6 PCI Express Interface - Differential Receiver (RX) Input (2.5 Gbps) Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit |
|--------------------------------------|----------------------------|--------|-------|--------|------|
| Unit Interval | UI | 399.88 | 400.0 | 400.12 | ps |
| Differential RX Peak-to-Peak Voltage | V _{RX-DIFF-PP-CC} | 175 | - | 1200 | mV |
| Receiver eye time opening | T _{RX-EYE} | 0.4 | - | - | UI |

| Parameter | Symbol | Min | Typ | Max | Unit |
|-------------------------------------------------------------|------------------------------------------|-----|-----|-----|------|
| Maximum time delta between median and deviation from median | T _{RX-EYE-MEDIAN-to-MAX-JITTER} | - | - | 0.3 | UI |
| Receiver DC common mode impedance | Z _{RX-DC} | 40 | - | 60 | Ω |
| DC differential impedance | Z _{RX-DIFF-DC} | 80 | - | 120 | Ω |
| RX AC Common Mode Voltage | V _{RX-CM-AC-P} | - | - | 150 | mV |
| DC input CM input impedance during reset or power down | Z _{RX-HIGH-IMP-DC} | 200 | - | - | kΩ |
| Electrical Idle Detect Threshold | V _{RX-IDLE-DET-DIFFp-p} | 65 | - | 175 | mV |
| Lane to Lane skew | L _{RX-SKEW} | - | - | 20 | ns |

13.4 OPERATING AMBIENT TEMPERATURE

Table 13-7 Operating Ambient Temperature

(The Operating Ambient Temperature be associated with Chapter 14.)

| Item | Low | High | Unit |
|----------------------------------------|-----|------|------|
| Ambient Temperature with power applied | -40 | 85 | °C |

Note: Exposure to high temperature conditions for extended periods of time may affect reliability.

13.1 POWER CONSUMPTION

Table 13-8 Power Consumption

| Active Lane per Port | 1.0VDDC | | 1.0VDDA | | 3.3AVDDH | | 3.3VDDR | | 3.3CVDDR | | Total | | Unit |
|-----------------------|---------|-------|---------|-------|----------|-------|---------|-------|----------|-------|-------|------|------|
| | Typ | Max | Typ | Max | Typ | Max | Typ | Max | Typ | Max | Typ | Max | |
| 4 x4 / 8 x1 | 0.547 | 2.041 | 0.653 | 1.838 | 0.165 | 0.191 | 0.02 | 0.022 | 0 | 0 | 1.39 | 4.09 | W |
| 3 x8 | 0.681 | 1.580 | 0.649 | 1.822 | 0.165 | 0.191 | 0.02 | 0.022 | 0.561 | 0.612 | 2.08 | 4.23 | W |
| 3 x8, ec ¹ | 0.681 | 1.580 | 0.649 | 1.822 | 0.165 | 0.191 | 0.02 | 0.022 | 0 | 0 | 1.52 | 3.62 | W |

Note:

¹: Use external clock buffer, Disable internal clock buffer

Test Conditions:

- Typical power measured under the conditions of 1.0V/ 3.3V power rail without device usage on all downstream ports.
- Maximum power measured under the conditions of 1.1V/ 3.6V with PCIe2 devices usage on all downstream ports
- Ambient Temperature at 25°C
- Power consumption in the table is a reference, be affected by various environment, bus traffic and power supply etc.

14 THERMAL DATA

The information described in this section is provided for reference only.

Table 14-1 Thermal Data

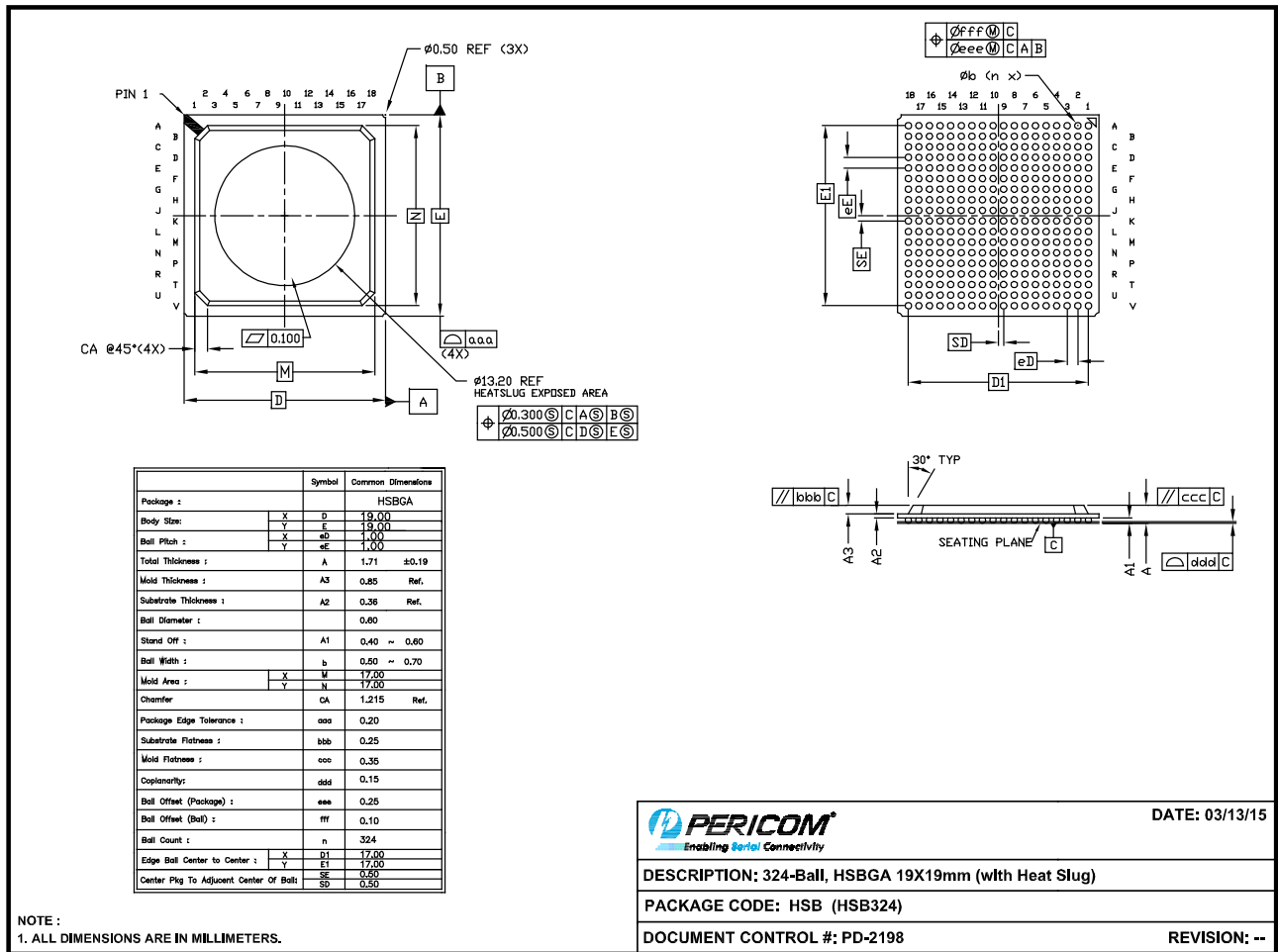
| Power (Watt) | T _a (°C) | Board | Airflow (m/s) | Θ _{JA} (°C/W) | T _j (°C) | Θ _{JB} (°C/W) | Θ _{JC} (°C/W) |
|------------------------|---------------------|---------------------------------|---------------|------------------------|---------------------|------------------------|------------------------|
| 3.72 ^{Note 6} | 85 | JEDEC 4L PCB w/o HeatSink | 0 | 15.7 | 143.40 | 5.3 | 4.4 |
| | | | 1 | 13.8 | 136.34 | | |
| | | | 2 | 12.6 | 131.87 | | |
| | | JEDEC 4L PCB with HeatSink | 0 | 15.0 | 140.80 | | |
| | | | 1 | 10.9 | 125.55 | | |
| | | | 2 | 9.6 | 120.71 | | |
| | | Customized 8L PCB w/o HeatSink | 0 | 13.6 | 135.59 | | 4.3 |
| | | | 1 | 11.7 | 128.52 | | |
| | | | 2 | 10.6 | 124.43 | | |
| | | Customized 8L PCB with HeatSink | 0 | 13.1 | 133.73 | | |
| | | | 1 | 9.6 | 120.71 | | |
| | | | 2 | 8.5 | 116.62 | | |
| 3.85 ^{Note 7} | 85 | JEDEC 4L PCB w/o HeatSink | 0 | 15.7 | 145.45 | 5.3 | 4.4 |
| | | | 1 | 13.8 | 138.13 | | |
| | | | 2 | 12.6 | 133.51 | | |
| | | JEDEC 4L PCB with HeatSink | 0 | 15.0 | 142.75 | | |
| | | | 1 | 10.9 | 126.97 | | |
| | | | 2 | 9.6 | 121.96 | | |
| | | Customized 8L PCB w/o HeatSink | 0 | 13.6 | 137.36 | | 4.3 |
| | | | 1 | 11.7 | 130.05 | | |
| | | | 2 | 10.6 | 125.81 | | |
| | | Customized 8L PCB with HeatSink | 0 | 13.1 | 135.44 | | |
| | | | 1 | 9.6 | 121.96 | | |
| | | | 2 | 8.5 | 117.73 | | |

Note:

1. T_a: Ambient Temperature
2. T_j: Junction Temperature
3. Maximum allowable junction temperature = 125°C
4. Θ_{JA}: Thermal Resistance, Junction-to-Ambient
5. Θ_{JC}: Thermal Resistance, Junction-to-Case
6. Power measured under the conditions of 1.0V/ 3.3V with PCIe2 devices usage on all downstream ports in 1224 mode
7. Power measured under the conditions of 1.0V/ 3.3V with PCIe2 devices usage on all downstream ports in 324 mode
8. The shaded fields provide a recommendation that allows PI7C9X2G1224GP to support Industrial Temperature Range
9. Customized 8L PCB Information
 PCB Type : Customized 2s6p PCB
 PCB Layers : 8
 PCB Dimension : 101.6x114.3 mm²
 PCB Thickness : 1.6 mm
 PCB Material : FR4
 Cu Trace Thickness : 0.070 mm (2oz)
 Cu Plane Thickness : 0.035 mm (1oz)
 PCB Thermal Via : 49 (7x7)
 Thermal Via Diameter : 0.33 mm
 Thermal Via Pitch : 1.00 mm
 Copper Coverage : Cu-1&8~60%, Cu-2~7~80%
10. Heat Sink Information
 Model: S1519-10W (Alpha Novatech, Inc.)
 Heat sink size – 19x19x10 mm³

15 PACKAGE INFORMATION

The package of PI7C9X2G1224GP is a 19mm x 19mm HSBGA (324 Ball) package. The following are the package information and mechanical dimension:



PERICOM
Enabling Serial Connectivity

DATE: 03/13/15

DESCRIPTION: 324-Ball, HSBGA 19X19mm (with Heat Slug)

PACKAGE CODE: HSB (HSB324)

DOCUMENT CONTROL #: PD-2198

REVISION: --

Figure 15-1 Package Outline Drawing



1st *: Part Rev
2nd *: Die Rev
YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

Figure 15-2 Part Marking

16 ORDERING INFORMATION

| Part Number | Operating Temperature | Package Code | Package Description |
|---------------------|------------------------------------------|--------------|----------------------------------|
| PI7C9X2G1224GPBHSBE | -40° to 85°C (Industrial Temperature) | HSB | 324-pin 19mmx19mm HSBGA (ULA) |

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

