A product Line of
Diodes Incorporated

PI2EQX602E

1.8V 5.0Gbps, 2-port, USB 3.0 Mux/DeMux ReDriver™

Features

- USB 3.0 compatible
- Full Compliancy to USB3.0 Super Speed Standard
- 1 to 2 DeMux from host T_X to device R_X
- 2 to 1 Mux from device T_X to Host R_X
- Pin Adjustable Receiver Equalization
- Pin Adjustable output swing
- Pin Adjustable Output Emphasis
- 100Ω Differential CML I/O's
- Input signal level detect and squelch for each channel
- Automatic Receiver Detect
- Low Power : 200mW
- Adaptive power management
  - 0.36mW/0.2mA (typ) in U2/U3 state
  - 0.36mW/0.2mA (typ) in no connection state
  - 26mW/14mA(typ) in U1 state
- Single Supply Voltage: 1.8V
- Packaging:
  - 18-Pin X2QFN 2x2.4 mm

Description

Pericom Semiconductor's PI2EQX602E is a low power, high performance 5.0 Gbps 2-Port USB3.0 Mux / DeMux ReDriver™ designed specifically for the USB 3.0 protocol.

The device provides programmable equalization, swing and De-emphasis to optimize performance over a variety of physical mediums by reducing Inter-Symbol Interference. PI2EQX602E supports two 100Ω Differential CML data I/O's between the Protocol ASIC to a switch fabric, over cable, or to extend the signals across other distant data pathways on the user's platform.

The integrated equalization circuitry provides flexibility with signal integrity of the signal before the ReDriver. A low-level input signal detection and output squelch function is provided for each channel. Each channel operates fully independently. The channels' input signal level (on xI+/-) determines whether the output is active.

The PI2EQX602E also includes an adaptive power management feature to maximize battery life for power sensitive consumer devices.

Block Diagram

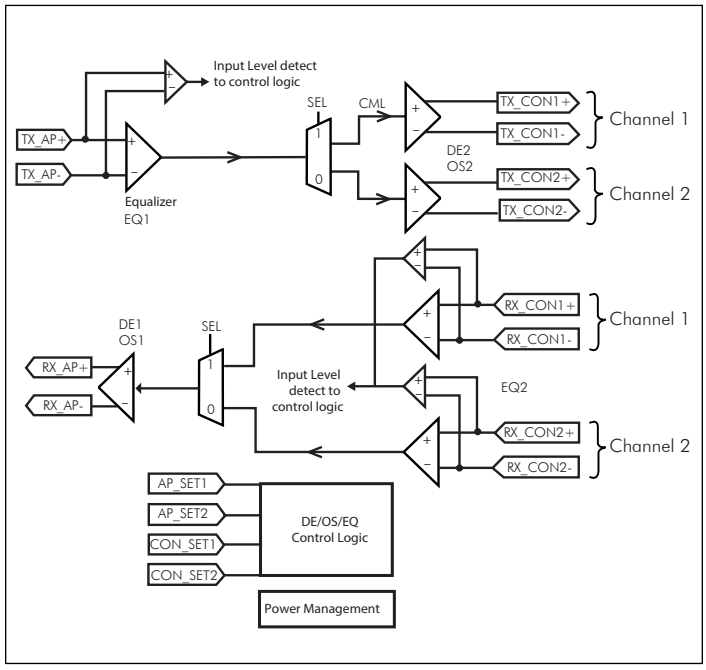
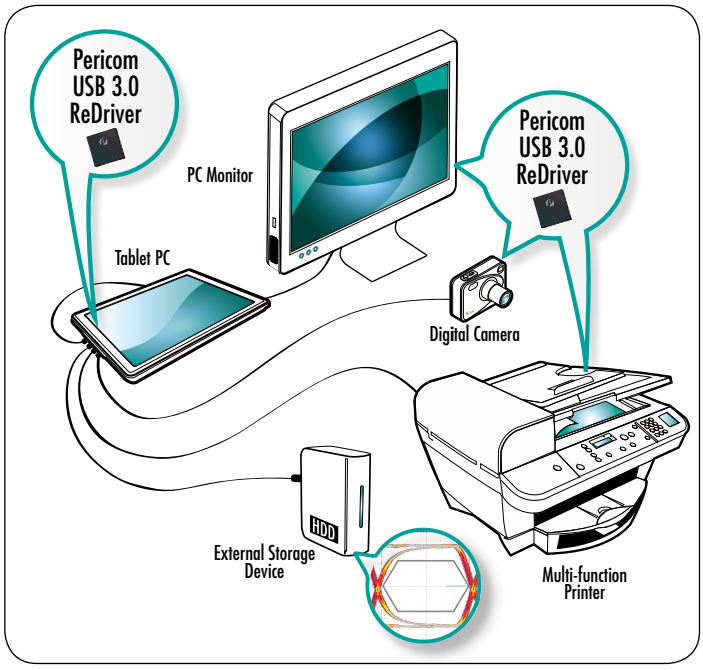
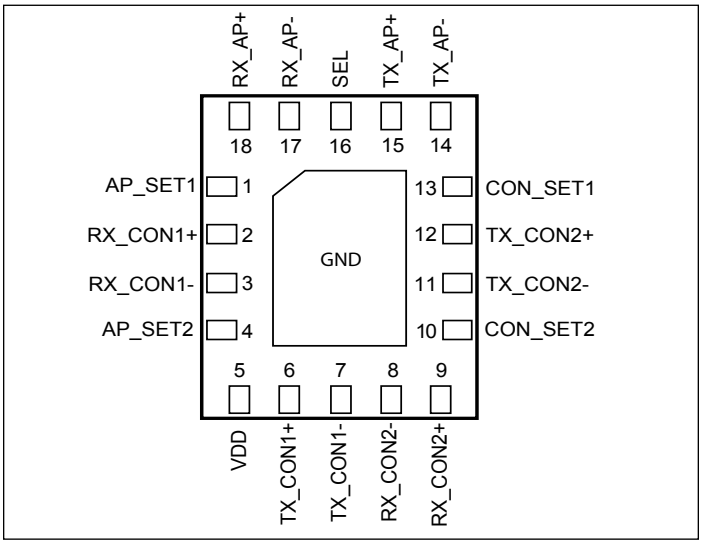


Figure1



Pin Diagram (Top Side View)



Pin Description

Pin #	Pin Name	Type	Description
5	VDD	Power	1.8V power supply, +/- 0.1V
13, 10	CON_SET1, CON_SET2	Input	Connector Side Setting: DE2/OS2/EQ2 setup. 2 x 3-level input pins. With internal 150KΩ pull-up resistor and 150kΩ pull-down resistor.
15, 14 2, 3 9, 8	TX_AP+, TX_AP- RX_CON1+, RX_CON1- RX_CON2+, RX_CON2-	Input	CML input terminals. With selectable input termination between 50Ω to internal VbiasRx or 67kΩ to GND.
18, 17 6, 7 12, 11	RX_AP+, RX_AP- TX_CON1+, TX_CON1- TX_CON2+, TX_CON2-	Output	CML output terminals. With selectable output termination between 50Ω to internal voltage bias, 2K to GND or Hi-Z
Center Pad	GND	GND	Supply Ground
1, 4	AP_SET1, AP_SET2	Input	Application Processor Side Setting: DE1/OS1/EQ1 setup. 2 x 3-level input pins. With internal 150KΩ pull-up resistor and 150kΩ pull-down resistor.
16	SEL	Input	Mode Selection Pin. 2-level input pin. With internal 300KΩ pull-down resistor. "High" – Channel 1 active "Low" – Channel 2 Active (Default)

Power Management

PI2EQX602E USB3.0 Active Switch includes an adaptive power management feature to support long battery run-time ideal for power-sensitive Smart Mobile Devices. PI2EQX602E is equipped with two differential paths, one is from application processor side to type-C connector side and the other is from type-C connector side to application processor side. Each path has 4 power modes: active mode, slumber mode, deep slumber mode and unplug mode. These power modes are managed by the adaptive power management feature according to the link status. The feature does not decode the USB3.x power management commands to obtain the link status, it relies on link electrical condition, internal timer and internal state machine. Hence, the feature can optimize the power saving in U1 (slumber mode), U2/U3 (deep slumber mode) and no connection state (Either no device is connected to the type-C connector or the receiver terminal of the connected device is in high impedance mode).

De-emphasis / Output Swing / Equalization Configuration Table for Application Processor Side:

Application Processor Side DE/OS/EQ Settings				
AP_SET1	AP_SET2	DE1	OS1	EQ1
0	0	-3.5dB	1.1V	3dB
	Float	-3.5dB	0.9V	3dB
	1	-3.5dB	1.1V	0dB
Float	0	-3.5dB	0.9V	0dB
	Float	0dB	1.1V	3dB (Default)
	1	0dB	0.9V	3dB
1	0	0dB	1.1V	0dB
	Float	0dB	0.9V	0dB
	1	-6dB	1.1V	3dB

De-emphasis / Output Swing / Equalization Configuration Table for Connector Side:

Connector Side DE/OS/EQ Settings				
CON_SET1	CON_SET2	DE2	OS2	EQ2
0	0	-3.5dB	1.1V	3dB
	Float	-3.5dB	0.9V	3dB
	1	-3.5dB	1.1V	0dB
Float	0	-3.5dB	0.9V	0dB
	Float	0dB	1.1V	3dB (Default)
	1	0dB	0.9V	3dB
1	0	0dB	1.1V	0dB
	Float	0dB	0.9V	0dB
	1	-6dB	1.1V	3dB

Unused Channel Configuration Table (single ended)

	Input R	Output R
Unused channel	67kΩ to GND	HiZ

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5V to +2V
DC SIG Voltage	–0.5V to V_{DD} +0.5V
Output Current	–25mA to +25mA
Power Dissipation Continuous	0.5W
Operating Temperature	-40°C to +85°C
ESD, Human Body Model	–2kv to +2kV

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
DEVICE PARAMETERS						
maximum date rate					5	Gbps
t_{idle_out}	Slumber mode exit time	LFPS signal		20		ns
t_{idle_in}	Slumber mode entry time	Electrical idle		1.3		ms
t_{dsm_in}	Deep Slumber mode entry time	Electrical idle		330		ms
Bi-Level Leakage						
I_{IH}	Input High Current				50	uA
I_{IL}	Input LOW Current		-50			
Tri-Level Control Pins						
V_{IH}	Input High Voltage		0.85Vdd			V
V_{IL}	Input Low Voltage				0.15Vdd	
V_{IMID}	Input Mid Voltage		0.35Vdd	0.5Vdd	0.65Vdd	
C_L	Loading Capacitance				150	pF

AC/DC Electrical Characteristics

1.8V Power Supply Characteristics						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Units**
V_{dd}	Supply voltage		1.7	1.8	1.9	V
$I_{typ\text{-}noDE}$	Active current consumption @ DE=0	5Gbps, compliance test pattern, De-emph=0dB and OS = 1.1V)		110	145	mA
$I_{typ\text{-}WithDE}$	Active current consumption @ DE= -3.5dB or -6dB	(5Gbps, compliance test pattern, De-emph=-3.5dB or -6dB and OS = 1.1V)		130	165	
I_{U1}	Current consumption @ U1	U1 Power - saving state		14	25	
$I_{U2/U3}$	Current consumption @ U2/U3	U2/U3 Power - saving state		0.2	1	
I_{unplug}	Current consumption @ Unplug	No USB connection state		0.2	1	

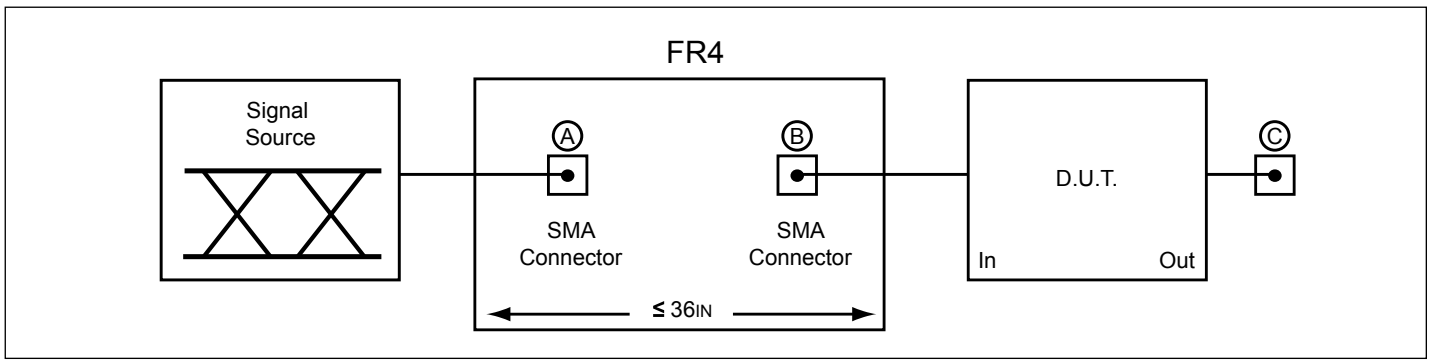
AC/DC Electrical Characteristics (Continued..)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Receiver AC/DC						
$V_{RX-DIFFP-P}$	Differential Peak-to-Peak Input Voltage	AC coupled differential RX peak to peak signal	150		1200	mVppd
V_{RX-C}	Common Mode Voltage			1		V
V_{cm_ac}	RX AC Common Mode Voltage	Measured at Rx pins with termination enabled			150	mV
Z_{CM_RX}	DC common mode impedance		18		30	Ω
Z_{diff_RX}	DC differential input impendance		70		120	
$Z_{CM\_RX\_HIZ}$	DC common mode high impedance	Device in unplug mode RX termination measured with respect to AC GND over 500mV max	25			kΩ
$RL_{RX-DIFF}$	Differential return loss	50 MHz-1.25GHz		21		dB
		1.25 GHz-2.5 GHz		13		
RL_{RX-CM}	Common mode return loss	50 MHz-2.5 GHz		7		dB
$V_{th\_U0/U1}$	Input threshold voltage in U0/U1 modes	In U0/U1 mode	50		150	mVppd
V_{th_upm}	LFPS input threshold voltage in no USB connection state	For the path that the receiver termination is not detected. (Notes: uses $V_{th\_U2/U3}$ for the path that the receiver termination is detected)	150		650	mVppd
$V_{th\_U2/U3}$	LFPS input threshold voltage in U2/U3 modes	In U2/U3 modes	150		650	
Transmitter Output AC/DC (100Ω differential)						
$V_{TX-DIFFP-P}$	Differential Peak-to-peak Output Voltage	$V_{TX-DIFFP-P} = 2 * \lvert V_{TX-D+} - V_{TX-D-} \rvert$	400		1200	mVppd
$V_{TX-LFPS}$	LFPS Differential Peak-to-peak Output Voltage		800		1200	
$V_{TX-DEFAULT}$	Default Differential Peak-to-Peak Output Voltage			1100		
V_{TX-C}	Common-Mode Voltage	$\lvert V_{TX-D+} + V_{TX-D-} \rvert /2$	0.5		1.2	V
DE	De-emphasis	DE = 0dB		0		dB
		DE = -3.5dB	-3.0	-3.5	-4.0	
		DE =-6dB		-6.0		
Z_{diff_TX}	DC differential impedance		70		120	Ω
Z_{CM_TX}	DC common mode impedance		18		30	
RL_{diff_TX}	Differential return loss	f= 50MHz-1.25 GHz		18		dB
		f= 1.25 GHz-2.5 GHz		12		
RL_{CM_TX}	Common mode return loss	f= 50 MHz-2.5GHz		9		dB
$V_{TX\_CM\_AC\_Active}$	TX AC common mode voltage active			30	100	mVpp

AC/DC Electrical Characteristics (Continued..)

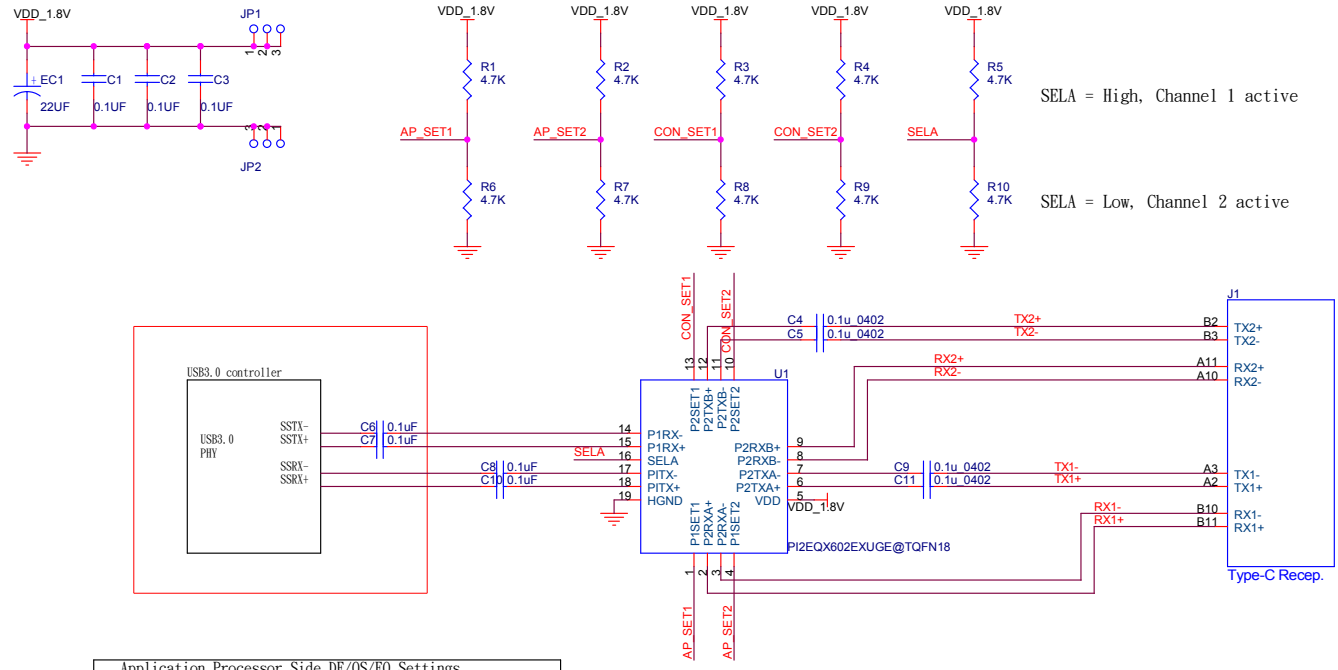
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{detect}	Voltage change to allow receiver detect	Positive voltage to sense receiver termination			600	mV
t_R,t_F	Output rise/fall time	20%-80% of differental voltage measured 1" from the output pin		60		ps
T_{diff_LH}, T_{diff_HL}	Differential propagation delay	Propagation delay between 50% level at input and output		460	1000	ps
Jitter Profile						
$T_{TX\text{-}EYE}$ (1)(2)	Total jitter(Tj)	with 36 inch of inputFR4 trace		0.2	0.5	UI(3)p-p
DJ_{TX} (2)	Deterministic jitter(Dj)			0.1	0.3	
RJ_{TX} (2)(4)	Random jitter(Rj)			0.09	0.2	

Note:
1.Includes RJ at 10^{-12} BER
2.Determininstic jitter measured with PRBS7 pattern, Random jitter measured with 1010 pattern VID=1000mVpp, 5Gbps,
3.UI = 200ps
4.Rj calculated as 14.069 times the RMS random jitter for 10^{-12} BER



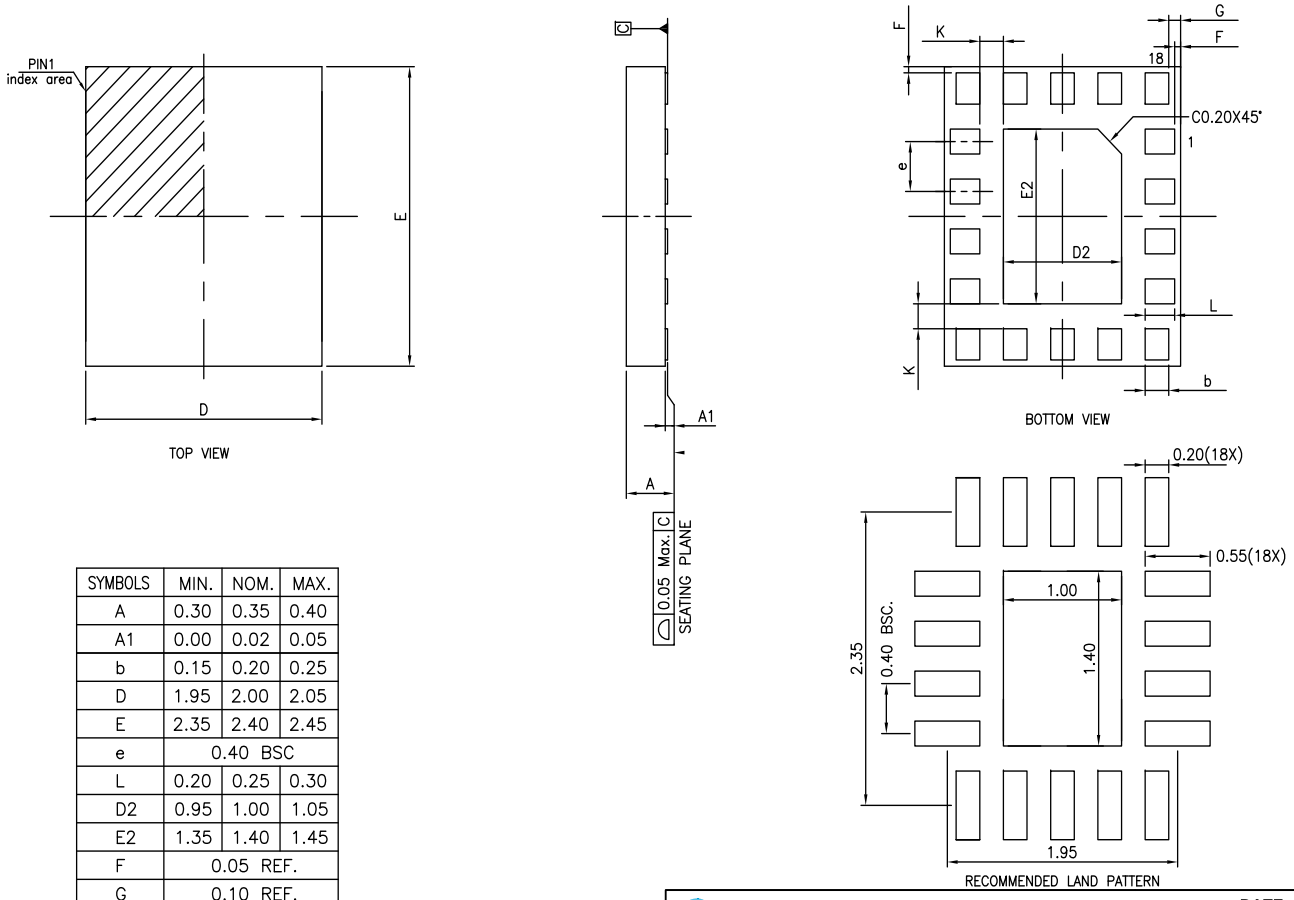
Test Condition Referenced in the Electrical Characteristic Table

Application Schematics



Application Processor Side DE/OS/EQ Settings Connector Side DE/OS/EQ Settings				
AP_SET1 CON_SET1	AP_SET2 CON_SET2	DE1 DE2	OS1 OS2	EQ1 EQ2
0	0	-3.5 dB	1.1V	3 dB
	F	-3.5 dB	0.9V	3 dB
	1	-3.5 dB	1.1V	0 dB
F	0	-3.5 dB	0.9V	0 dB
	F	0 dB	1.1V	3 dB
	1	0 dB	0.9V	3 dB
1	0	0 dB	1.1V	0 dB
	F	0 dB	0.9V	0 dB
	1	-6 dB	1.1V	3 dB

Packaging Mechanical: 18 pin X2QFN



SYMBOLS	MIN.	NOM.	MAX.
A	0.30	0.35	0.40
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
D	1.95	2.00	2.05
E	2.35	2.40	2.45
e	0.40 BSC		
L	0.20	0.25	0.30
D2	0.95	1.00	1.05
E2	1.35	1.40	1.45
F	0.05 REF.		
G	0.10 REF.		
K	0.20 REF.		

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. REFER JEDEC MO-288
3. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY. MESH STENCIL DESIGN IS RECOMMENDED.

PERICOM Enabling Serial Connectivity

DATE: 08/26/15

DESCRIPTION: 18-Pin, X2QFN 2X2.4mm

PACKAGE CODE: XUG (XUG18)

DOCUMENT CONTROL #: PD-2202 REVISION: --

Note: For latest package info, please check: http://www.pericom.com/support/packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Number	Package Code	Package Description
PI2EQX602EXUGEX	XUGEX	18-pin, 2X2.4 mm (X2QFN), Pb-free and Green, Tape & Reel

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- X suffix = Tape/Reel