DISCONTINUED 01/13/2010

T3V3LCS3

Lead-free Green

LOW CAPACITANCE SURFACE MOUNT TVS

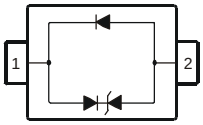
Features

- 350 Watts Peak Pulse Power (tp = 8x20μs)
- IEC 61000-4-2 (ESD): Air – 15kV, Contact – 8kV
- IEC 61000-4-4 (EFT): 40A – 5/50ns
- IEC 61000-4-5 (Surge): 24A, 8/20μs – Level 2(Line-Gnd) & Level 3(Line-Line)
- Low Capacitance, typ. = 3 pF
- Unidirectional Configuration
- **Lead Free/RoHS Compliant (Note 4)**
- **"Green" Device (Note 5)**

Mechanical Data

- Case: SOD-323
- Case Material: Molded Plastic, "Green" Molding Compound, Note 5. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Matte Tin Finish annealed over Alloy 42 leadframe (Lead Free Plating). Solderable per MIL-STD-202, Method 208
- Polarity: Cathode Band, See Page 2
- Marking Information: See Page 2
- Ordering Information: See Page 2
- Weight: 0.004 grams (approximate)

Top View



TOP VIEW

Device Schematic

Maximum Ratings @T_A = 25°C unless otherwise specified

Characteristic	Symbol	Value	Unit
Peak Pulse Power (tp = 8x20μs) (Note 7) T_A = 25°C	P_{pk}	350	W

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Ambient (Note 7) T_A = 25°C	$R_{\theta JA}$	425	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics @T_A = 25°C unless otherwise specified (Note 8)

Reverse Standoff Voltage	Breakdown Voltage V_{BR} @ I_T		Test Current	Max. Reverse Leakage @ V_{RWM} (Note 6)	Max. Clamping Voltage @ I_{pp} = 1A (Note 3)	Max. Clamping Voltage V_C @ I_{PP} (Note 3)		Typical Total Capacitance C_T (Note 1)
V_{RWM} (V)	Min (V)	Max (V)	I_T (mA)	I_R (μA)	V_C (V)	V_C (V)	I_{PP} (A)	(pF)
3.3	4.0	—	1.0	5	7	19	20	3

Notes:
1. V_R = 0V, f = 1MHz.
2. tp = 8x20μs.
3. Clamping voltage value is based on an 8x20 μs peak pulse current (I_{pp}) waveform (see figure 1).
4. No purposefully added lead.
5. Diodes Inc.'s "Green" policy can be found on our website at http://www.diodes.com/products/lead_free/index.php.
6. Short duration pulse test used to minimize self-heating effect.
7. Device mounted on FR-4 PC board with suggested pad layout, which can be found on page 3 or on our website at http://www.diodes.com/datasheets/ap02001.pdf.
8. Positive potential is applied from pin 1 to pin 2.

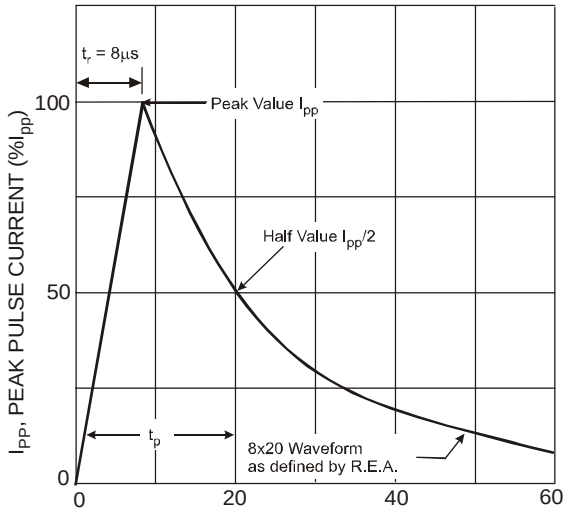


Fig. 1 Pulse Waveform

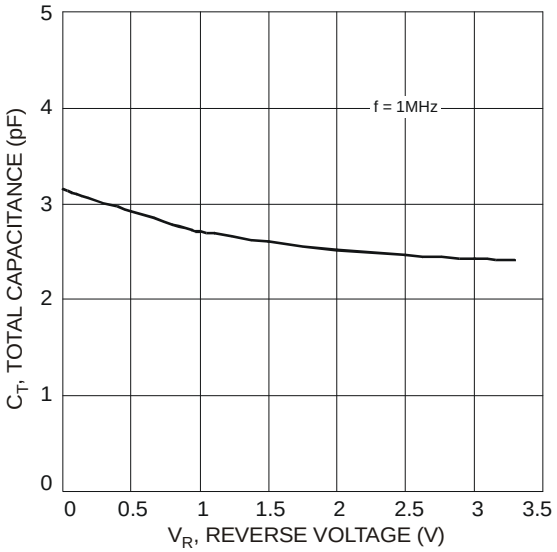


Fig. 2 Typical Total Capacitance vs. Reverse Voltage

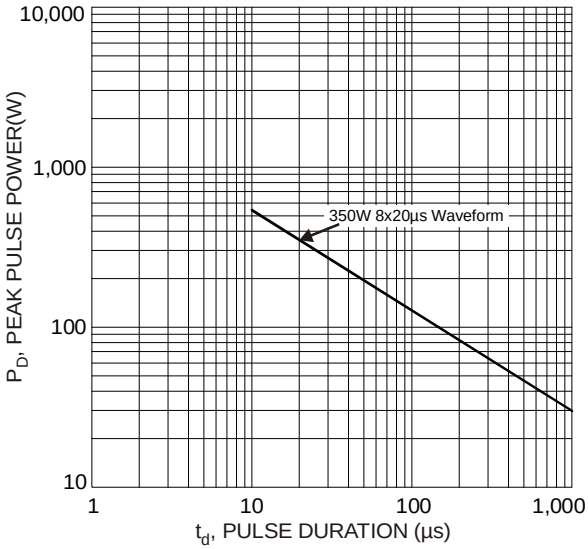


Fig. 3 Max. Peak Pulse Power vs. Power Duration

Ordering Information (Note 9)

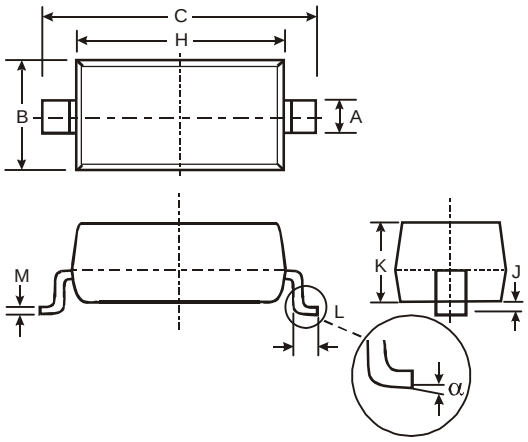
Part Number	Case	Packaging
T3V3LCS3-7	SOD-323	3000/Tape & Reel

Notes: 9. For packaging details, go to our website at http://www.diodes.com/datasheets/ap02007.pdf.

Marking Information

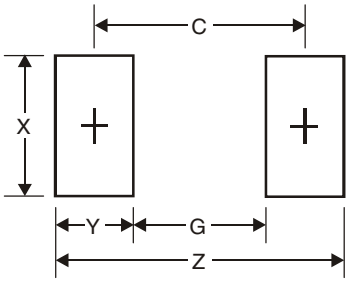
DE = Product Type Marking Code

Package Outline Dimensions



SOD-323		
Dim	**Min**	**Max**
A	0.25	0.35
B	1.20	1.40
C	2.30	2.70
H	1.60	1.80
J	0.00	0.10
K	1.0	1.1
L	0.20	0.40
M	0.10	0.15
α	0°	8°
All Dimensions in mm		

Suggested Pad Layout



Dimensions	Value (in mm)
Z	3.75
G	1.05
X	0.65
Y	1.35
C	2.40

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