Lead-free Green

ZNBG4008

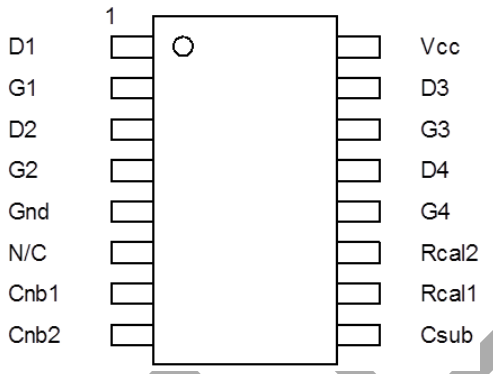
4 STAGE FET LNA BIAS CONTROLLER

Description

The ZNBG4008 is a GaAs and HEMT FET bias controller intended primarily for satellite Low Noise Blocks (LNBs). With the addition of two capacitors and resistors, the device provides drain voltage and current control for up to 4 external grounded source FETs, generating the regulated negative rail required for FET gate biasing while operating from a single supply. The negative bias, at -3 volts, can also be used to supply other external circuits. In setting drain current, ZNBG4008 uses two resistors to split control between two and four FETs. This allows the operating current of input FETs to be adjusted to minimize noise, while the following FET stages can be separately adjusted for maximum gain.

Pin Assignments

QSOP-16



Features

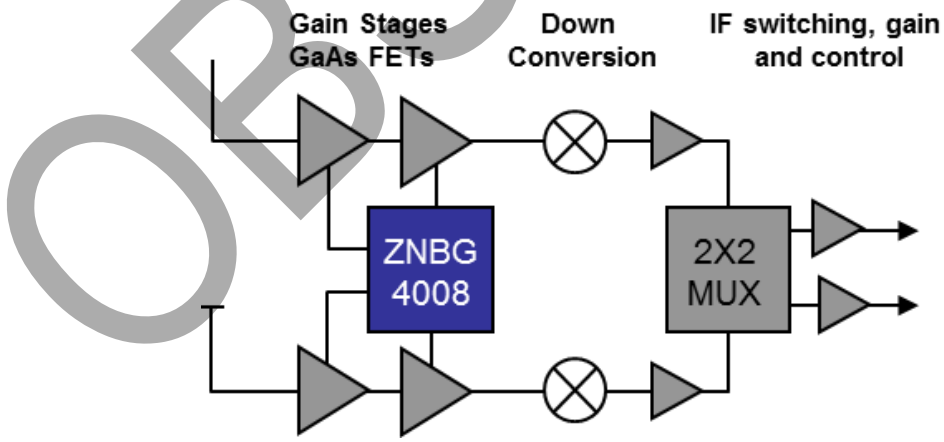
- Provides Bias for up to 4 GaAs and HEMT FETs
- Operating Range of 5.0 to 12.0V
- Dynamic FET Protection
- Amplifier FET Drain Current Selectable (0 to 15mA)
- Regulated Negative Rail Generator Requires only 2 External Capacitors
- Wide Supply Voltage Range
- QSOP-16 Surface Mount Package
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Applications

- Twin LNB's
- Quad LNB's
- Microwave Links
- PMR and Cellular Telephone Systems

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Twin LNB System Diagrams



Detailed Description

The ZNBG series of devices are designed to meet the bias requirements of GaAs and HEMT FETs commonly used in satellite receiver LNBs with a minimum of external components while operating from a minimal voltage supply and using minimal current.

The ZNBG4008 has four FET bias stages that can be programmed to provide a constant drain current. Programming of the FET bias stage arrangement and the operating currents of each FET group is achieved by having resistors connected to the R_{CAL1} and R_{CAL2} pins, allowing input FETs to be biased for optimum noise, and amplifier FETs for optimum gain. Amplifier FETs can be operated at currents in the range 0 to 15mA.

Drain voltages of amplifier stages are set at 2.2V and are current limited to the approximate current set by their associated R_{CAL} resistors.

Depletion mode FETs require a negative voltage bias supply when operated in grounded source circuits. The ZNBG4008 includes an integrated switched capacitor DC-DC converter generating a regulated output of -3V to allow single supply operation. The ZNBG4008 is design to be used with supply rails of 5V to 12V.

It is possible to use less than the device's full complement of FET bias controls, and unused drain and gate connections can be left open circuit without affecting operation of the remaining bias circuits.

To protect the external FETs, the circuits are designed to ensure that under any conditions, including power-up/down transients, the gate drive from the bias circuits cannot exceed -3.5V. Additionally, each stage has its own individual current limiter. Furthermore, if the negative rail experiences a fault condition, such as overload or short circuit, the drain supply to the FETs will shut down to avoid excessive current flow.

The ZNBG4008 is available in the 16-pin QSOP-16 package.

The device's operating temperature is -40°C to +70°C in order to suit a wide range of environmental conditions.

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Parameter	Rating	Unit
Supply Voltage	-0.6 to +15	V
Supply Current	100	mA
Power Dissipation	500	mW
Junction Temperature	+125	°C
Storage Temperature Range	-40 to +150	°C

Recommended Operating Conditions (Note 4) (@T_A = +25°C, unless otherwise specified.)

Parameter	Symbol	Min.	Max.	Unit
Operating Voltage Range	V_{DD}	4.5	12	V
Operating Temperature Range	T_A	-40	+70	°C

Note: 4. ESD sensitive, handling precautions are recommended.

Electrical Characteristics (@ T_{AMB} = +25°C, V_{CC} = 5V, R_{CAL1} = R_{CAL2} = 33K (setting I_{D1} to I_{D6} to 10mA), unless otherwise stated.)

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Supply Current	I_{D1-6} = 0	I_{CC}	—	—	10	mA
	I_{D1-6} = 10mA	$I_{CC(L)}$	—	—	50	mA
Substrate Voltage (Note 6)	I_{CSUB} = 0	V_{CSUB}	-3.5	-3.0	-2.0	V
	I_{CSUB} = -200uA	$V_{CSUB(L)}$	—	—	-2.0	V
Oscillator Frequency	—	F_{OSC}	200	350	800	kHz
Drain Voltage (Note 7)	$C_{GATE-GND}$ = 10nF $C_{DRAIN-GND}$ = 10nF	$V_{D(NOISE)}$	—	—	0.02	Vpk-pk
Gate Voltage (Note 7)	$C_{GATE-GND}$ = 10nF $C_{DRAIN-GND}$ = 10nF	$V_{G(NOISE)}$	—	—	0.005	Vpk-pk
Gate Characteristics (Pins G1 to G4)						
Current Range	—	I_G	-30	—	2,000	µA
Voltage Low	I_D = 12mA, I_G = -10µA	$V_{G(L)}$	-3.5	—	-2.0	V
Voltage High	I_D = 8mA, I_G = 0	$V_{G(H)}$	0	—	1.0	V
Drain Characteristics (Pins D1 to D4)						
Current Range	—	I_D	0	—	15	mA
Current Operating (Note 5)	Standard Application Circuit	$I_{D(OP)}$	8	10	12	mA
Voltage Operating	I_D = 10mA	$V_{D(OP)}$	2.0	2.2	2.4	V
Delta V_D vs. V_{CC}	V_{CC} = 5V to 12V	dV_D/dV_{CC}	—	0.5	—	%/V
Delta V_D vs. T_{OP}	T_{OP} = -40°C to +100°C	dV_D/dT_{OP}	—	50	—	ppm

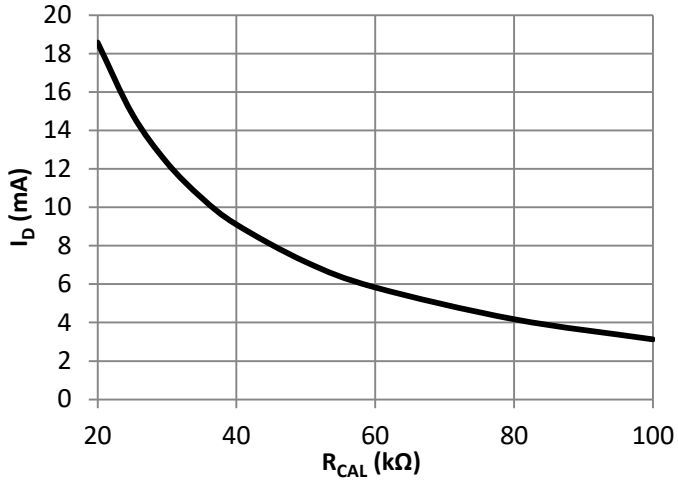
Notes: 5. The characteristics are measured using up to two external reference resistors, R_{CAL1} and R_{CAL2} wired from pins $R_{CAL1/2}$ to ground. Resistor R_{CAL1} sets the drain current of FETs 1 and 3. R_{CAL2} sets the drain currents of FETs 2 and 4.

6. The negative bias voltages are generated on-chip using an internal oscillator. Two external capacitors, C_{NB} and C_{SUB} of value 47nF are required for this purpose.

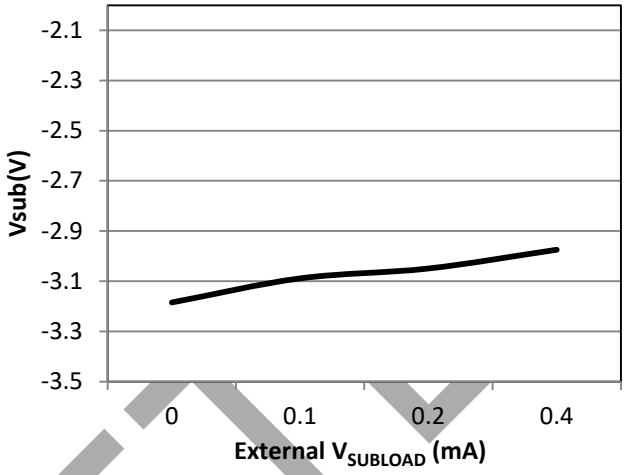
7. Noise voltage measurements are made with FETs and gate and drain capacitors of value 10nF in place. Noise voltages are not measured in production.

Typical Characteristics (@ T_{AMB} = +25°C, V_{CC} = 5V, R_{CAL1} = R_{CAL2} = 33K (setting I_D to 10mA), unless otherwise stated.)

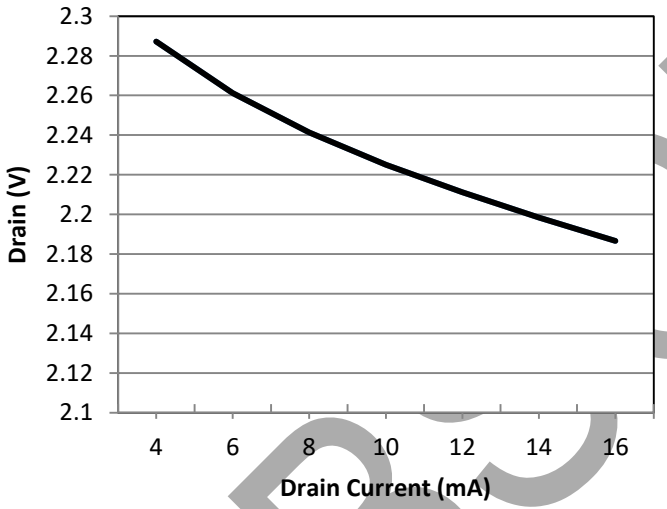
Drain Current vs. R_{CAL}



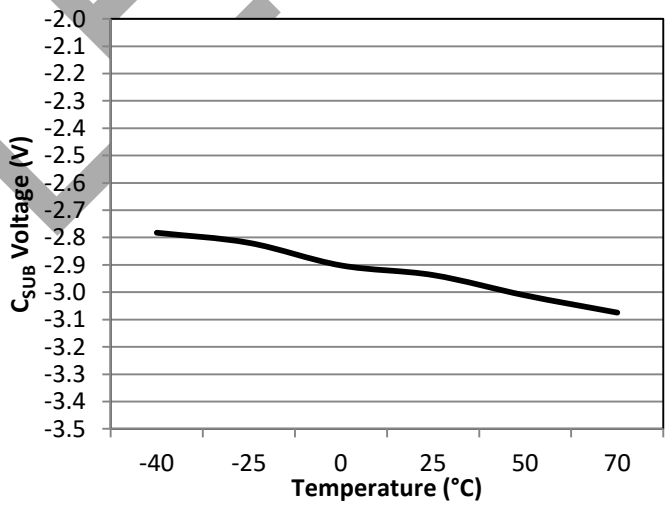
V_{SUB} vs. External Load



Drain Voltage vs. Drain Current

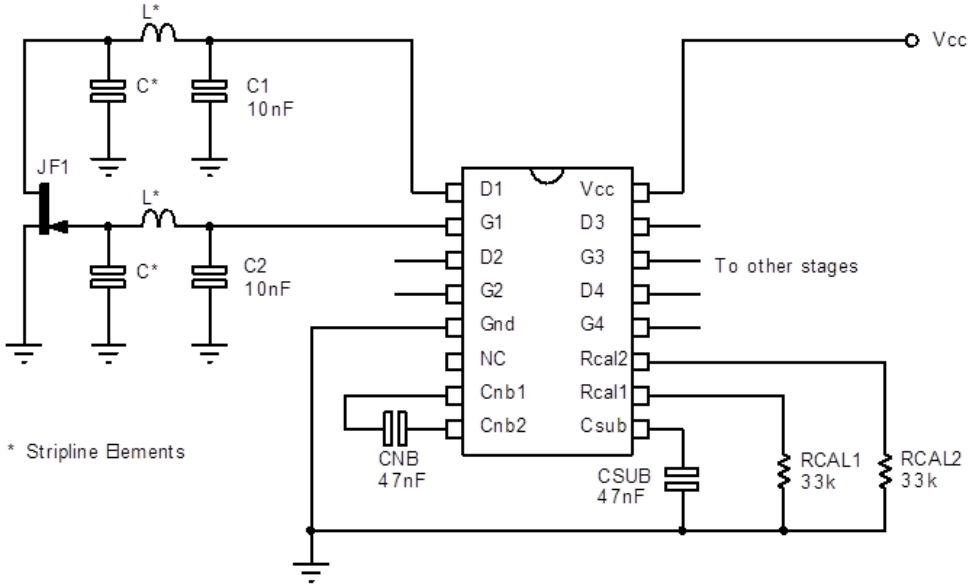


C_{SUB} vs. Temperature



Application Information

Below is a partial applications circuit for the ZNBG4008 showing all external components needed for biasing one of the four FET stages available as a normal LNA bias. Each bias stage is provided with a gate and drain pin. The drain pin provides a regulated 2.2V supply that includes a drain current monitor. The drain current taken by the external FET is compared with a user-selected level, generating a signal that adjusts the gate voltage of the FET to obtain the required drain current. If for any reason, an attempt is made to draw more than the user set drain current from the drain pin, the drain voltage will be reduced to ensure excess current is not taken. The gate pin drivers are also current limited.



The bias stages are split up into two groups, with the drain current of each group set by an external R_{CAL} resistor. R_{CAL1} sets the drain currents for stages 1 and 3, while R_{CAL2} sets the drain currents for stages 2 and 4. This allows the optimization of drain currents for differing tasks such as input stages where noise can be critical and later amplifier stages where gain may be more important. A graph showing the relationship between the value of R_{CAL} and I_D is provided in the Typical Characteristics section of this datasheet.

The ZNBG4008 includes a switched capacitor DC-DC converter that is used to generate the negative supply required to bias depletion mode FETs used in common source circuit configuration as shown above. This converter uses two external capacitors, C_{NB}, the charge transfer capacitor, and C_{SUB}, the output reservoir capacitor. The circuit provides a regulated -3V supply for both gate driver use and external use, if required (for extra discrete bias stages, mixer bias, local oscillator bias etc.). The -3V supply is available from the C_{SUB} pin.

If any bias stages are not required, their gate and drain pins may be left open circuit. If all bias stages associated with an R_{CAL} resistor are not required, then this resistor may be omitted.

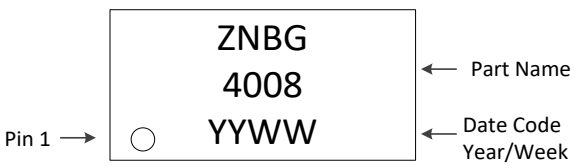
Ordering Information (Note 8)

Device	Package	Reel Size (inches)	Tape Width (mm)	Quantity per Reel
ZNBG4008Q16TC	QSOP-16	13	16	2,500

Note: 8. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information

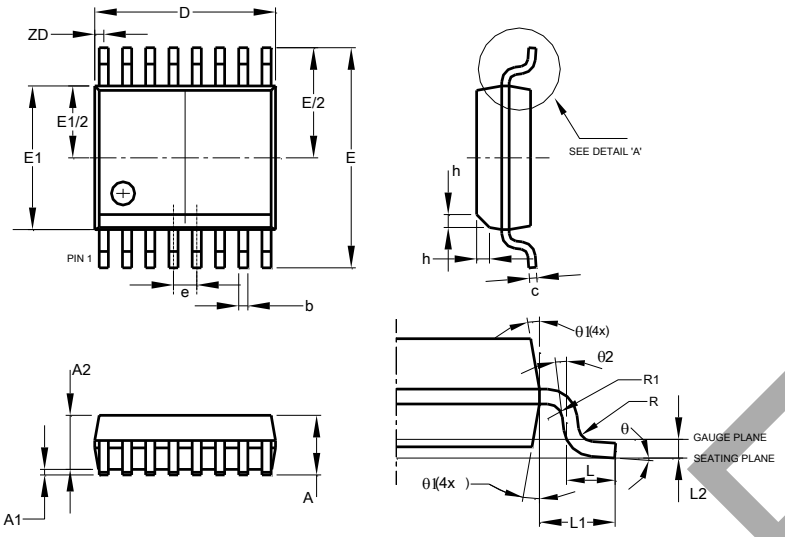
QSOP-16



Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

QSOP-16

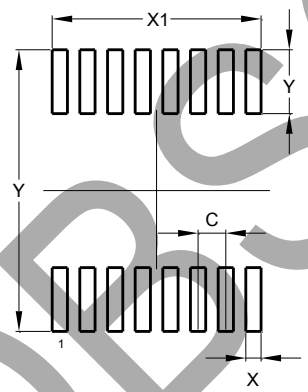


QSOP-16			
Dim	**Min**	**Max**	**Typ**
A	1.55	1.73	-
A1	0.10	0.25	-
A2	1.40	1.50	-
b	0.20	0.30	-
c	0.18	0.25	-
D	4.80	5.00	-
E	5.79	6.20	-
E1	3.81	3.99	-
e	0.635 BSC		
h	0.254	0.508	-
L	0.41	1.27	-
L1	1.03 REF		
L2	0.254 BSC		
R	0.0762	-	-
R1	0.0762	-	-
ZD	0.23 REF		
θ	0°	8°	-
θ1	5°	15°	-
θ2	0°	-	-
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

QSOP-16



Dimensions	Value (in mm)
C	0.635
X	0.350
X1	4.795
Y	1.450
Y1	6.400

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