

Description

The ZXMS82120S14P is a dual-channel, high-side power switch in a SO-14EP exposed heatsink package incorporating protective and diagnostic functions.

The device comprises a monolithic n-channel vertical power MOSFET with integrated temperature and current sensors with a charge-pumped gate supply and has a low quiescent current in OFF state.

The device is enabled by active high 3.3V and 5V logic-level drive to the inputs. The device includes a diagnostic current-sense output proportional to load current and a defined diagnostic fault signal in case of overload operation, overtemperature, short-circuit or open-load conditions.

Features

Protection Functions

- Reverse Battery Protection Using External Components
- Voltage Dependent Current Limiting
- Overtemperature Protection with Auto-Restart
- Overvoltage Protection Including Load Dump
- Stable Undervoltage Protection
- ESD Protection
- Loss of Ground Protection with External Components
- Enhanced Short-Circuit Protection

Diagnostic Functions

- Proportional Load Current-Sense Output
 - Linear Voltage Drop Regulation to Maintain Sense Accuracy Even at Very Low Load Currents
 - Enabled by Logic Input
 - Channel Selected by Logic Input
 - Defined Temperature and Current Dependency
- Open-Load Detection
 - Using Load Current-Sense in ON State
 - Using Output Voltage Detection in OFF State
- Defined Fault Signal in Case of Overload Operation, Overtemperature, or Short-Circuit and Open-Load in OFF State

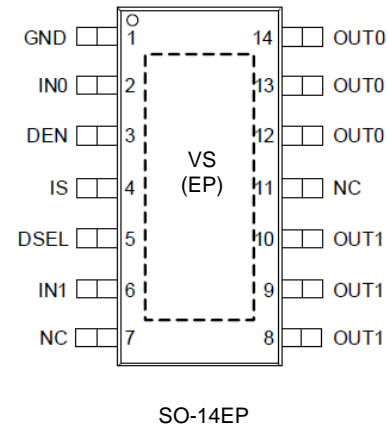
Miscellaneous

- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **An automotive-compliant part is available under separate datasheet ([ZXMS82120S14PQ](#))**

Notes: 1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Assignment

(Top View)



Applications

- High-side switching with diagnostic feedback for:
 - 12V grounded loads
 - Resistive, inductive and capacitive loads
- Suitable for high inrush current loads
 - Incandescent lamps (P10W), motors, LEDs, etc.
- Compact low power replacement for:
 - Relays, fuses and discrete circuits

Summary Specifications

| Parameter | Symbol | Rating |
|---|---------------------|-----------|
| Operating Voltage | V _S | 5V to 28V |
| Maximum Supply Voltage | V _{S(LD)} | 41V |
| Maximum ON Resistance, T _J = +150°C | R _{DS(ON)} | 240mΩ |
| Nominal Load Current | I _{L(NOM)} | 2.5A |
| Typical Current Sense Ratio | K _{ILIS} | 550 |
| Minimum Current Limitation | I _{L5(SC)} | 10A |
| Maximum Standby Current, T _J = +25°C | I _{S(OFF)} | 0.5μA |

Typical Applications Circuit

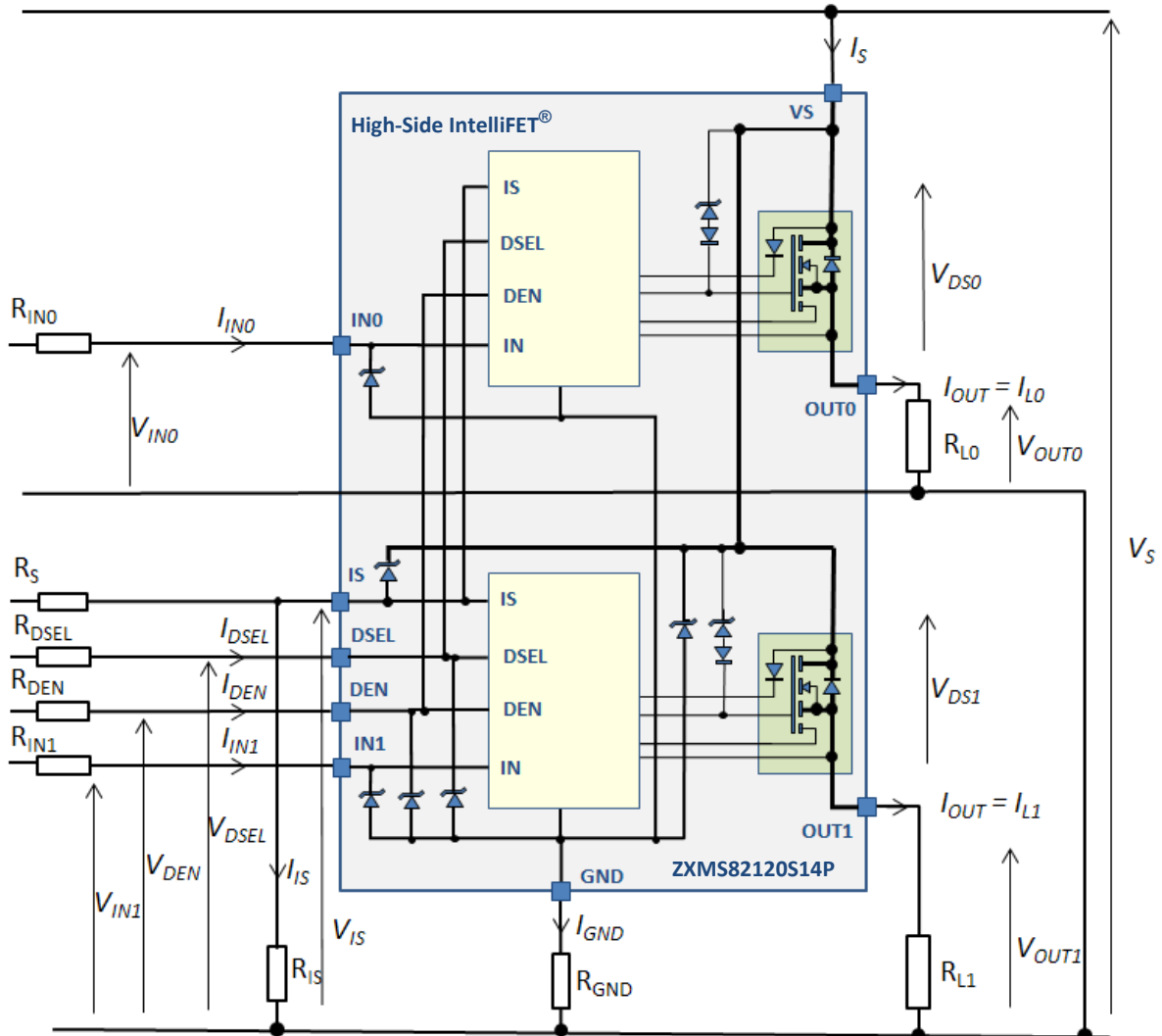


Figure 1. Typical Application Configuration

R_{GND}, R_{INx}, R_{DEN}, R_{DSEL} and R_S are optional. They may be replaced by shorts depending on the application. Non-zero resistors may be used to:

- Reduce peak currents during supply voltage transients that exceed the ±V_S internal clamp voltages
 - Typically transients exceeding 41V or may activate the internal clamps
- Protect the customer's application from high currents during transients exceeding 41V
- Keep within rated current during reverse battery, recommended is R_S = R_{DEN} = R_{INx} = R_{DSEL} = 4.7kΩ, R_{GND} = 150Ω
- Ensure that the device is off when there is loss of ground connection to the device or module

Pin Description

| Pin Number | Pin Name | Function and Description |
|------------|----------|---|
| 1 | GND | Ground or negative supply |
| 2 | IN0 | Input channel 0, activates output channel 0 |
| 3 | DEN | Diagnostic enable, allows common connection of the IS pin with multiple devices |
| 4 | IS | Diagnostic output, provides an analog sense current proportional to the load current under normal operation, or a defined current under overload or shutdown conditions |
| 5 | DSEL | Input to select which channel to be diagnosed |
| 6 | IN1 | Input channel 1, activates output channel 1 |
| 7, 11 | NC | Not connected |
| 8, 9, 10 | OUT1 | Output 1 to the load, must be connected together |
| 12, 13, 14 | OUT0 | Output 0 to the load, must be connected together |
| EP | VS | Voltage supply or battery positive |

Table 1. Pin Description

Functional Block Diagram

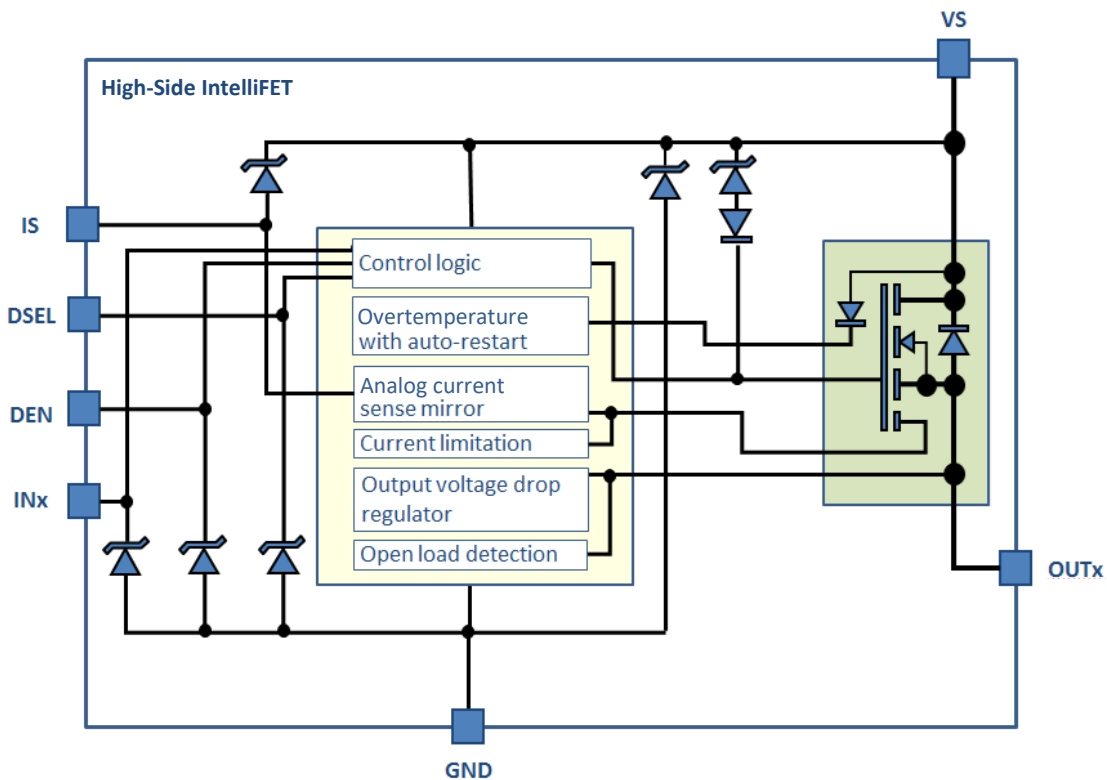


Figure 2. Functional Block Diagram of ZXMS82120S14P

Absolute Maximum Ratings (Notes 4, 5) (@T_J = +25°C, unless otherwise specified.)

| Symbol | Parameter | Ratings | | Unit | Conditions |
|--------------------------------|--|---------|----------------|------|---|
| | | Min | Max | | |
| Supply Voltage | | | | | |
| V _S | Supply voltage | -0.3 | 28 | V | — |
| V _{S(REV)} | Reverse supply voltage | 0 | 16 | V | R _L ≥ 12Ω, R _{GND} = 150Ω T _{amb} = +25°C, t < 2 mins |
| V _{S(SC)} | Supply voltage for short-circuit protection (Note 6) | 0 | 24 | V | — |
| V _{S(LD)} | Supply voltage for load-dump protection (ISO 7637) | — | 41 | V | R _{IN} = 2Ω, R _L = 12Ω |
| Interface Pins | | | | | |
| V _{IN} | IN pins voltage | -0.3 | 6 | V | — |
| | | — | 7 | V | t < 2 mins |
| I _{IN} | Current in IN pins | -2 | 2 | mA | — |
| V _{DEN} | DEN pin voltage | -0.3 | 6 | V | — |
| | | — | 7 | V | t < 2 mins |
| I _{DEN} | Current in DEN pin | -2 | 2 | mA | — |
| V _{DSEL} | DSEL pin voltage | -0.3 | 6 | V | — |
| | | — | 7 | V | t < 2 mins |
| I _{DSEL} | Current in DSEL pin | -25 | 50 | mA | — |
| V _{IS} | IS pin voltage | -0.3 | V _S | V | — |
| I _{IS} | Current in IS pin | -25 | 50 | mA | — |
| Output Stage | | | | | |
| I _L | Load current (Note 7) | — | Self-limited | A | — |
| P _{TOT} | Power dissipation | — | 1.8 | W | T _{amb} = +85°C, T _J < +150°C |
| E _{AS} | Energy dissipation (single pulse, one channel) | — | 15 | mJ | V _S = 13.5V, I _L = 2A T _J = +150°C |
| V _{DS} | VS to OUT pin voltage | — | 41 | V | — |
| N _{RSC} | Repetitive short-circuit capability (Note 8) | — | 300 | kcyc | t _{ON} = 300ms |
| Current | | | | | |
| I _{GND} | Current in GND pin | -10 | 10 | mA | — |
| | | -150 | 20 | mA | t < 2 mins |
| Temperature | | | | | |
| T _J | Junction temperature | -40 | +150 | °C | — |
| T _{STG} | Storage temperature | -55 | +150 | °C | — |
| Electrostatic Discharge | | | | | |
| V _{ESD(HBM)} | ESD capability HBM (all pins) | -2 | 2 | kV | EIA/JESD 22-A 114B |
| | ESD capability HBM OUT to GND and V _S shorted | -4 | 4 | kV | |
| V _{ESD(CDM)} | ESD capability CDM | -0.75 | 0.75 | kV | AEC-Q100-011 |

- Notes:
- Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.
 - Not subject to production test, guaranteed by design.
 - Short-circuit protection is outside normal operation and is limited to single pulse and allows combinations of resistance and inductance.
 - Current limit is a protection feature and operation in current limitation, e.g. with short-circuit loads, is outside the normal operation range.
 - Repetitive short-circuit protection characterisation also carried out according to AEC-Q100-012 at 14V.

Package Thermal Data

| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------------|---|-----|-----|-----|------|
| $R_{\theta JS}$ | Thermal resistance, junction-to-soldering point (Note 5) | — | 4 | — | °C/W |
| $R_{\theta JA}$ | Thermal resistance, junction-to-ambient mounted on PCB Both channels active (Notes 5, 9) | — | 47 | — | °C/W |

Note: 9. Device mounted on vertical PCB, 2" x 2" x 1.6mm, FR4 with 2oz copper for all connections.

Recommended Operating Conditions

| Symbol | Parameter | Min | Max | Unit |
|--------------|--------------------------------------|-----|-----|------|
| $V_{S(NOM)}$ | Normal operating voltage (Note 10) | 8 | 18 | V |
| $V_{S(OP)}$ | Extended operating voltage (Note 11) | 5 | 28 | V |

Notes: 10. For normal operation and protection features.

11. Operation across an extended range is possible but is load dependant – device may have reduced protection against faulty (overload or short-circuit) loads.

Operational Electrical Characteristics

(Unless otherwise specified: $-40^{\circ}\text{C} < T_J < +150^{\circ}\text{C}$; typical values based on $T_J = +25^{\circ}\text{C}$)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------|--|---|-----|------|-----|---------------|
| General | | | | | | |
| $V_{S(OP)}$ | Extended operating voltage | $V_{IN} = 4.5\text{V}$, $V_{DS} < 0.5\text{V}$ | 5 | 13.5 | 28 | V |
| $V_{S(OP_MIN)}$ | Undervoltage restart | $V_{IN} = 4.5\text{V}$, $R_L = 12\Omega$ | 3.8 | 4.2 | 5 | V |
| $V_{S(UV)}$ | Undervoltage shutdown | $V_{IN} = 4.5\text{V}$, $V_{DEN} = 0\text{V}$ $R_L = 12\Omega$ | 3 | 3.3 | 4.1 | V |
| $V_{S(UV_HYS)}$ | Undervoltage hysteresis | — | — | 0.85 | — | V |
| I_{GND} | Operating current One channel active | $V_{IN} = V_{DEN} = 5.5\text{V}$, $V_S = 18\text{V}$ Device in $R_{DS(ON)}$ | — | 2.5 | 6 | mA |
| | Operating current Both channels active | | — | 3.5 | 8 | mA |
| $I_{S(OFF)}$ | Standby current | V_{IN} and V_{DEN} floating $V_{OUT} = 0\text{V}$, $V_S = 18\text{V}$ $T_J \leq +85^{\circ}\text{C}$ | — | 0.1 | 0.5 | μA |
| | | V_{IN} and V_{DEN} floating $V_{OUT} = 0\text{V}$, $V_S = 18\text{V}$ $T_J = +150^{\circ}\text{C}$ | — | 2 | 20 | μA |
| $I_{S(OFF_DEN)}$ | Standby current with diagnostic pin active | V_{IN} floating, $V_{OUT} = 0\text{V}$ $V_S = 18\text{V}$, $V_{DEN} = 5.5\text{V}$ | — | 1 | — | mA |

Output ON-State Characteristics

The ON-state resistance $R_{DS(ON)}$ depends on the supply voltage V_S and junction temperature T_J .

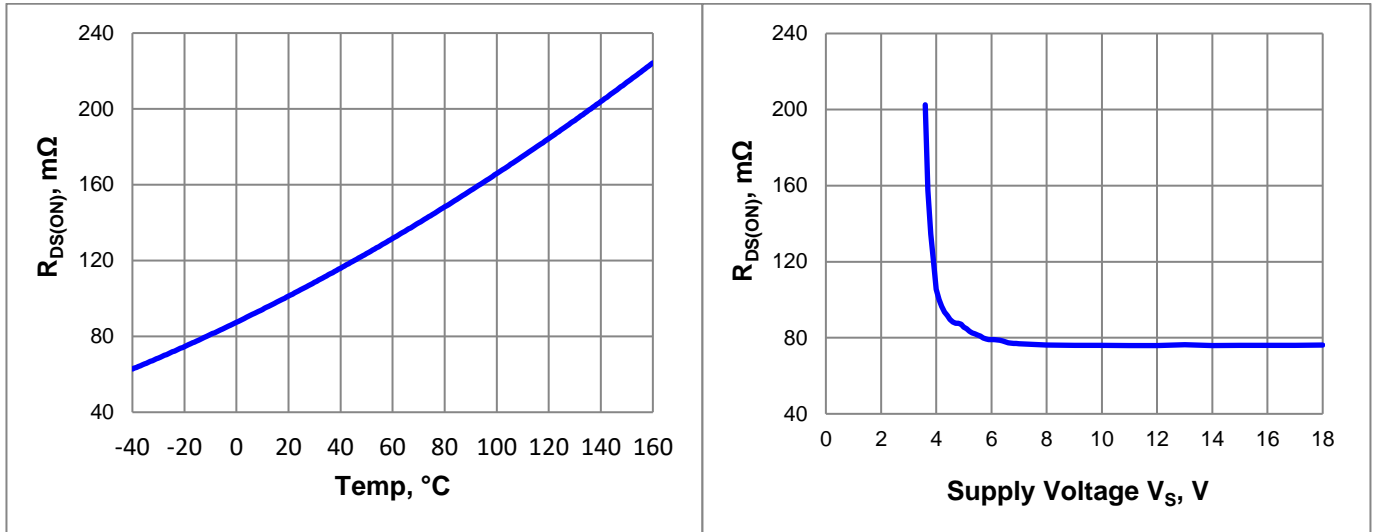


Figure 3. Typical R_{DS} ON-State Resistance

At low load current I_L , the MOSFET gate drive is reduced to maintain a near constant output voltage drop $V_{DS(NL)}$. This limits the effect of internal op-amp offset voltage, to maintain useful K_{ILIS} ratio accuracy even at very low I_L .

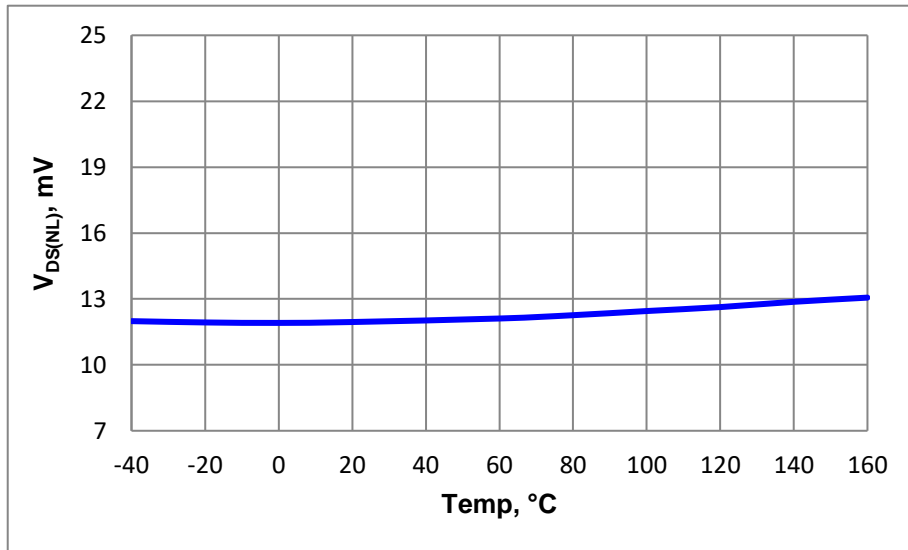


Figure 4. Output Voltage Drop Regulation, $I_{out} = 30\text{mA}$

Resistive Load Switching

The power MOSFET turn-ON and turn-OFF processes are determined by the device itself, with rates suitable for EMC compatibility.

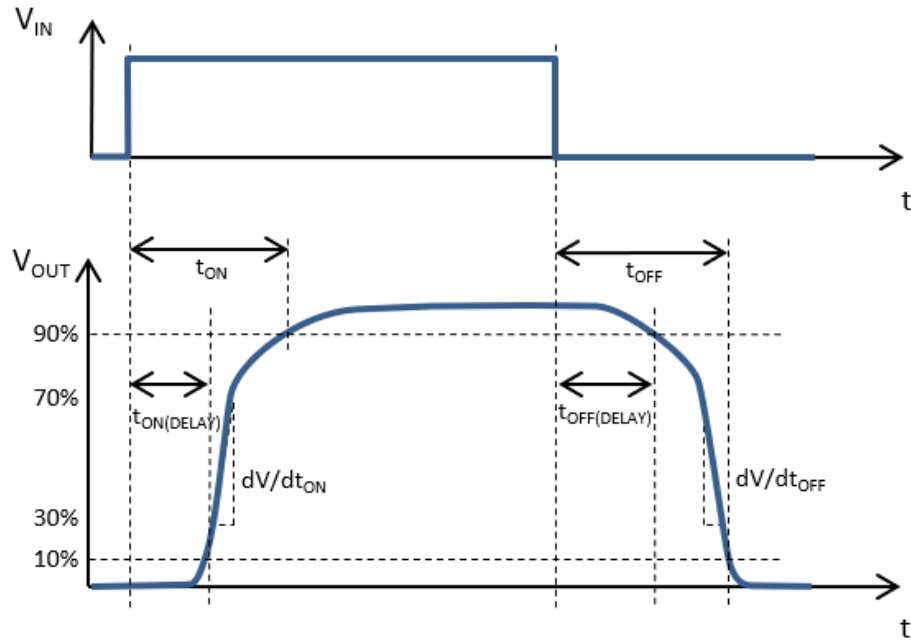


Figure 5. Switching a Resistive Load

Output Inductive Load Clamp

To de-energise inductive loads the OUT terminal must be allowed to swing below ground (V_{OUT} rings negative) during the OFF state.

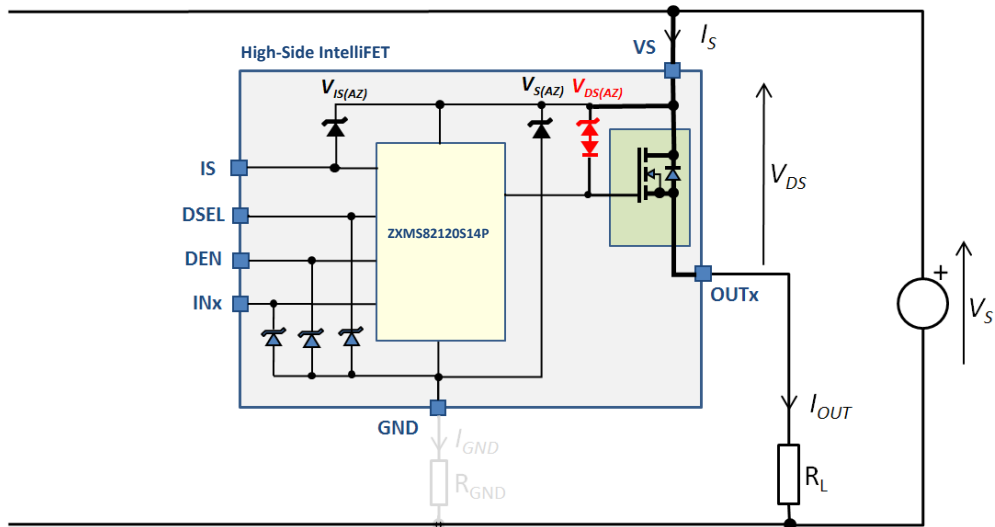


Figure 6. Output Clamp

Output Inductive Load Clamp (continued)

A low-impedance active voltage clamp uses the MOSFET channel to limit the maximum voltage across the MOSFET drain-source terminals, limiting the swing of OUT below V_S to safe $V_{DS(AZ)}$. This prevents avalanche of the MOSFET or associated circuitry.

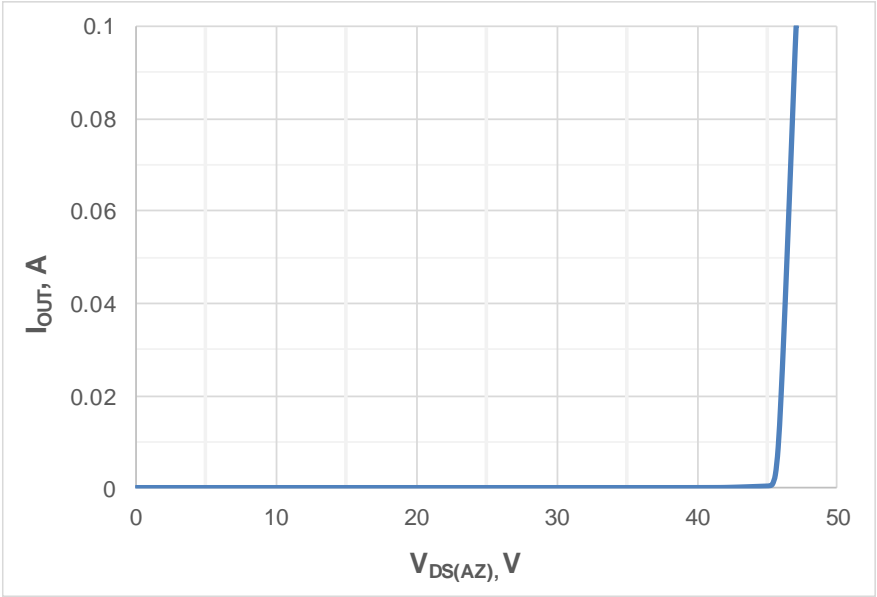


Figure 7. Typical Output Clamp Characteristic

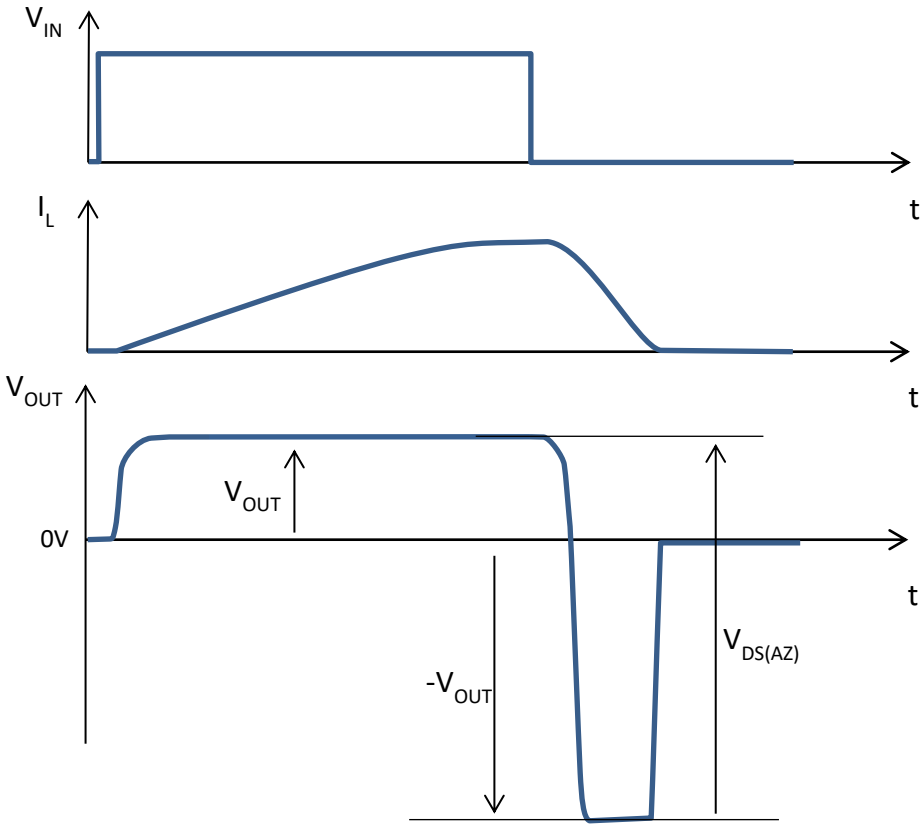


Figure 8. Switching an Inductive Load

Maximum Load Inductance

Stored inductive load ring-OFF energy is dissipated in the MOSFET during switching and load ring-OFF clamping. Additional energy is also supplied to the system by the V_S supply until the load current I_L reaches zero. This causes a temporary rise in MOSFET temperature after turn-OFF begins. The temperature reached depends on the starting temperature, thermal environment, load current I_L , load inductance L_L , load resistance R_L and supply voltage V_S .

Inverse Current Capability

In the ON-state the device will remain on if the output current becomes inverse until or unless the inverse current becomes high enough to create a $-V_{DS}$ approaching body diode conduction. During inverse current conduction, $I_{L(INV)}$, the IS sense output will be zero. If body diode conduction occurs all functions are disabled or unspecified until the inverse current becomes very small.

If inverse current is present in the OFF-state body diode conduction occurs and all functions are disabled or unspecified. When inverse current is removed or becomes very small then turn-ON and normal function become possible.

Power Electrical Characteristics

(Unless otherwise specified: $8V < V_S < 18V$, $-40^\circ C < T_J < +150^\circ C$; typical values based on $V_S = 13.5V$, $T_J = +25^\circ C$)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|--|---|-----|------|-----|------------|
| Output Characteristics | | | | | | |
| $R_{DS(ON)}$ | ON-state resistance per channel | $V_{IN} = 4.5V$, $I_L = 2A$ $T_J = +150^\circ C$ | — | 200 | 240 | m Ω |
| | | $V_{IN} = 4.5V$, $I_L = 2A$ $T_J = +25^\circ C$ | — | 100 | — | m Ω |
| $I_{L(NOM)}$ | Nominal load current One channel active (Note 12) | $T_{amb} = +85^\circ C$, $T_J < +150^\circ C$ | — | 2.5 | — | A |
| | Nominal load current Both channels active (Note 12) | | — | 2 | — | A |
| $V_{DS(NL)}$ | Voltage drop regulation at low I_L | $I_L = 30mA$ | — | 12 | 25 | mV |
| $V_{DS(AZ)}$ | Output clamp voltage | $I_L = 20mA$ | 41 | 47 | 53 | V |
| $I_{L(OFF)}$ | Output leakage current per channel | V_{IN} floating, $V_{OUT} = 0V$ $T_J \leq +85^\circ C$ | — | 0.1 | 0.5 | μA |
| | | V_{IN} floating, $V_{OUT} = 0V$ $T_J = +150^\circ C$ | — | 1 | 10 | μA |
| $I_{L(INV)}$ | Inverse output current (Note 13) | $V_S < V_{OUT}$ | — | 2 | — | A |
| Timings | | | | | | |
| dV/dt_{ON} | Slew rate ON, 30% to 70% V_S | $R_L = 12\Omega$, $V_S = 13.5V$ | 0.1 | 0.25 | 0.5 | V/ μs |
| dV/dt_{OFF} | Slew rate OFF, 70% to 30% V_S | | 0.1 | 0.45 | 0.7 | V/ μs |
| t_{ON} | Turn-ON time to 90% V_S | | 30 | 90 | 230 | μs |
| t_{OFF} | Turn-OFF time to 10% V_S | | 30 | 170 | 230 | μs |
| $t_{ON(DELAY)}$ | Turn-ON delay to 10% V_S | | 10 | 25 | 100 | μs |
| $t_{OFF(DELAY)}$ | Turn-OFF delay to 90% V_S | | 10 | 95 | 150 | μs |
| E_{ON} | Switch ON energy | $R_L = 12\Omega$, $V_S = 18V$ $V_{OUT} = 90\% V_S$ | — | 0.4 | — | mJ |
| E_{OFF} | Switch OFF energy | $R_L = 12\Omega$, $V_S = 18V$ $V_{OUT} = 10\% V_S$ | — | 0.3 | — | mJ |

Notes: 12. Device mounted on vertical 50mm x 50mm x 1.5mm FR4 single-sided PCB with 6cm² 2oz copper in free air.
13. ON-state reverse conduction, functional test only.

Protection Features

Loss of Ground Protection

The device will turn off in the case that the ground pin connection is lost and the load remains connected. It is recommended to use high ohmic input resistors in the interface pins to ensure that the device is turned off by limiting the current in the paths from the ground pin, through the input and diagnostic enable ESD diodes, to the external driving circuits.

Undervoltage Protection

The device will not turn on if the V_S supply voltage is below the minimum operating voltage $V_{S(OP_MIN)}$ where protection functions may not be operational. If the device is already on then the supply voltage has to drop to below the undervoltage threshold $V_{S(UV)}$ to turn the output off. Figure 9 shows the undervoltage mechanism.

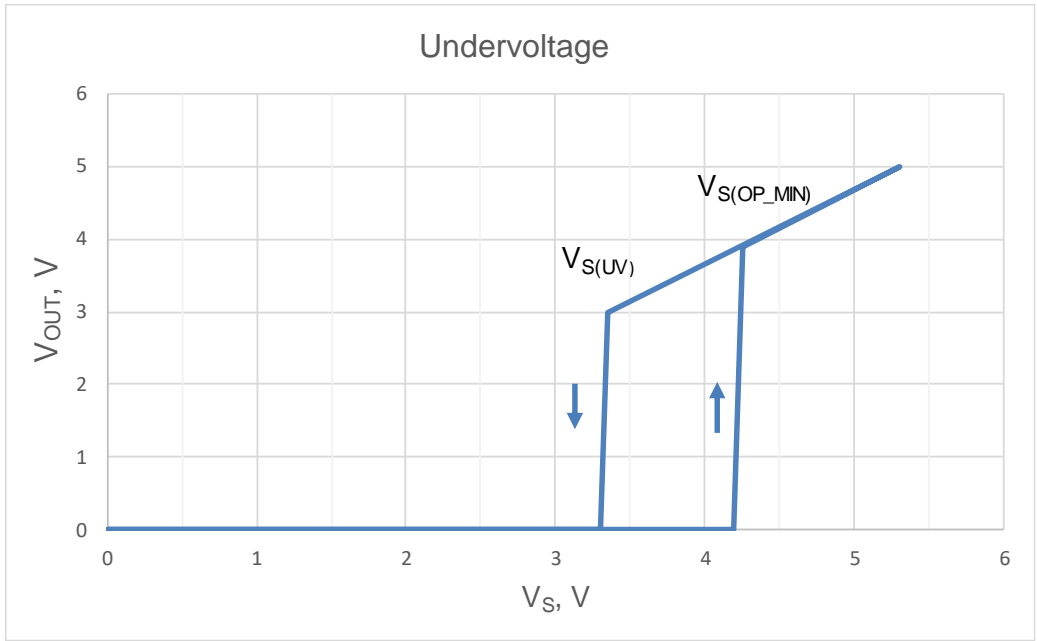


Figure 9. Undervoltage Behavior

Protection Features (continued)

Overvoltage Protection

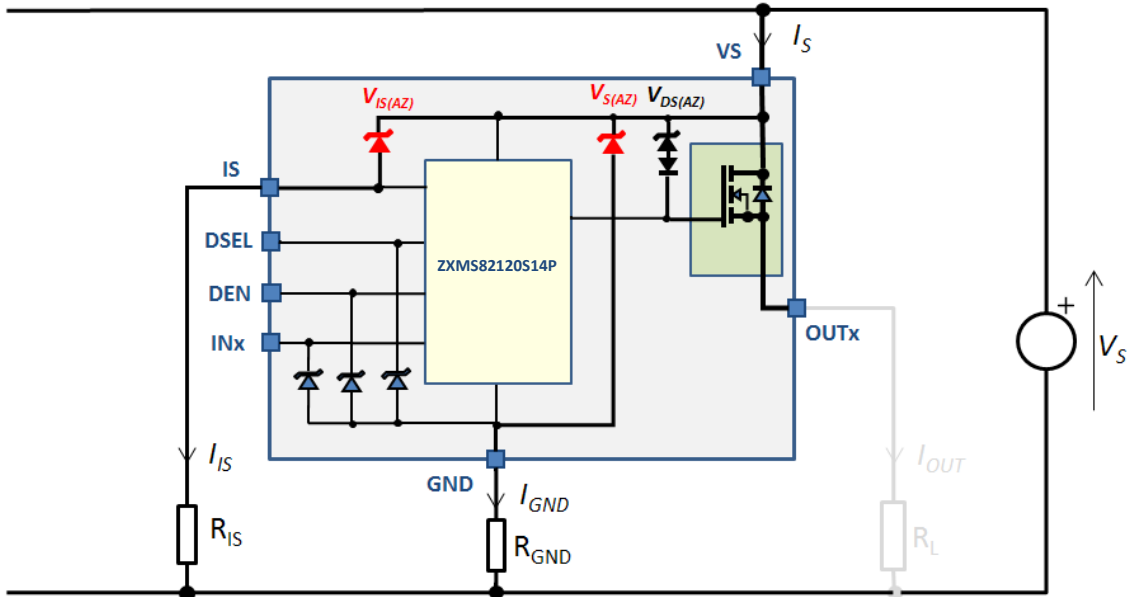


Figure 10. Overvoltage Clamping Circuit

The GND pin has an active protection clamp, operating much as a low noise high voltage Zener device, to protect it from overvoltage for high V_S transients. During V_S transient overvoltage the voltage is clamped and the excess voltage, $V_S - V_{S(AZ)}$, is applied across the ground resistor R_{GND} raising the potential on the ground pin. Additional high ohmic series resistors may be needed to prevent high V_{IN} and V_{DEN} being applied directly to the driving circuits.

The IS pin also has an active protection clamp and during V_S transient overvoltage the voltage is clamped and excess voltage, $V_S - V_{IS(AZ)}$, is applied across the sense resistor R_{IS} . An additional high ohmic series resistor may be needed in the application to prevent high V_{IS} being applied directly to the application monitoring circuit.

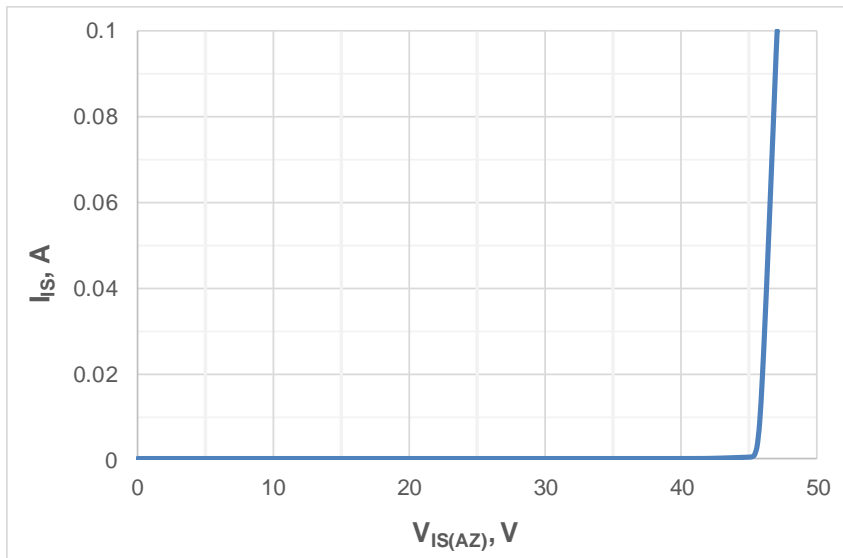


Figure 11. Typical V_S Clamp Characteristic

Protection Features (continued)

Also during V_S overvoltage transient the voltage V_{S-OUT} is clamped and the excess voltage, $V_S - V_{DS(AZ)}$, is applied across the load R_L . V_{S-OUT} is the same clamp described under the earlier section [Output Inductive Load Clamp](#).

Reverse Battery Protection

During reverse battery the output body diode is conducting current limited by the load itself resulting in power dissipation and the current in the ground and logic inputs has to be limited by external resistor components. No operating functions are available in this condition.

Overload Protection

During overload the output current is limited to a value depending on the V_{DS} voltage resulting in high dissipation in the output power stage. Sustained operation in this mode will raise the internal junction temperature until dynamic or absolute overtemperature protection cycling begins. There is a dynamic ($\Delta T_{J(SW)}$) and an absolute ($T_{J(SC)}$) temperature sensor. Figure 12 gives a sketch of overload protection.

If the temperature rise of the power stage versus the cooler control area exceeds $\Delta T_{J(SW)}$ then the device will be turned off until the rise falls to a reset level. Each cycle causes the absolute temperature to increase a little.

If the absolute temperature reaches $T_{J(SC)}$ then the device will be turned off until the absolute temperature falls by $\Delta T_{J(SC)}$. The device will continue to cycle to $T_{J(SC)}$ as long as the fault condition remains.

The IS pin outputs $I_{IS(FAULT)}$ during load current limitation, during dynamic overtemperature cycling and absolute overtemperature cycling.

Both channels are independently overload protected and if both are in overtemperature shutdown there is no restart synchronization. As only one channel can be monitored on the IS pin it is not recommended to use both channels connected in parallel.

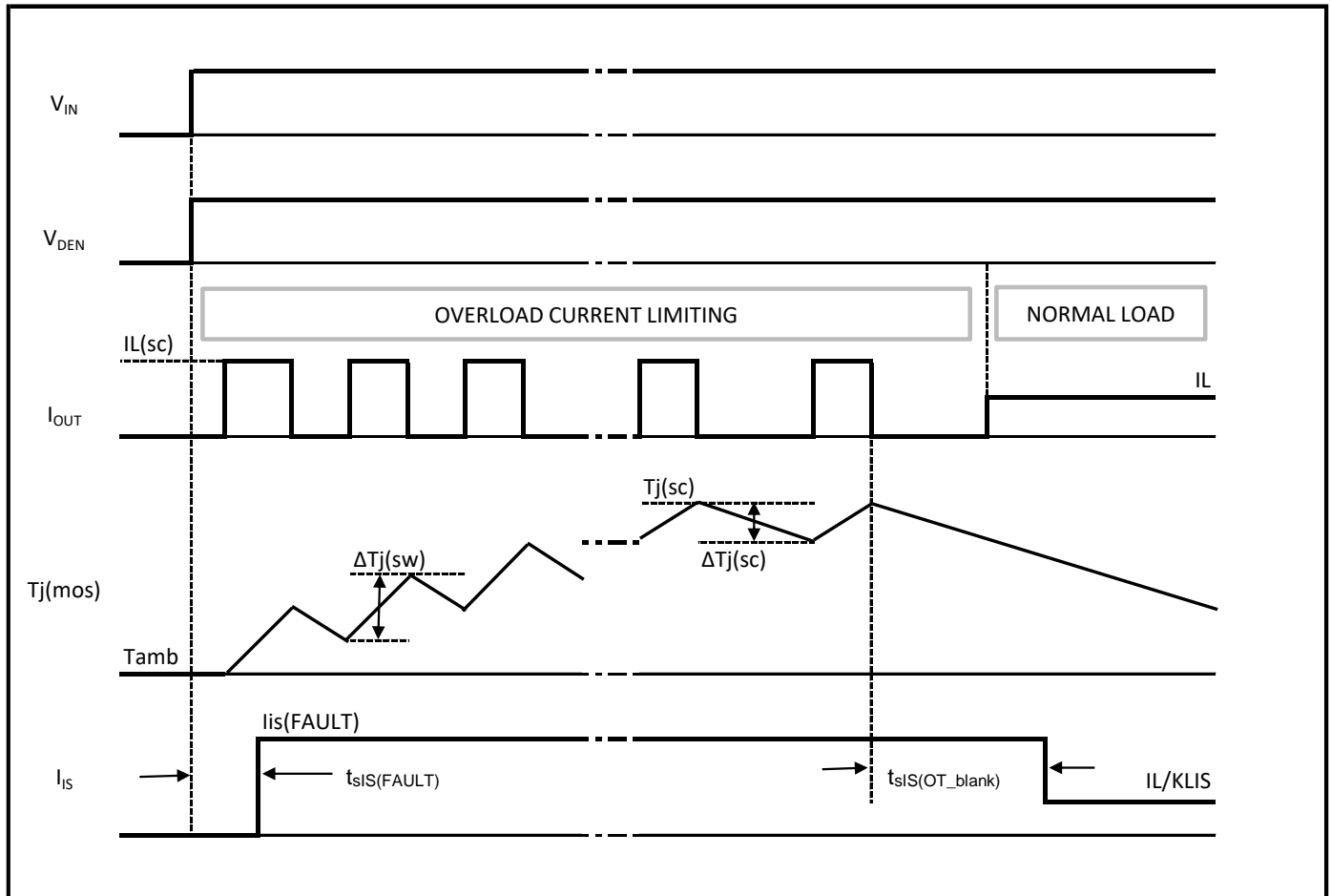


Figure 12. Overload Protection Diagram

Protection Electrical Characteristics

(Unless otherwise specified: $8V < V_S < 18V$, $-40^{\circ}C < T_J < +150^{\circ}C$; typical values based on $V_S = 13.5V$, $T_J = +25^{\circ}C$)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------------------|--|---|------|------|------|-------------|
| Loss of Ground Protection | | | | | | |
| $I_{OUT(GND)}$ | Output leakage current (Note 14) | $V_S = 28V$ GND disconnected | — | 0.1 | — | mA |
| Reverse Battery Protection | | | | | | |
| $V_{DS(REV)}$ | Reverse output voltage (Note 15) | $I_L = -1A$, $T_J = +150^{\circ}C$ | 0.2 | 0.65 | 0.7 | V |
| Overvoltage Protection | | | | | | |
| $V_{S(AZ)}$ | V_S to GND clamping | $I_S = 5mA$ | 41 | 47 | 53 | V |
| Overload Protection | | | | | | |
| $I_{L5(SC)}$ | Load current limit | $V_{DS} = 5V$ | 10 | 13.5 | 17 | A |
| $I_{L28(SC)}$ | Load current limit (Note 14) | $V_{DS} = 28V$ | — | 7 | — | A |
| $I_{L(RMS)}$ | Load current during over-temperature cycling (Note 14) | $R_{SHORT} = 0.1\Omega$ $L_{SHORT} = 5\mu H$ | — | 2 | — | A |
| $\Delta T_{J(SW)}$ | Dynamic temperature rise during cycling (Note 16) | — | — | 80 | — | K |
| $T_{J(SC)}$ | Thermal shutdown temperature (Note 17) | — | +150 | +170 | +200 | $^{\circ}C$ |
| $\Delta T_{J(SC)}$ | Thermal hysteresis (Note 17) | — | — | 20 | — | K |

Notes: 14. Not subject to production test, guaranteed by design.
 15. During reverse battery the body diode will conduct with a voltage drop $V_{DS(REV)}$.
 16. Functional test only.
 17. Functional test only at $T_J = +150^{\circ}C$.

Diagnostic Functionality – Detailed Description

In normal operation the IS pin outputs a small analog sense current proportional to the main OUT current flowing in the power MOSFET depending upon which channel is selected by the DSEL pin. In the case where it is disabled by the DEN pin it becomes high impedance.

| V_{DEN} | V_{DSEL} | IS Output |
|-----------|------------|-----------------------|
| L | X | Z |
| H | L | Channel 0 diagnostics |
| H | H | Channel 1 diagnostics |

Table 2. Diagnostic Truth Table

During overload/current limit operation/overtemperature/high temperature gradient or open load in the OFF-state, the IS pin outputs a defined current $I_{IS(FAULT)}$ greater than normal sense currents for normal loads.

During ON-state operation with open load, normal OFF-state, or OFF-state with inductive load ring-off current still flowing, the IS current is approximately zero.

Diagnostic Functionality – Detailed Description (continued)

| Operating Condition | V _{INx} | V _{DEN} | V _{OUTx} | IS Output Current, I _S (Note 18) |
|-------------------------------------|------------------|------------------|---|---|
| Normal operation | L H | H H | Z H | Z = I _L / K _{ILIS} |
| Current limiting | H | H | H | I _{S(FAULT)} |
| Short circuit OUT to GND | L H | H H | L L | Z I _{S(FAULT)} |
| Overtemperature | L H | H H | Z Z | Z I _{S(FAULT)} |
| Short circuit OUT to V _S | L H | H H | H H | I _{S(FAULT)} < I _L / K _{ILIS} (Note 19) |
| Open load | L L H | H H H | < V _{OL(OFF)} > V _{OL(OFF)} H | Z I _{S(FAULT)} (Note 20) < I _{S(OL)} |
| Inverse load current | L H | H H | H H | I _{S(FAULT)} I _{S(OL)} |
| All | X | L | X | Z |

Table 3. Operational Truth Table (Note 21)

- Notes:
- 18. The appropriate channel is selected by the DSEL pin.
 - 19. A low resistance short between OUT and V_S will reduce the output current, I_L and therefore reduce the analog sense current, I_S.
 - 20. With external pullup resistor.
 - 21. H = high level; L = low level; Z = high impedance, voltage depends on external circuit; X = don't care.

Diagnostic Diagrams

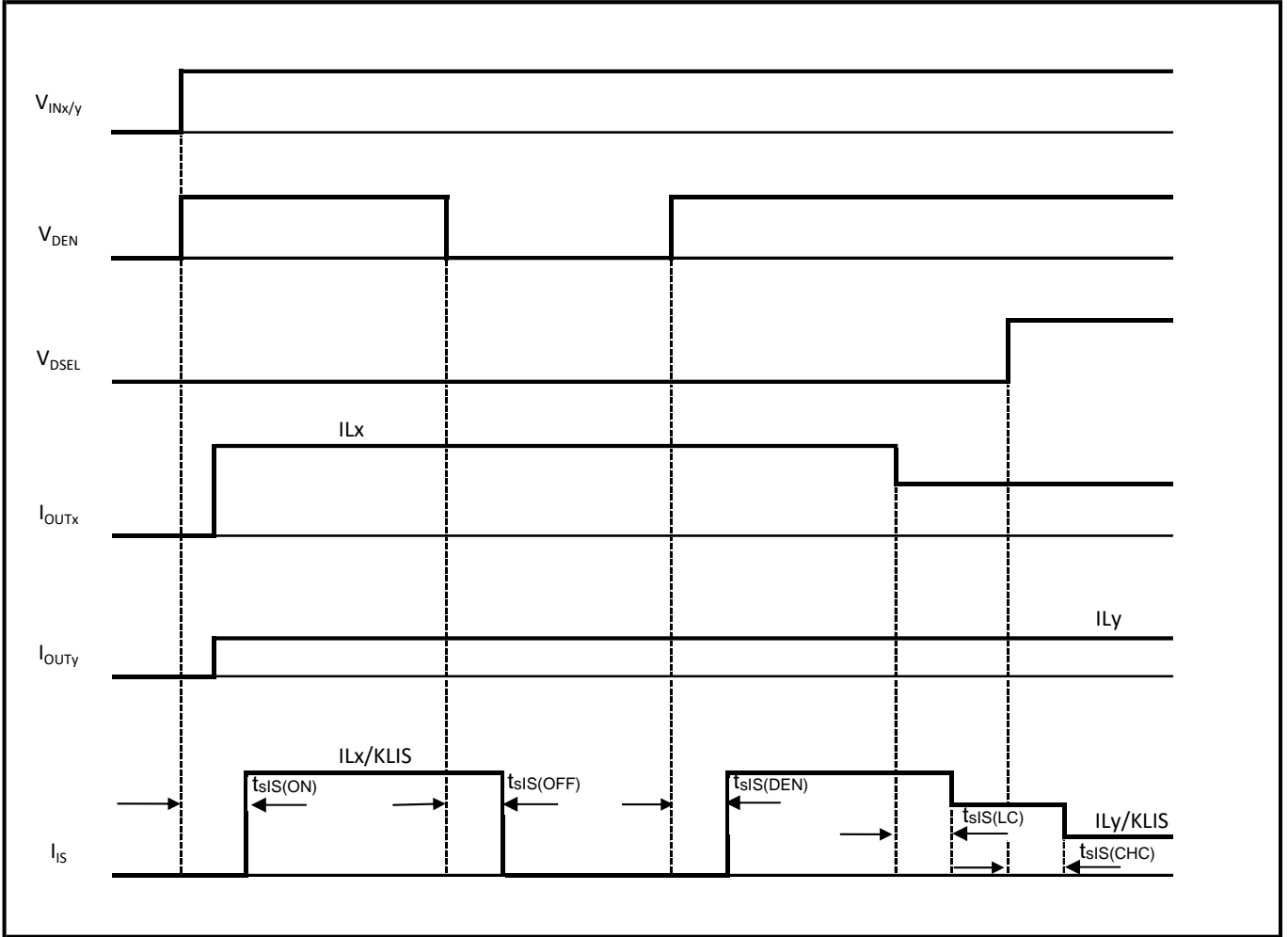


Figure 13. IS Signal Timing Diagram

Diagnostic Diagrams (continued)

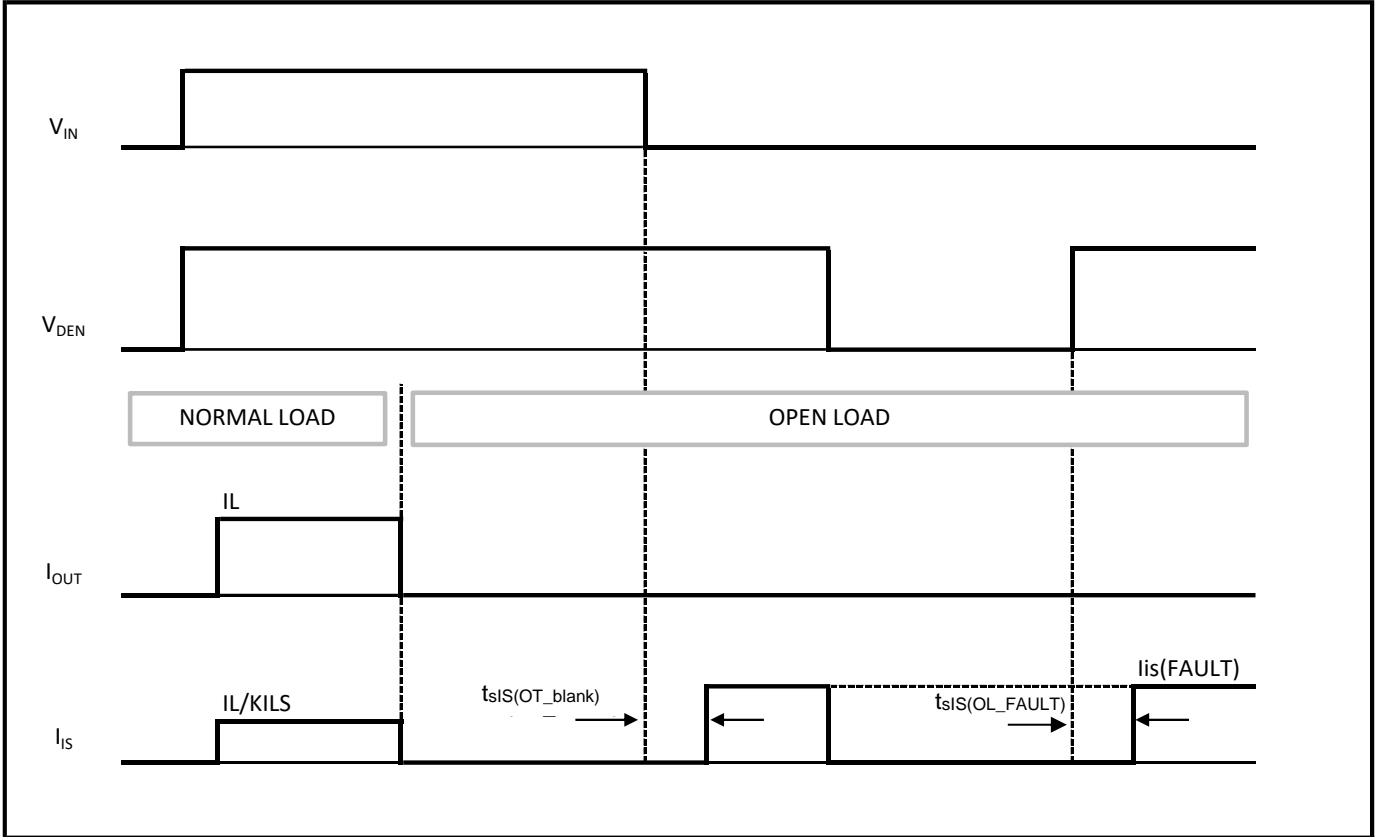


Figure 14. Open-Load Timing Diagram

Diagnostic Electrical Characteristics

(Unless otherwise specified: $8V < V_S < 18V$, $-40^{\circ}C < T_J < +150^{\circ}C$; typical values based on $V_S = 13.5V$, $T_J = +25^{\circ}C$)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------------|--|--|------|-----|------|---------|
| Open-Load Detection | | | | | | |
| $V_{DS(OL)}$ | Open load OFF state detection voltage | $V_{IN} = 0V$, $V_{DEN} = 4.5V$ | 4 | 4.9 | 6 | V |
| $I_{L(OL)}$ | Open load ON state detection current | $V_{IN} = V_{DEN} = 4.5V$ $I_{IS(OL)} = 22\mu A$ | 5 | — | 30 | mA |
| Current Sense Pin | | | | | | |
| $I_{IS(DIS)}$ | Current sense leakage current | $V_{IN} = 4.5V$, $V_{DEN} = 0V$ $I_L = 2A$ | — | — | 1 | μA |
| $V_{IS(SAT)}$ | VS to IS saturation voltage | $V_{IN} = 0V$, $V_{DEN} = 4.5V$ $I_{IS} = 6mA$, $V_{OUT} = V_S > 10V$ | — | — | 3 | V |
| $I_{IS(FAULT)}$ | Current sense under fault conditions | $V_{IN} = V_{IS} = 0V$, $V_{DEN} = 4.5V$ $V_{OUT} = V_S > 10V$ | 6 | 15 | 35 | mA |
| $V_{IS(AZ)}$ | VS to IS clamp voltage | $I_{IS} = 5mA$ | 41 | 47 | 53 | V |
| Load Current Sense | | | | | | |
| K_{ILIS0} | Sense current ratio $I_L = 50mA$ | $V_{IN} = V_{DEN} = 4.5V$ | -30% | 610 | +30% | — |
| K_{ILIS1} | Sense current ratio $I_L = 0.25A$ | | -21% | 590 | +21% | — |
| K_{ILIS2} | Sense current ratio $I_L = 0.5A$ | | -9% | 570 | +9% | — |
| K_{ILIS3} | Sense current ratio $I_L = 1A$ | | -6% | 560 | +6% | — |
| K_{ILIS4} | Sense current ratio $I_L = 2A$ | | -5% | 550 | +5% | — |
| ΔK_{ILIS} | Sense current ratio variation $I_L = 1A$ versus $I_L = 0.5A$ | | -6% | 0 | +6% | — |
| Diagnostic Timings | | | | | | |
| $t_{sIS(ON)}$ | Current sense settling time to 90% I_{IS} after IN and DEN high | $V_S = 13.5V$ $I_L = 1A$, $R_{IS} = 1.2k\Omega$ | — | — | 250 | μs |
| $t_{sIS(DEN)}$ | Current sense settling time to 90% I_{IS} after DEN high | $V_S = 13.5V$, $V_{IN} = 4.5V$ $I_L = 1A$, $R_{IS} = 1.2k\Omega$ | — | — | 20 | μs |
| $t_{sIS(LC)}$ | Current sense settling time to 90% I_{IS} after load current change | $V_S = 13.5V$, $V_{IN} = V_{DEN} = 4.5V$ $I_L = 0.5A$ to $1A$, $R_{IS} = 1.2k\Omega$ | — | — | 20 | μs |
| $t_{sIS(OL_FAULT)}$ | Diagnostic fault current settling time to 90% $I_{IS(FAULT)}$ after DEN high with OFF state open-load condition | $V_{IN} = 0V$, $V_{OUT} = V_S = 13.5V$ $R_{IS} = 1.2k\Omega$ | — | — | 150 | μs |
| $t_{sIS(FAULT)}$ | Diagnostic fault current settling time to 90% $I_{IS(FAULT)}$ after IN and DEN high with overload condition | $V_{DS} = 5V$, $R_{IS} = 1.2k\Omega$ | — | — | 250 | μs |
| $t_{sIS(OT_blank)}$ | Diagnostic fault current off delay time to 90% $I_{IS(FAULT)}$ after overtemperature condition returning to normal operation (Note 22) | $V_{IN} = V_{DEN} = 4.5V$ $R_{IS} = 1.2k\Omega$ | — | 150 | — | μs |
| $t_{sIS(OFF)}$ | Current sense fall time to < 50% I_{IS} after DEN low | $V_{IN} = 4.5V$, $I_L = 1A$ $R_{IS} = 1.2k\Omega$ | — | — | 30 | μs |
| $t_{sIS(ChC)}$ | Current sense settling time to 90% I_{IS} after DSEL high | $V_S = 13.5V$, $V_{IN0} = V_{IN1} = 4.5V$ $V_{DEN} = 4.5V$ $I_{L0} = 1A$, $I_{L1} = 0.5A$ $R_{IS} = 1.2k\Omega$ | — | — | 20 | μs |

Note: 22. Not subject to production test, guaranteed by design.

Input Pins

The input circuit is compatible with 3.3V and 5V logic levels. The input diode provides ESD protection. If the pin is left open the internal tie down resistor will keep the output off. A Schmitt trigger provides switching hysteresis to avoid an undefined state if there is a slowly rising or falling voltage on the IN pin. Figure 15 shows the electrical equivalent circuit.

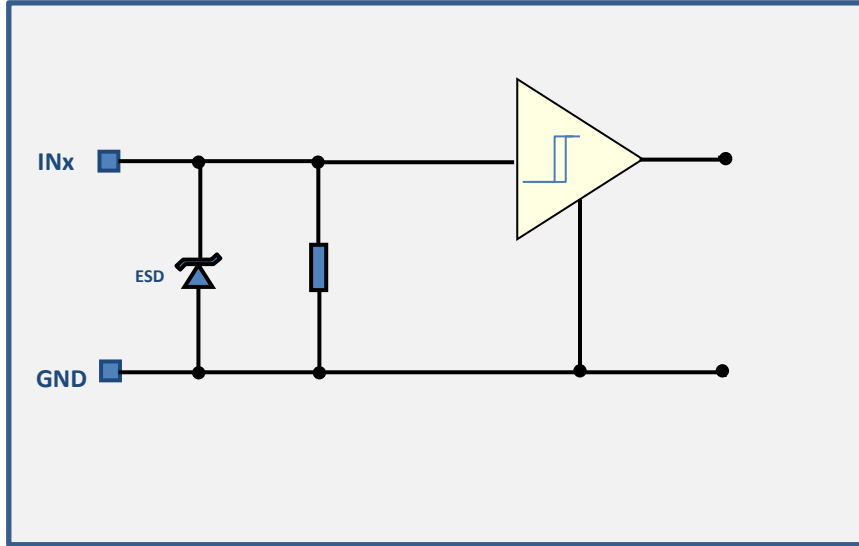


Figure 15. Input Pin Circuitry

The DEN and DSEL pins have the same circuitry as the IN pin.

Input Electrical Characteristics

(Unless otherwise specified: $8V < V_S < 18V$, $-40^{\circ}C < T_J < +150^{\circ}C$; typical values based on $V_S = 13.5V$, $T_J = +25^{\circ}C$)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|--------------------------|-------------------|------|------|-----|---------|
| INx Pin | | | | | | |
| $V_{IN(L)}$ | Low level input voltage | — | -0.3 | — | 0.8 | V |
| $V_{IN(H)}$ | High level input voltage | — | 2 | — | 6 | V |
| $V_{IN(HYS)}$ | Input voltage hysteresis | — | — | 0.25 | — | V |
| $I_{IN(L)}$ | Low level input current | $V_{IN} = 0.8V$ | 1 | 3 | 25 | μA |
| $I_{IN(H)}$ | High level input current | $V_{IN} = 5.5V$ | 2 | 8 | 25 | μA |
| DEN Pin | | | | | | |
| $V_{DEN(L)}$ | Low level input voltage | — | -0.3 | — | 0.8 | V |
| $V_{DEN(H)}$ | High level input voltage | — | 2 | — | 6 | V |
| $V_{DEN(HYS)}$ | Input voltage hysteresis | — | — | 0.25 | — | V |
| $I_{DEN(L)}$ | Low level input current | $V_{DEN} = 0.8V$ | 1 | 3 | 25 | μA |
| $I_{DEN(H)}$ | High level input current | $V_{DEN} = 5.5V$ | 2 | 8 | 25 | μA |
| DSEL Pin | | | | | | |
| $V_{DSEL(L)}$ | Low level input voltage | — | -0.3 | — | 0.8 | V |
| $V_{DSEL(H)}$ | High level input voltage | — | 2 | — | 6 | V |
| $V_{DSEL(HYS)}$ | Input voltage hysteresis | — | — | 0.25 | — | V |
| $I_{DSEL(L)}$ | Low level input current | $V_{DSEL} = 0.8V$ | 1 | 3 | 25 | μA |
| $I_{DSEL(H)}$ | High level input current | $V_{DSEL} = 5.5V$ | 2 | 8 | 25 | μA |

Characterisation – General Product

Minimum Functional Supply Voltage

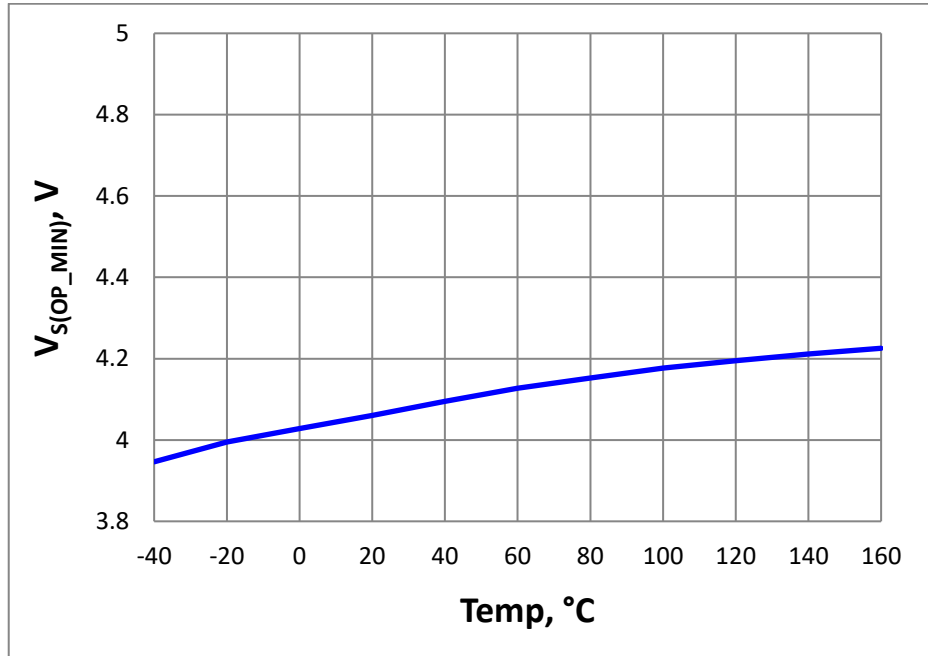


Figure 16. Minimum Functional Supply Voltage $V_{S(OP_MIN)} = f(T_J)$

Undervoltage Shutdown

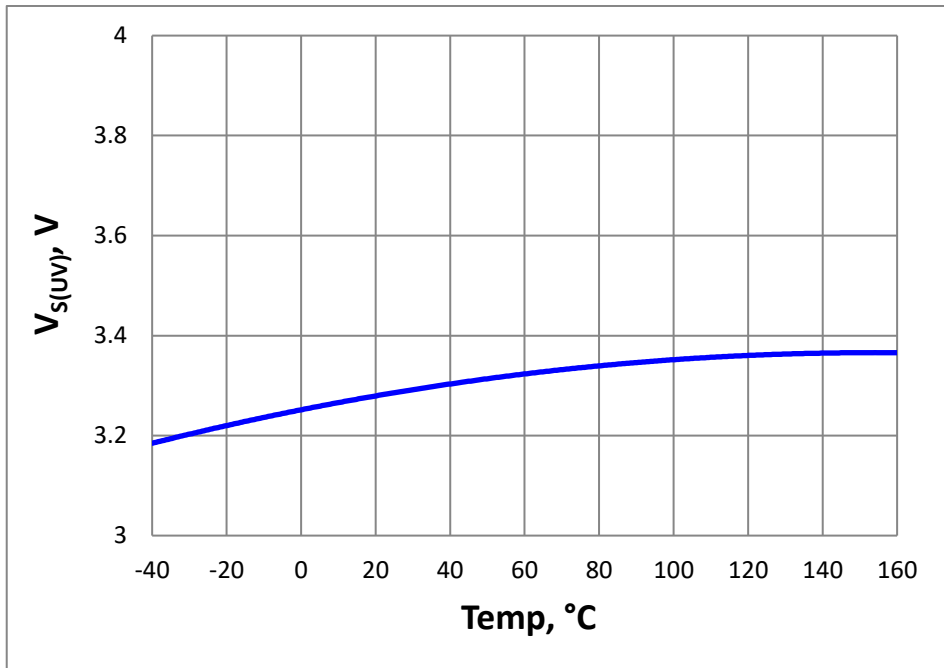


Figure 17. Undervoltage Shutdown $V_{S(UV)} = f(T_J)$

Characterisation – General Product (continued)

Current Consumption One Channel Active

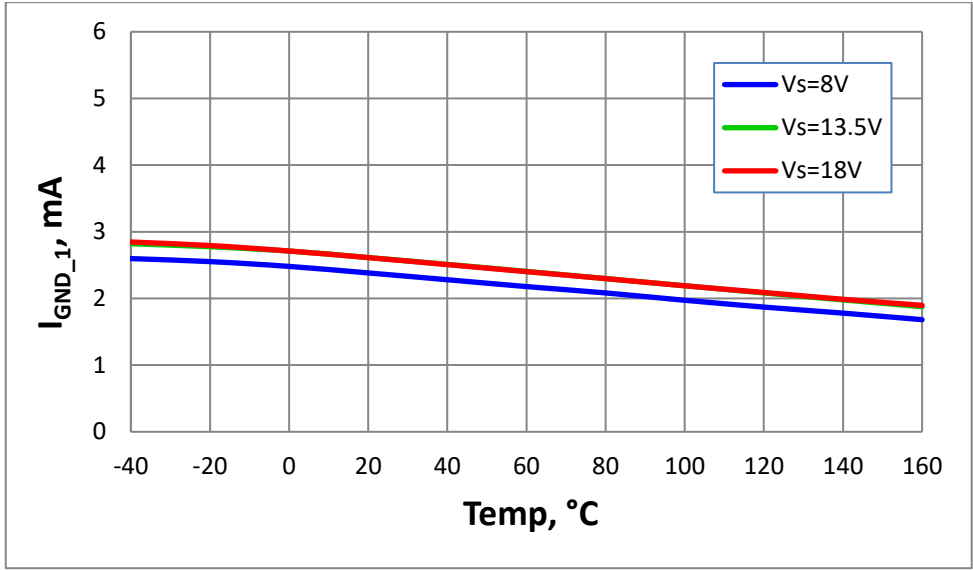


Figure 18. Current Consumption for Whole Device with Load, $I_{GND} = f(T_J; V_s)$

Current Consumption Two Channels Active

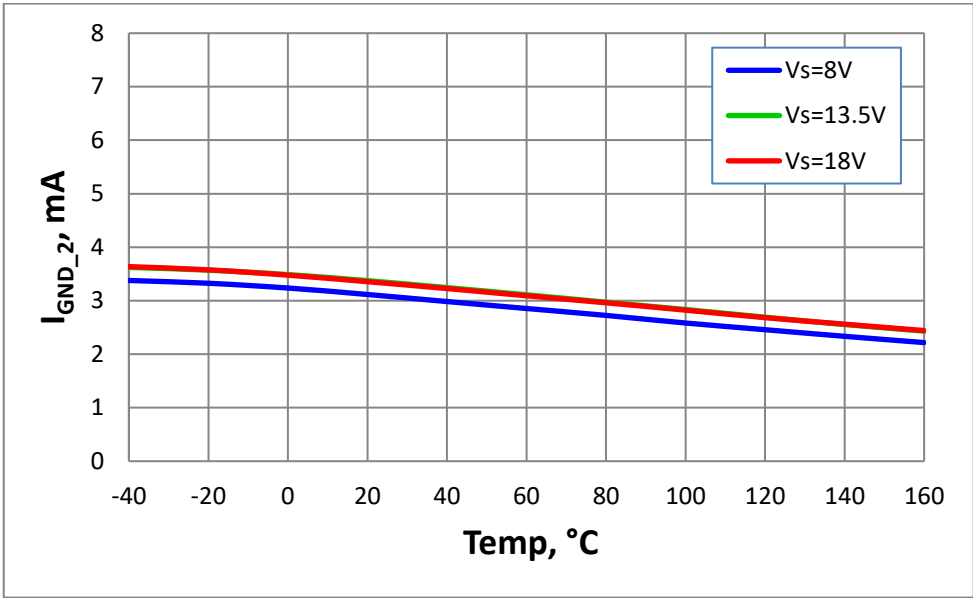


Figure 19. Current Consumption for Whole Device with Load, $I_{GND} = f(T_J; V_s)$

Characterisation – General Product (continued)

Standby Current for Whole Device with Load

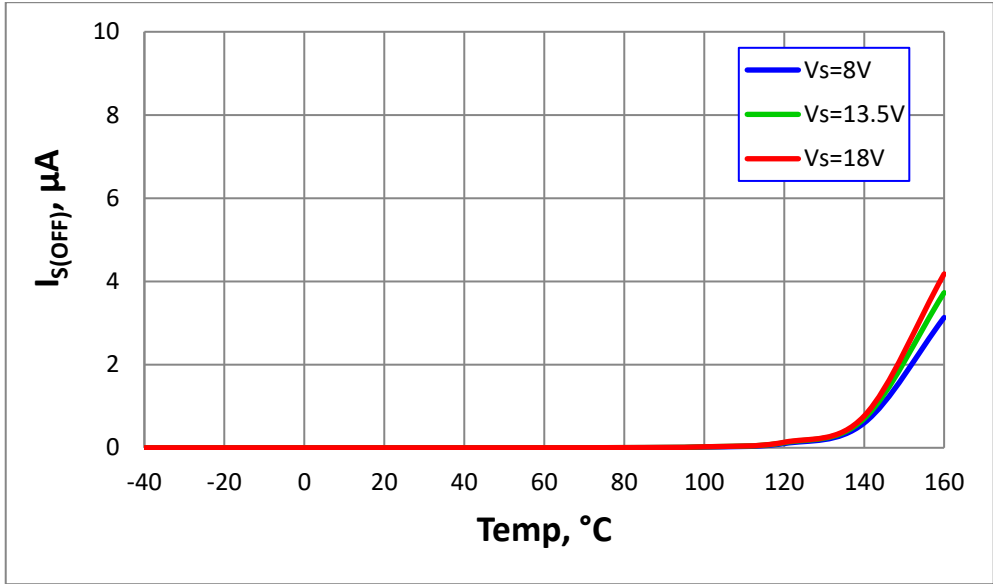


Figure 20. Standby Current for Whole Device with Load, $I_{S(OFF)} = f(T_J; V_S)$

Characterisation – Power Stage

Output Voltage Drop Limitation at Low Load Current

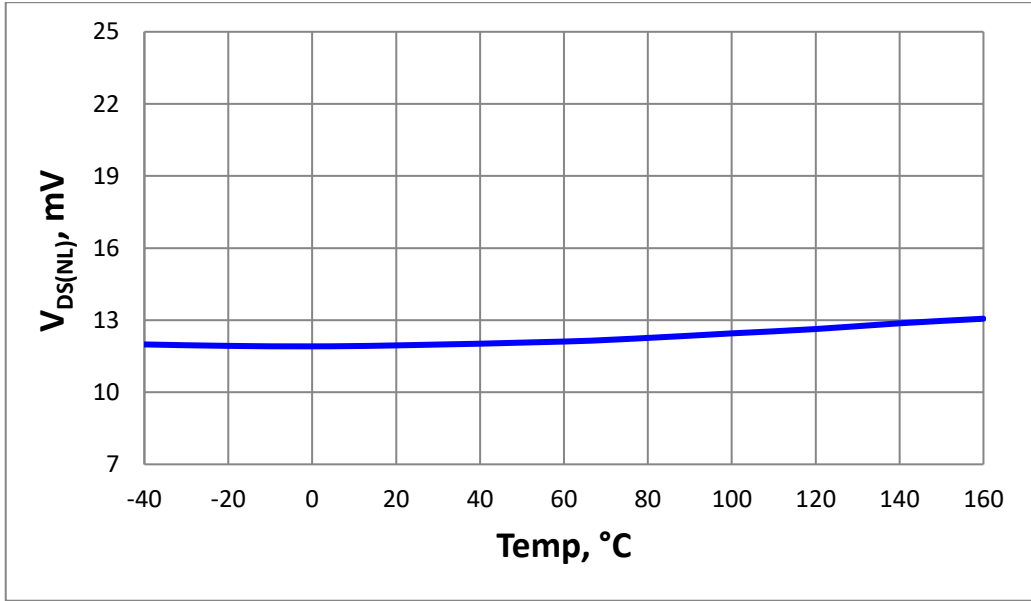


Figure 21. Output Voltage Drop Limitation at Low Load Current $V_{DS(NL)} = f(T_J; V_S)$

Drain to Source Clamp Voltage

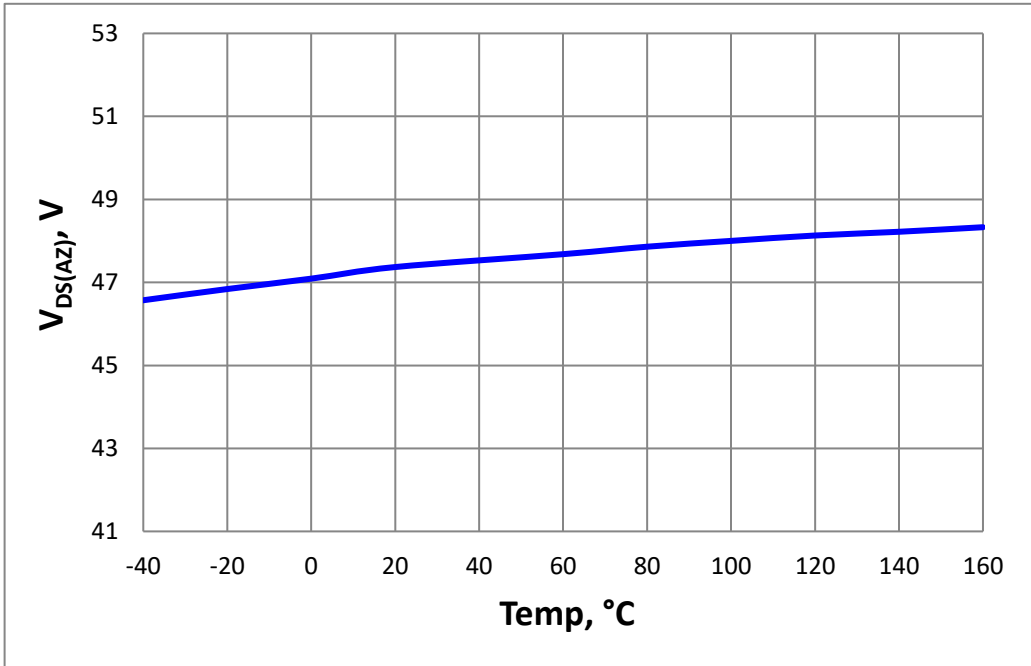


Figure 22. Drain to Source Clamp Voltage $V_{DS(AZ)} = f(T_J)$

Characterisation – Power Stage (continued)

Slew Rate at Turn ON

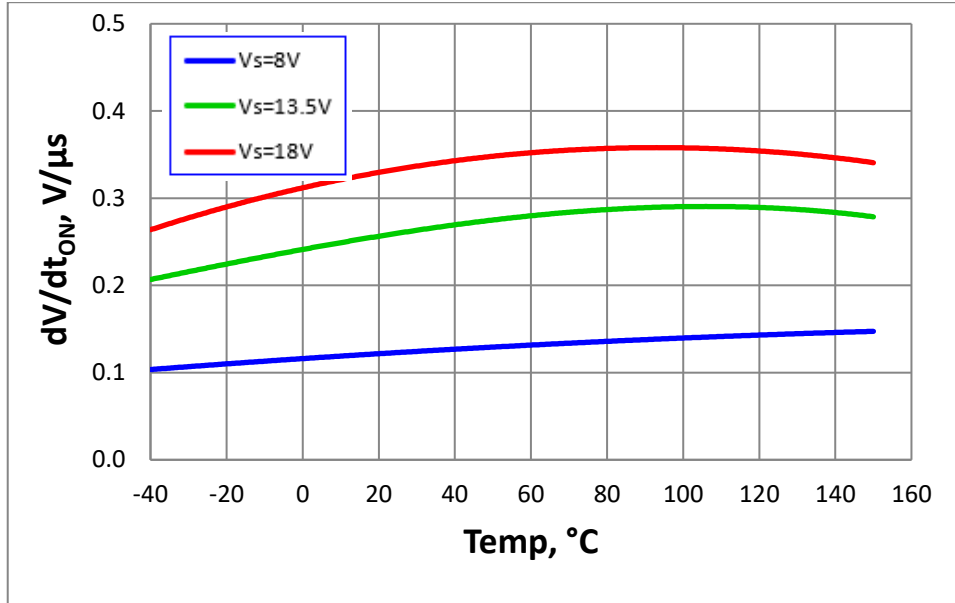


Figure 23. Slew Rate at Turn ON $dV/dt_{ON} = f(T_J; V_s)$

Slew Rate at Turn OFF

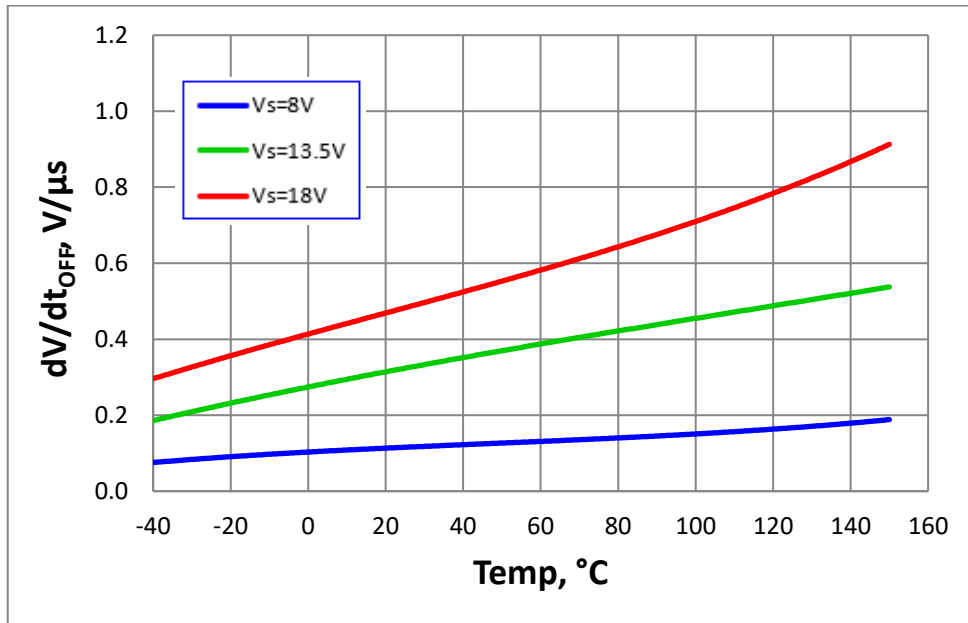


Figure 24. Slew Rate at Turn OFF $dV/dt_{OFF} = f(T_J; V_s)$

Characterisation – Power Stage (continued)

Turn ON Time

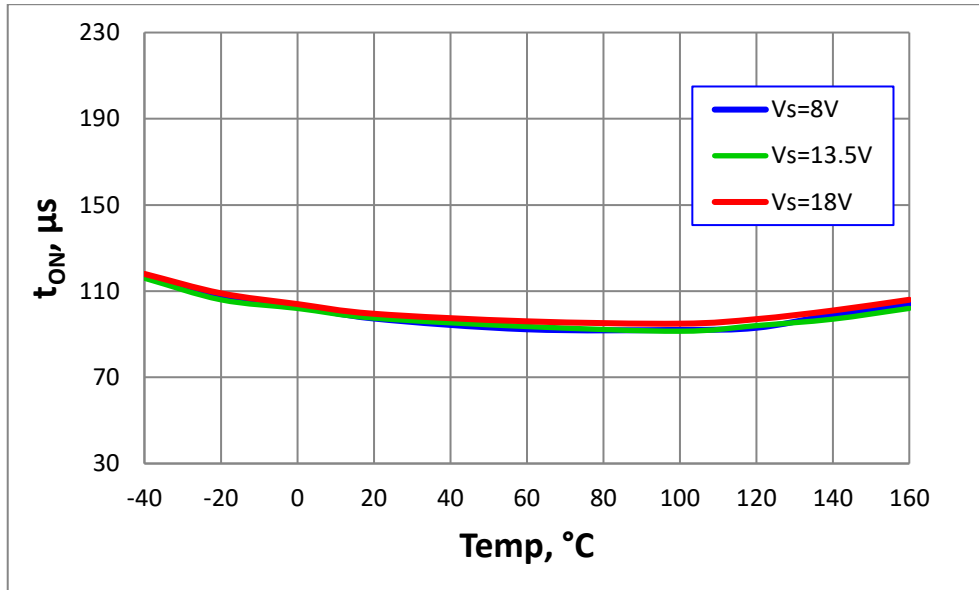


Figure 25. Turn ON $t_{ON} = f(T_J; V_S)$, $R_L = 12\Omega$

Turn OFF Time

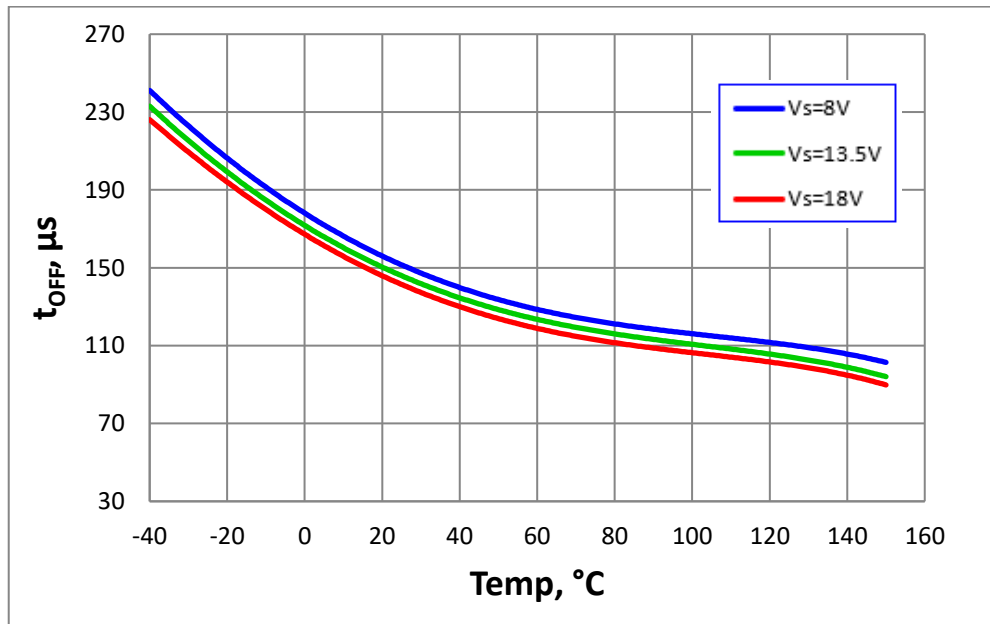


Figure 26. Turn OFF $t_{OFF} = f(T_J; V_S)$, $R_L = 12\Omega$

Characterisation – Power Stage (continued)

Switch ON Energy

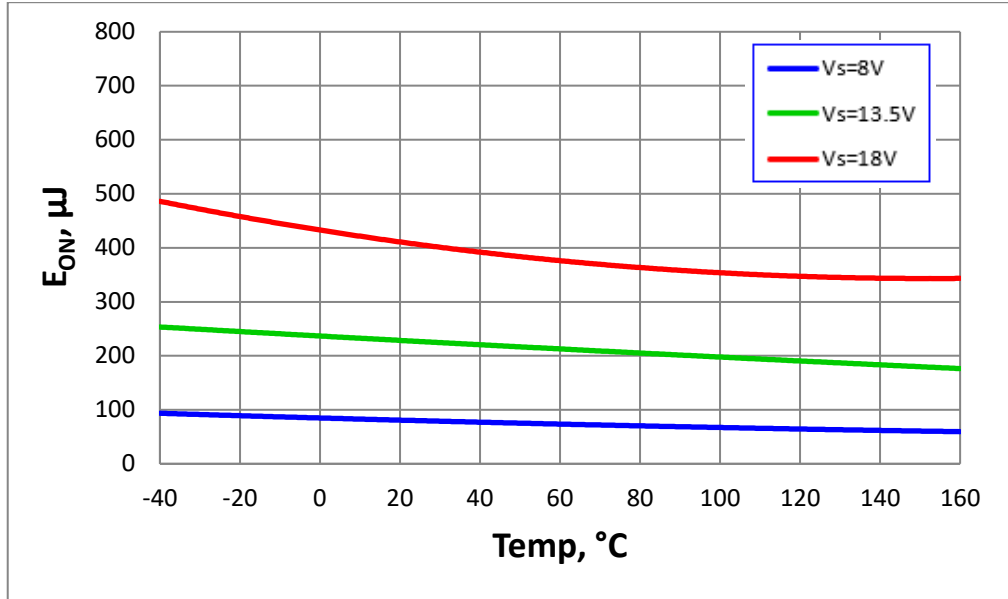


Figure 27. Switch ON Energy $E_{ON} = f(T_J; V_s)$, $R_L = 12\Omega$

Switch OFF Energy

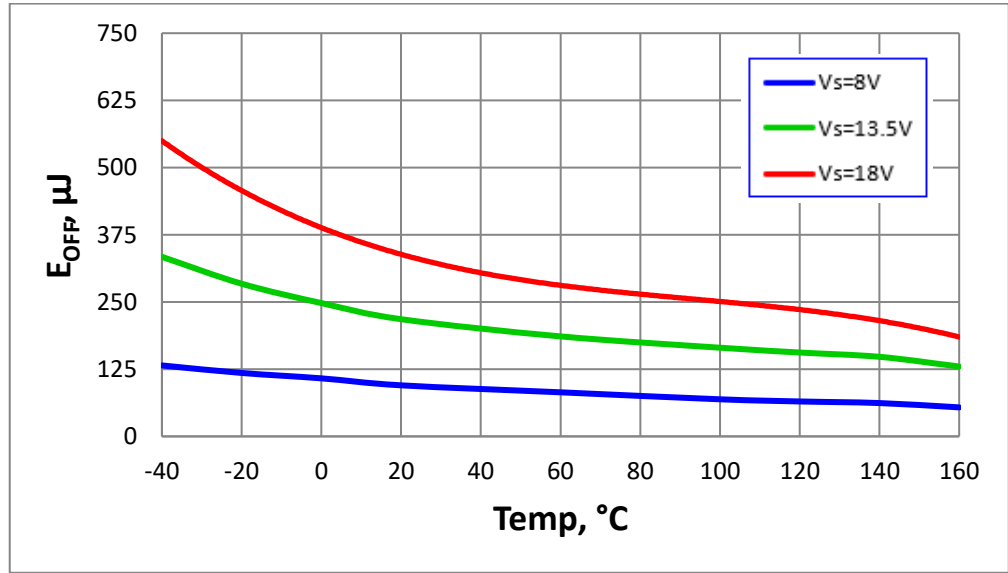


Figure 28. Switch OFF Energy $E_{OFF} = f(T_J; V_s)$, $R_L = 12\Omega$

Characterisation – Protection

Overload Condition with Low Output Voltage Drop

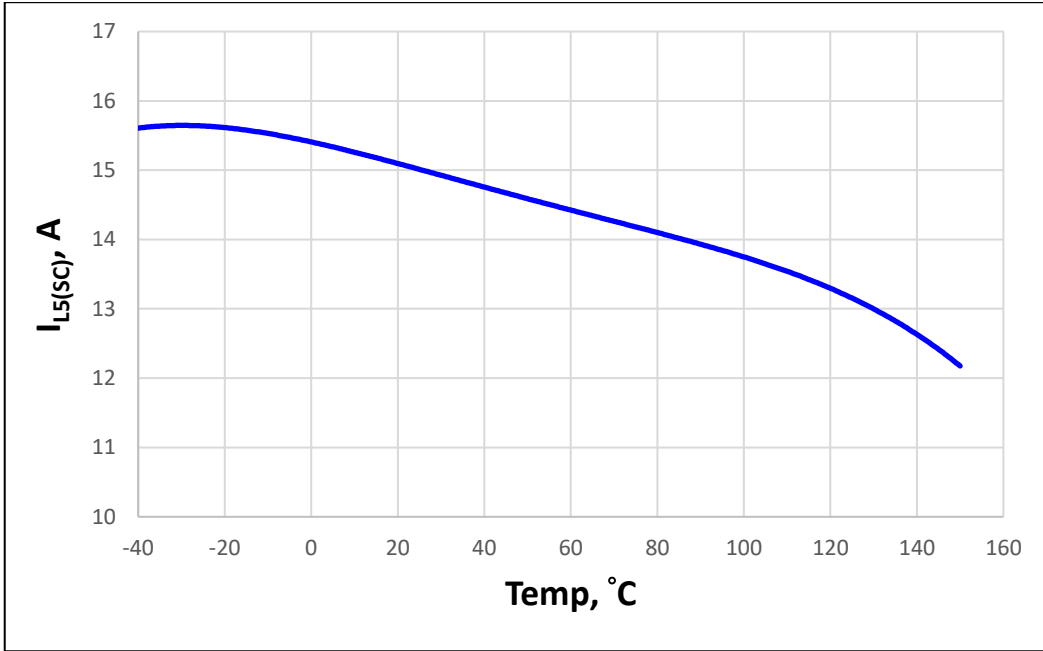


Figure 29. Overload Condition with Low Output Voltage Drop $I_{L5(SC)} = f(T_J)$

Overload Condition with High Output Voltage Drop

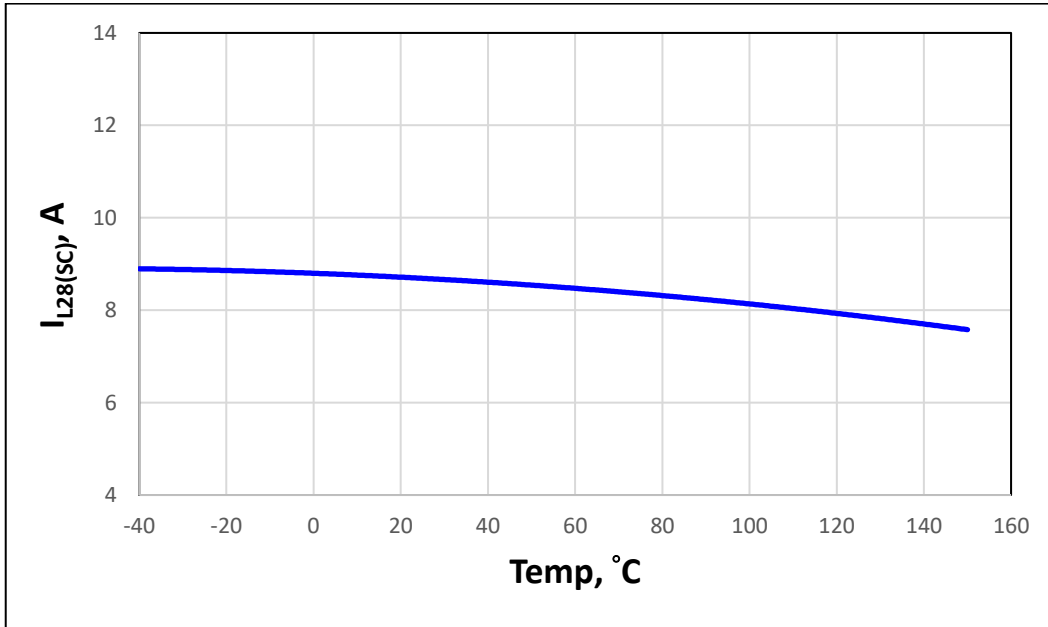


Figure 30. Overload Condition with High Output Voltage Drop $I_{L28(SC)} = f(T_J)$

Characterisation – Diagnostic Mechanism

Current Sense at No Load

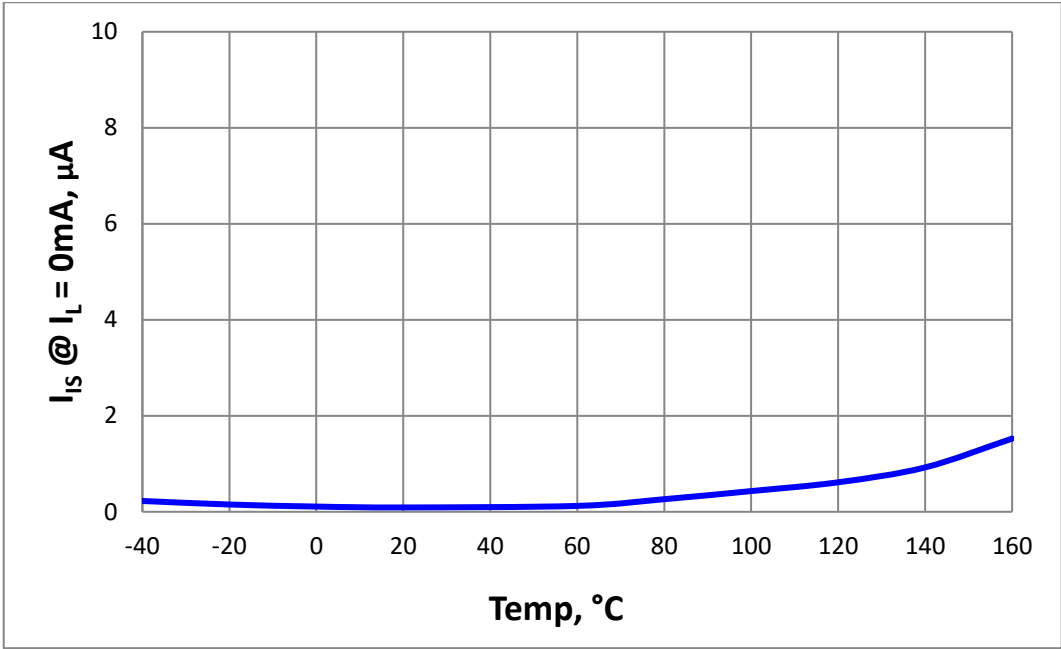


Figure 31. Current Sense at No Load $I_s = f(T_j)$

Open-Load Detection Threshold in ON State

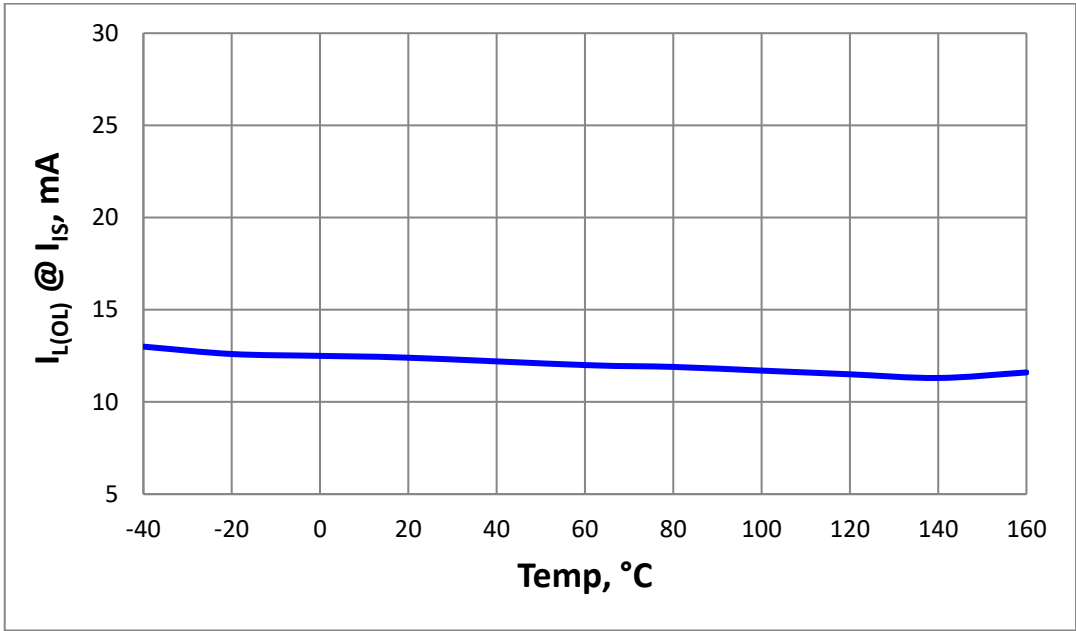


Figure 32. Open-Load Detection ON State Threshold $I_{L(OL)} = f(T_j)$

Characterisation – Diagnostic Mechanism (continued)

Sense Signal Maximum Voltage

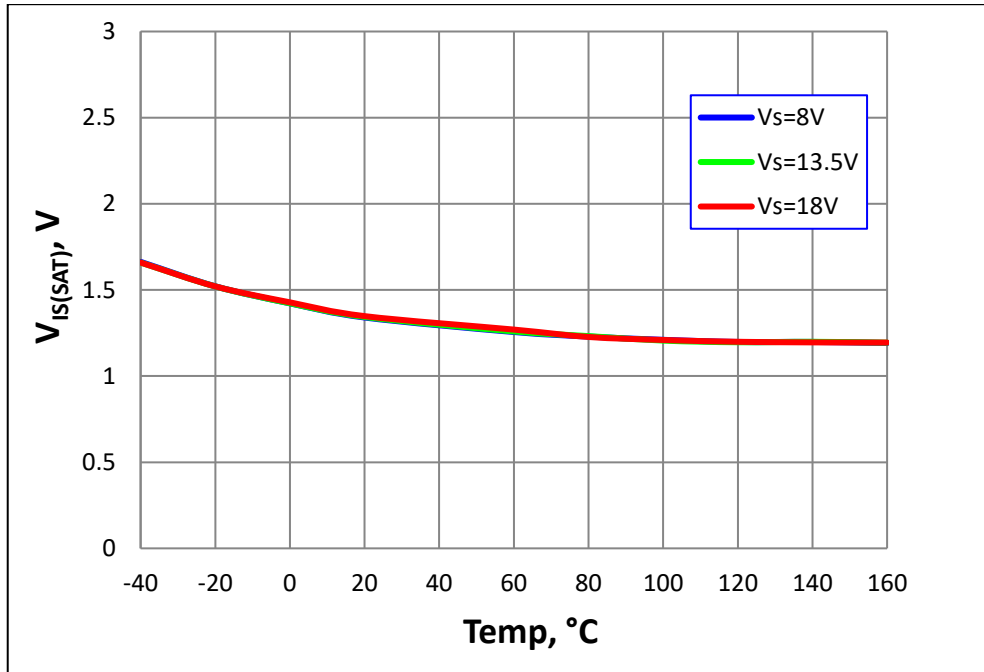


Figure 33. Sense Signal Maximum Voltage $V_{IS(SAT)} = f(T_J; V_S)$

Sense Signal Maximum Current

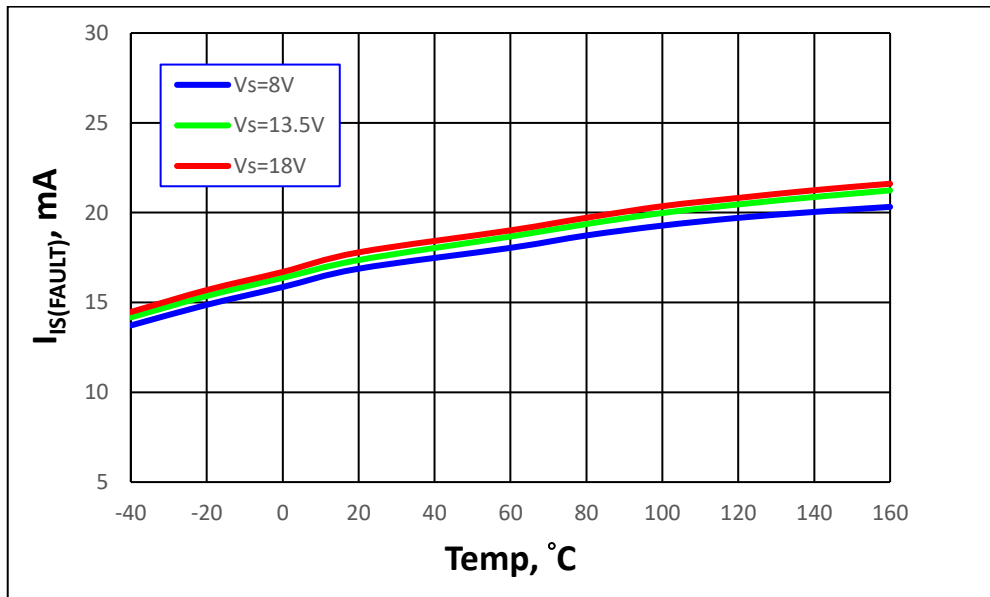


Figure 34. Sense Signal Maximum Current in Fault Condition $I_{IS(FAULT)} = f(T_J; V_S)$

Characterisation – Input Pins

Input Voltage Threshold ON to OFF

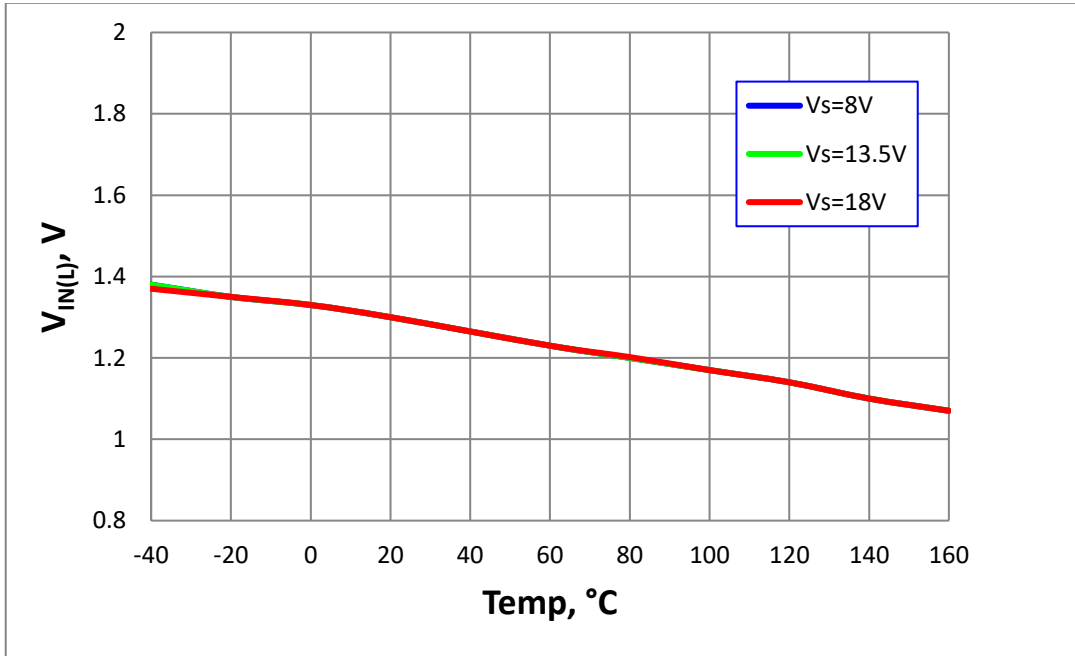


Figure 35. Input Voltage Threshold $V_{IN(L)} = f(T_J; V_S)$

Input Voltage Threshold OFF to ON

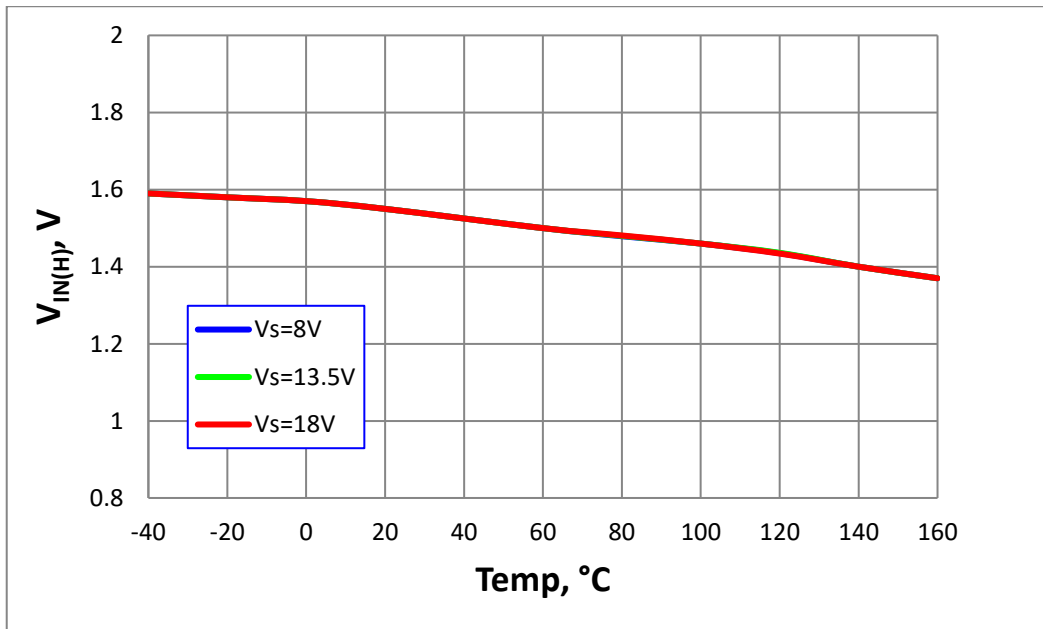


Figure 36. Input Voltage Threshold $V_{IN(H)} = f(T_J; V_S)$

Characterisation – Input Pins (continued)

Input Voltage Hysteresis

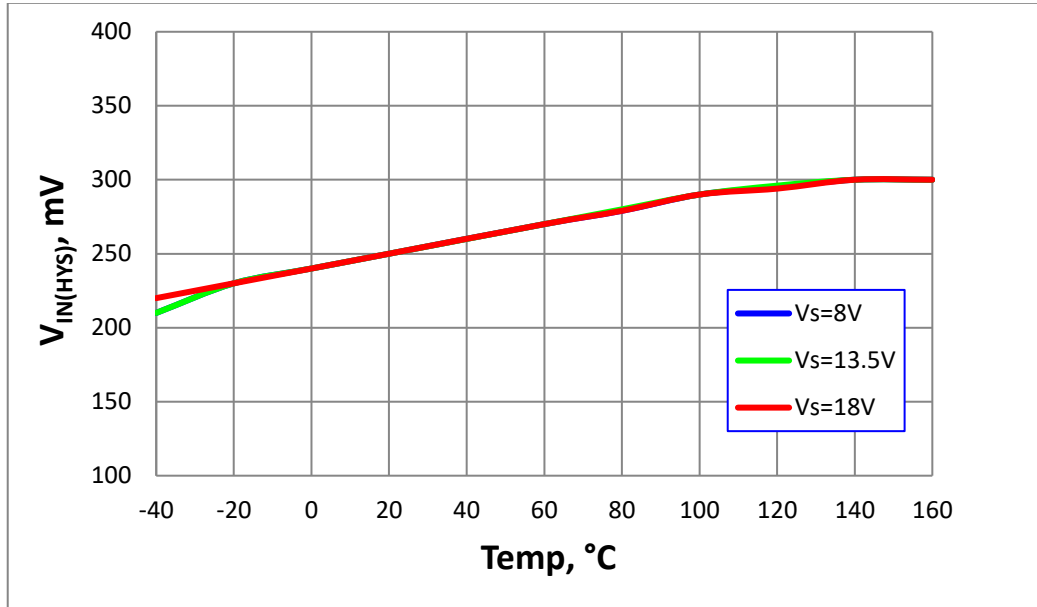


Figure 37. Input Voltage Hysteresis $V_{IN(HYS)} = f(T_J; V_s)$

Input Current High Level

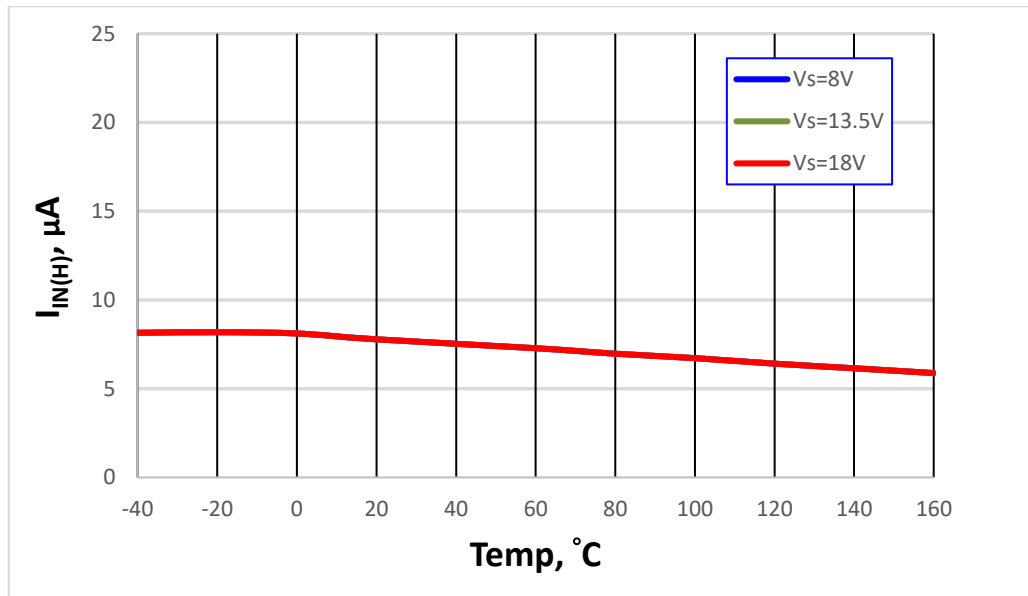


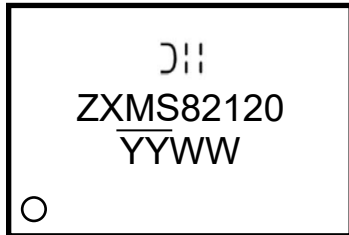
Figure 38. Input Current High Level $I_{IN(H)} = f(T_J; V_s)$

Ordering Information (Note 24)

| Part Number | Package | Marking | Reel Size (inches) | Tape Width (mm) | Packing | |
|------------------|---------|-----------|--------------------|-----------------|---------|---------|
| | | | | | Qty. | Carrier |
| ZXMS82120S14P-13 | SO-14EP | ZXMS82120 | 13 | 16 | 2500 | Reel |

Note: 24. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information

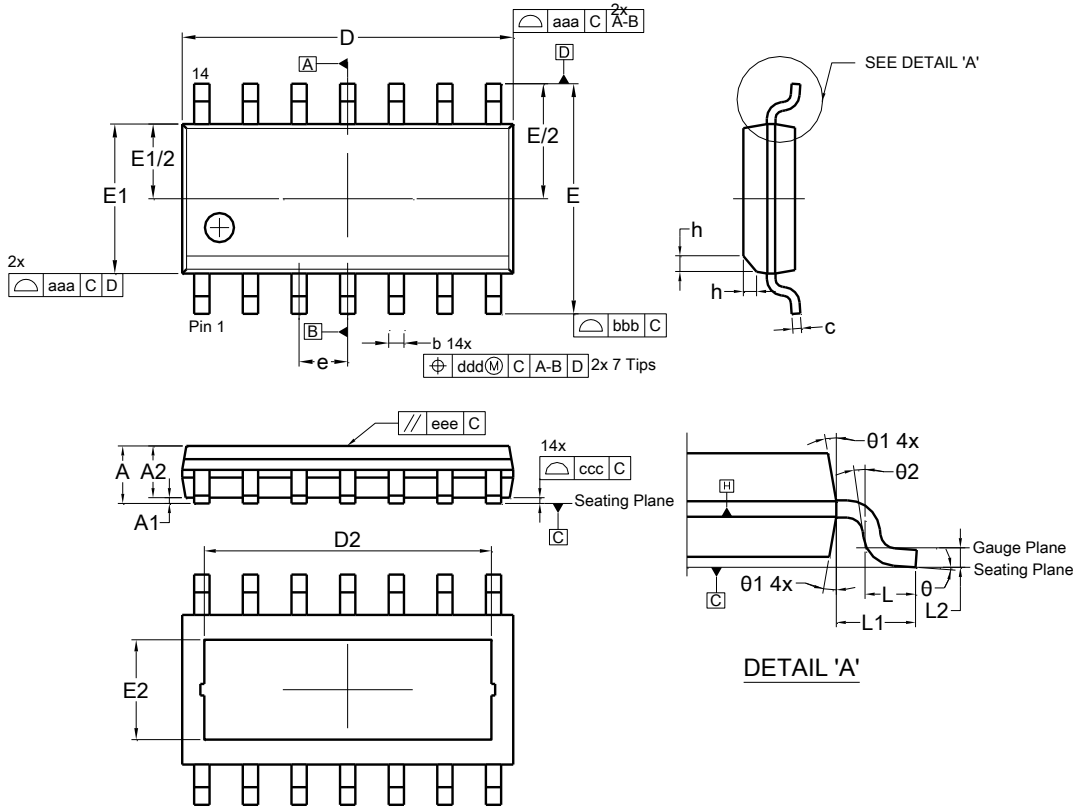


DII: Manufacturer's Code Marking
 ZXMS82120: Product Type Marking Code
 YY or YY: Year (ex: 23 = 2023)
 WW or WW: Week 01 to 52;
 52 represents week 52 and 53

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

SO-14EP

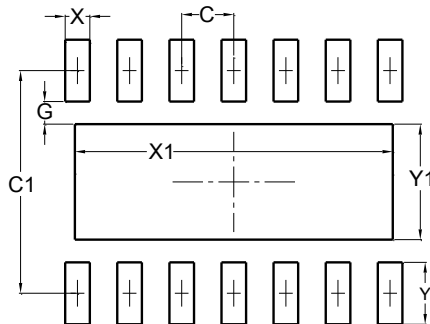


| SO-14EP | | | |
|----------------------|----------|------|------|
| Dim | Min | Max | Typ |
| A | -- | 1.75 | -- |
| A1 | 0.00 | 0.10 | -- |
| A2 | 1.25 | 1.55 | -- |
| b | 0.31 | 0.51 | -- |
| c | 0.10 | 0.25 | -- |
| D | 8.55 | 8.75 | -- |
| D2 | 7.40 | 7.60 | 7.50 |
| E | 5.80 | 6.20 | -- |
| E1 | 3.80 | 4.00 | -- |
| E2 | 2.50 | 2.70 | 2.60 |
| e | 1.27 BSC | | |
| h | 0.25 | 0.50 | -- |
| L | 0.40 | 1.27 | -- |
| L1 | 1.04 REF | | |
| L2 | 0.25 BSC | | |
| θ | 0° | 8° | -- |
| θ1 | 5° | 15° | -- |
| θ2 | 0° | -- | -- |
| aaa | 0.10 | | |
| bbb | 0.20 | | |
| ccc | 0.10 | | |
| ddd | 0.25 | | |
| eee | 0.10 | | |
| All Dimensions in mm | | | |

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

SO-14EP



| Dimensions | Value (in mm) |
|------------|---------------|
| C | 1.270 |
| C1 | 5.400 |
| G | 0.550 |
| X | 0.600 |
| X1 | 7.750 |
| Y | 1.500 |
| Y1 | 2.800 |

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 (E3)
- Weight: 0.15 grams (Approximate)

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